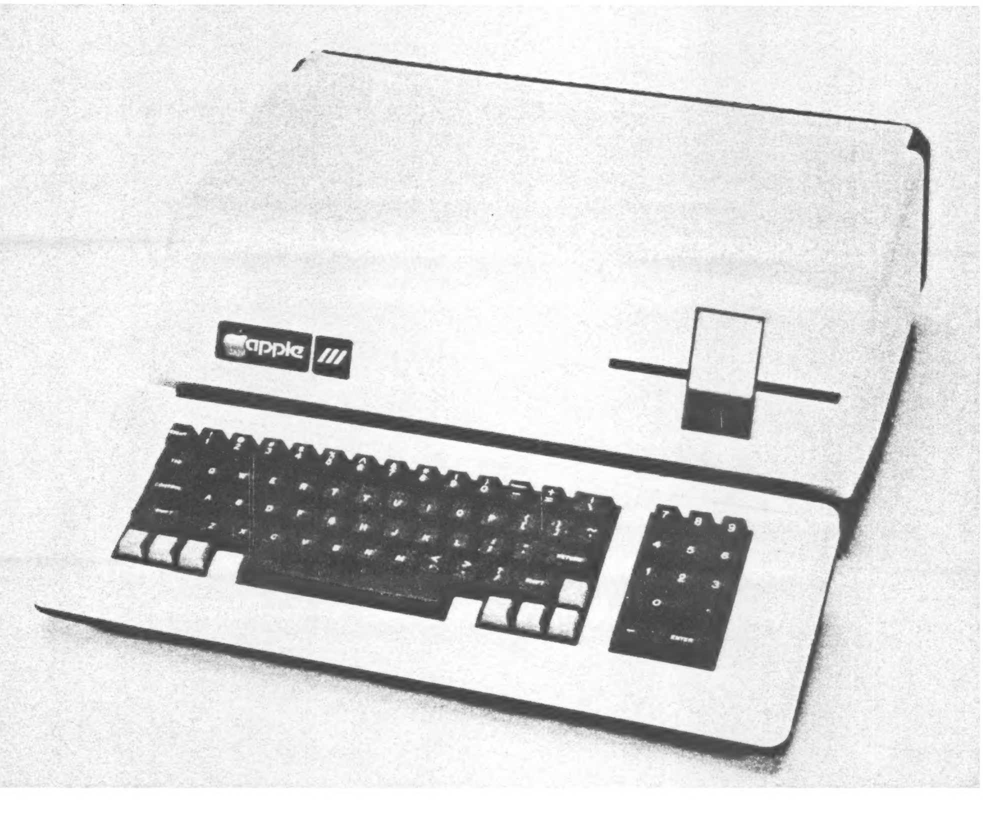
apple service



APPLE III
SERVICE REFERENCE
MANUAL

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         *
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   **** * ****
 ***************          **   **   **
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  **************     **   **   **
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TO: All Apple /// User Groups

Bob Cummings

FROM: Bob Cummings, A/// Product Manager

SUBJECT: "Apple /// Service Reference Manual"

DATE: May 16, 1984

The enclosed "Apple /// Service Reference Manual" is for the exclusive use of your users group. We thought it would be beneficial to all of your members. It's our way of saying "Thank you" for being such avid supporters of the Apple ///.

Thanks again.

TABLE OF CONTENTS

PAGE

SECTION I. THEORY OF OPERATION

CHAPTER 1 INTRODUCTION

General Description 1.1
Simplified Functional Description 1.4
The Main Logic Board 1.4
The Memory Board 1.6
The Keyboard PCB 1.7
The Disk Drive 1.7
The Apple /// Power Supply 1.7

CHAPTER 2 MEMORY & MEMORY ADDRESSING

Introduction to the Apple /// Memory 2.1
Simplified Memory Logic 2.1
Memory Addressing: Block Flow 2.4
The Processor 2.4
Memory Address Multiplexer 2.6
RAS/CAS Decode 2.6
Alternate Stack 2.10
Memory & Memory Addressing Appendices 2.12

CHAPTER 3 THE VERSATILE INTERFACE ADAPTER

General 3.1
VIA 6522 Pin Descriptions 3.1
VIA Functional Description 3.6
Interrupt Operation 3.8
6522 VIA Environment and Control 3.10
VIA (FFDX) 3.12
VIA (FFEX) 3.15
VIA Appendices 3.18

CHAPTER 4 THE ACIA

The 6551 Asynchonous Communications Interface Adapter 4.1
Status Register 4.3
Command Register 4.4
Control Register 4.5
Simple Serial Port 4.6

CHAPTER 5 SYSTEM CLOCKS & TIMING

Main Clock C14M 5.1
Frequency Divider 5.1
"Q" Timing 5.1
HPE* Freeze 5.5
Ax, PRE1M, & C1M 5.5
RAS (Row Address Strobe[Select]) 5.5
Video Horizontal & Vertical State Counters 5.7
Horizontal Section 5.7
Vertical Section 5.10

CHAPTER 6 VIDEO DISPLAY LOGIC

Display Modes 6.1
Introduction 6.2
40 Character Apple][6.2
40 Character Apple /// 6.3
80 Character Black & White Apple /// 6.3
Black & White Hires 6.4
Medium Resolution 16 Color Graphics Apple /// 6.4
Super Hires Apple /// 6.5
Apple /// Hires 6.5
Super Hires Apple /// 6.7
Video Appendix 6.9

CHAPTER 7 INPUT/OUTPUT

Description 7.1
Interface Control Signals 7.1
Interrupts 7.2
Addressing the I/O 7.2
The Input Operation 7.3
The Output Operation 7.3
System Timing 7.3
the A/// Joystick 7.5

CHAPTER 8 THE KEYBOARD

The Keyboard 8.1
Reading the Keyboard 8.1
Keyboard Codes 8.6
The Apple][Emulation Mode 8.7
Electronic Circuit Description 8.7
The Repeat Function 8.8
The Reset Function 8.8
Keyboard Light 8.8

CHAPTER 9 POWER SUPPLY

The Apple /// Power Supply 9.1
The Basic Switching Power Supply 9.1
How it works! 9.3
Detailed Hardware Description 9.6
Schematic 9.9
Parts List 9.10
Component Layout 9.13

CHAPTER 10 A][EMULATION

A][Emulation Restrictions 10.1
The Color Video Connector 10.2
The High-Resolution Graphics (Hi-Res) Mode 10.3
The Speaker 10.3
The Cassette Interface 10.3
Input/Output Special Locations 10.4
A/D Selection 10.4
Analog Inputs 10.5
Strobe Output 10.5
Autostart ROM/Monitor ROM 10.5

The System Monitor 10.6
Built-In I/O Locations 10.8
Peripheral I/O 10.10
The Joystick Ports 10.11
Peripheral Connector Pinout 10.14
Peripheral Connector Signal Description 10.15
ROM Listings 10.18

CHAPTER 11 SCHEMATIC DIAGRAMS

Annotated Schematic Diagrams 11.1

CHAPTER 12 DISK SUBSYSTEM

Theory Of Operation 12.1
Disk Conditioning Circuit 12.1
Analog Card 12.4

SECTION II. SERVICING INFORMATION

CHAPTER 13 TESTING & TROUBLESHOOTING

Apple /// Final Test Procedure 13.1
16 Sector Disk /// Final Test (1000T) 13.9
Apple /// Troubleshooting (Module Level) 13.11
5 Volt Memory Board Ram Troubleshooting Procedure 13.16
The Apple /// Troubleshooting Flowchart (Component) 13.28

CHAPTER 14 PARTS LAYOUT AND PARTS LIST

Apple /// IC Parts by Location 14.1
Apple /// Indented Bill of Materials 14.4

CHAPTER 15 WIRE LIST

Wire List 15.1

CHAPTER 16 MODULE REPLACEMENT PROCEDURES & ASSEMBLY DRAWINGS

Apple /// Module Replacement Procedures 16.1
Apple /// Dealer Service Diagnostics Reference 16.25
Apple /// Assembly Drawings 16.32

CHAPTER 17 GENERAL APPENDIX

Apple /// System Overview 17.1
Apple /// System Monitor 17.3
Apple /// Logic Signal Source 17.5
Main Logic Board Circuit Function Areas 17.9
How to Read Prom (Rom) Logic Expressions 17.10
Prom (ROM) Logic Expressions 17.11
Ascii Conversion Tables 17.19

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LIST OF TABLES & ILLUSTRATIONS

AIII System Block Diagram (Illustration) 1.2
AIII System Block Diagram - Detailed (Illustration) 1.3
System Functional Block Diagram 1.5
The 12 Volt Memory Board (128K Configuration) 1.6
The 5 Volt Memory Board (128K Configuration) 1.7
The Apple /// Main Logic Board (Module) 1.8
The Apple /// Detailed System Functional Block Diagram1.9
The Apple /// Memory Map 2.2
Simplified Memory Address Block Diagram 2.3
Block Diagram Memory Address Logic 2.5
RAS/CAS Decode Logic Block Diagram 2.7
Indirect Addressing (Listing) 2.8
Memory & Memory Addressing Appendix 2.12
    Apple /// Memory Map 2.13
    Memory Map Space Allocations 2.17
    Address Logic Truth Table 2.18
    The Apple /// Memory Board (12V) 2.19
    The Apple /// Memory Board (5V) 2.20
    The 5 Volt Memory Board (256K) 2.21
    How to READ PROM (ROM) Logic Expressions 2.22
    RAM Logic Expression 2.23-2.28
    MPU Registers 2.29
Block Diagram of the 6522 VIA 3.2
Addressing 6522 VIA Internal Register 3.2
VIA FFDX Internal Register Summary 3.11
VIA FFEX Internal Register Summary 3.14
VIA Appendices 3.18
The ACIA Block Diagram 4.2
ACIA Control Register 4.11
ACIA Command Register 4.11
ACIA Status Register 4.12
ACIA Pin Configuration 4.12
Main Clock 14Mhz Circuit 5.2
Frequency Divider Circuit 5.2
A/// System Timing Diagrams 5.3-5.6
1 to 2 Mhz Gearshift 5.8
Video State Counter 5.8
Video Scan Decode ROM 5.9
Video Appendix 6.9
    Apple /// Video Logic Block Diagram 6.10
    Hires Mode Page 1, B/W, 280 X 192 6.11
    Hires Mode Page 2, B/W, 280 X 192 6.12
    280 X 192 Color Hires Mode Page 1 6.13
    280 X 192 Color Hires Mode Page 2 6.14
    Super Hires Mode Page 1 6.15
    Super Hires Mode Page 2 6.16
    Ahires Test Page 1 6.17

    Ahires Test Page 2 6.18
    Color Bar & Gray Scale Test 6.19
    Apple][Text Mode Page 1 6.20
    Apple][Text Mode Page 2 6.21
    Sara 40 Column Text Mode Test 6.22
    Sara 80 Column Text Mode Test 6.23
    Video Mode Truth Tables 6.24
    Video Circuit Schematic 6.25
    Video Output types 6.26
    Video Output Type (Circuit diagrams) 6.27
    Video ROM Logic Expressions 6.29
    Video ROM Circuit truth table representation 6.30
    Color Video Connector Description 6.31
I/O System Timing Diagram 7.4
Peripheral Connector Pinout 7.7
Peripheral Connector Signal Description 7.8
Pin Signal Assignment 8.9
Keys & Associated ASCII Codes 8.10
Keyboard Circuit Schematic 8.12
Reset Circuit Schematic 8.13
A/// Power Supply Parts Layout 9.2
Switching Power Supply Block Diagram 9.4
Switching Power Supply Circuit Block Diagram 9.5
A/// Power Supply Schematic Diagram 9.8
A/// Power Supply Parts List 9.10
A/// Power Supply Parts Layout 9.13
A/// Schematic Diagrams 11.1-11.12
Disk Conditioning Circuit Schematic 12.2
Analog Card A/// Circuit Schematic 12.5
A/// Internal Disk Assembly Drawing 12.8
Install Disk Drive Illustration 12.9
Apple /// Disk Enables 12.10
Main Logic Board IC Designators 14.3
Apple /// Logic Signal Source 17.5
Main Logic Board Circuit Function Areas 17.9
How to Read Prom (Rom) Logic Expressions 17.10
Prom (ROM) Logic Expressions 17.11
Ascii Conversion Tables 17.19

INTRODUCTION

GENERAL DESCRIPTION

The Apple /// is a personal computer for the professional. It has the capabilities to run very involved programs since it can have up to 256K of RAM. The overall unit has been designed to incorporate the best features and options that make it a complete personal computer. The Apple][emulation mode allows users to run most Apple][software. However, minor modifications may be required for some Apple][programs or other peripheral devices.

The base system has a full ASCII keyboard which includes a 13-key numeric key pad with two special function keys. There are four cursor control keys. The A/// has two special repeat features: 1) each key repeats when held depressed, and 2) a high-speed repeat is activated with the Solid Apple key. It's typewriter style keyboard is sculptured for maximum typing speed and accuracy.

The Apple /// has a built-in disk drive (140K bytes) and controller which is capable of supporting three additional external drives without additional interfacing. One interesting feature is that the two drives may be on at the same time. This increases the disk-to-disk transfer effectiveness. The Apple /// can also be used with "Profile"- Apple's 5 Megabyte hard disk for mass data storage.

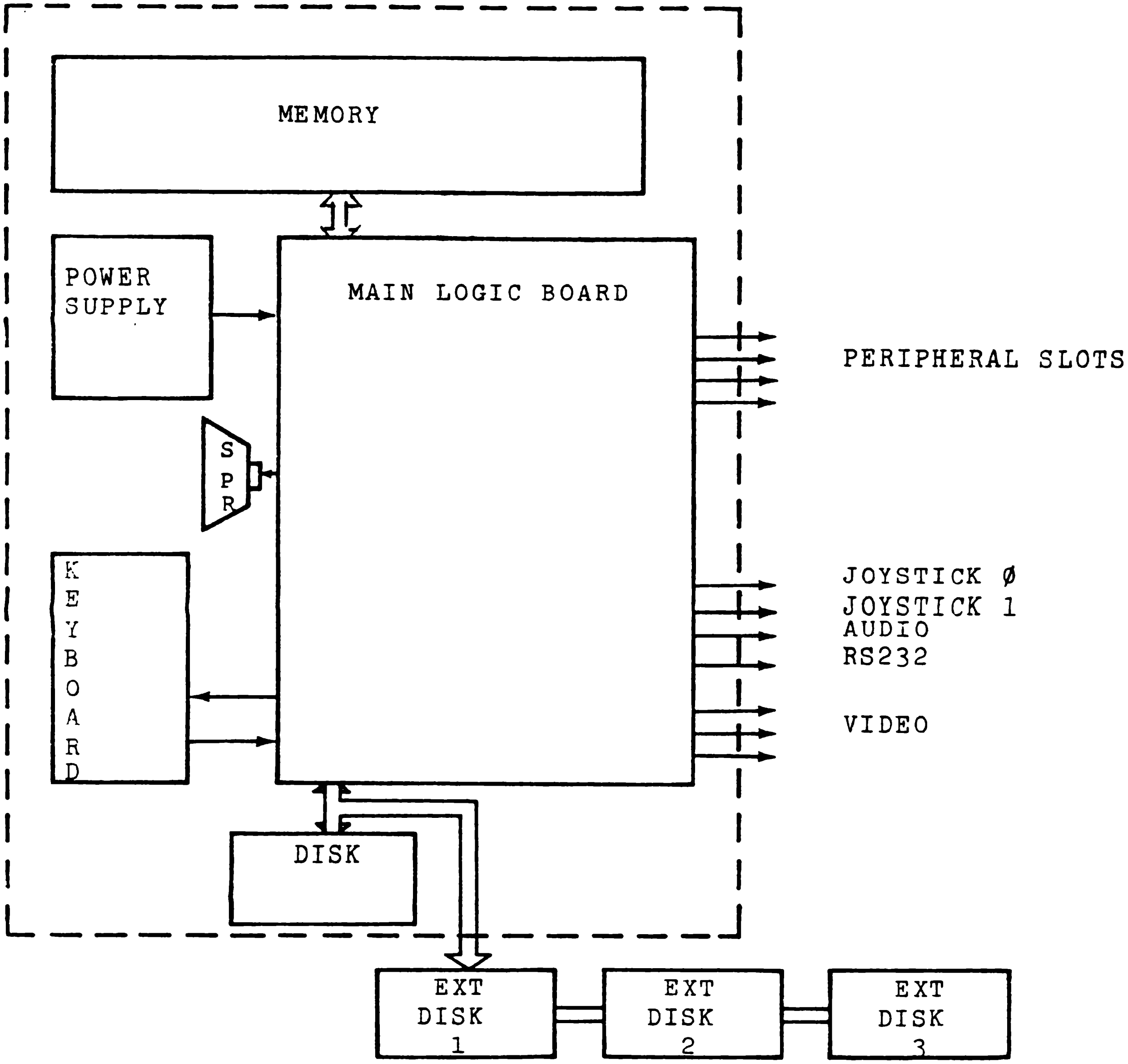
A built-in RS-232 port, located on the back panel, allows you to connect the Apple /// to letter quality printers, high-speed data collection devices, modems, and other serial input/output devices using RS-232-C protrocol. The A/// has two joystick ports for games, sophisticated cursor control, or silentype operation.

The Apple /// has 8 different modes of video operation. B/W Text in 40 and 80 column, a 40 column 16 color text mode (where the foreground and background of each character can be defined). The Apple][graphics modes are duplicated and there are three more graphics modes: a super black and white Hi-Res, 16 color Hi-Res, and 16 color medium resolution graphics. The eigth mode is actually a utilizatin of the color text mode where the user defines the character image and builds video images with these "character sets". Since the video character generator is RAM, not ROM, as in the Apple][, it provides the user with the capability of defining character sets to display whatever the user wants. Three video outputs are provided at the back panel; these are black and white, NTSC color composite, and RGB video for exceptional color purity and resolution.

The Apple ///'s Central Processing Unit (CPU) can be "interrupted" by peripheral devices whenever they require CPU control. Alternatively the CPU can poll the devices to determine which needs attention, thereby minimizing the software required for peripheral control.

There are more features in the Apple /// such as, a built-in clock/calender, a hardware beeper to simplify programming, a six-level D/A converter for more

A III SYSTEM BLOCK DIAGRAM



A III SYSTEM BLOCK DIAGRAM

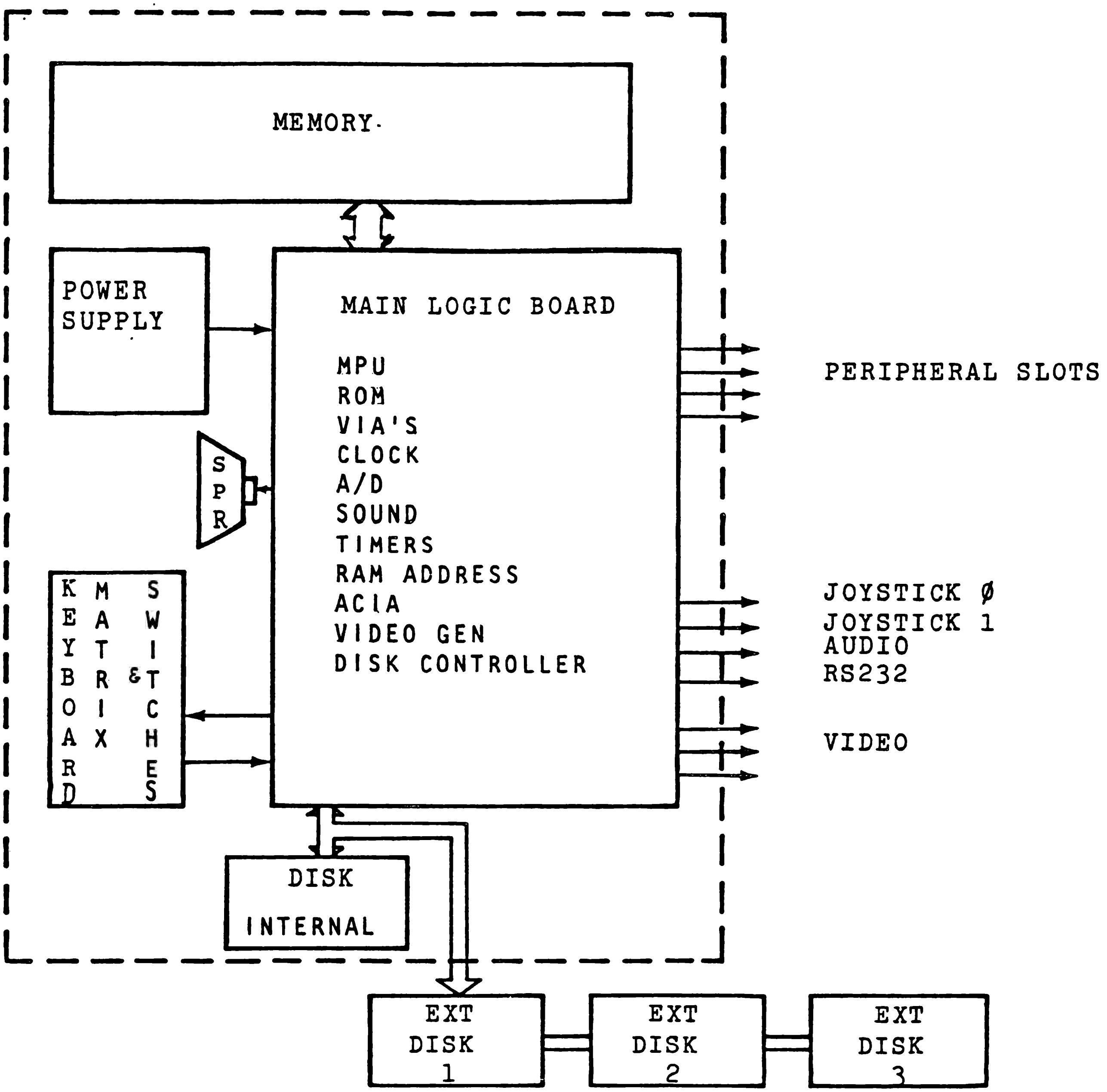


FIG 1.1

DEFINITIONS

MPU - MICROPROCESSOR
ROM - READ ONLY MEMORY
VIA - VERSATILE INTERFACE ADAPTER: A SPECIAL PURPOSE PROCESSOR
ACIA - ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER PROVIDES RS232 COMMUNICATIONS CAPABILITY.
A/D - ANALOG TO DIGITAL CONVERTER

complex tone generation, and the duplication of the speaker function of the Apple][.

As you can see there are many onboard features that would fully load an Apple][, yet the Apple /// has four expansion slots for additional user interfacing. As you read this document and learn how it works, you will appreciate its capabilities, design, and usefulness.

SIMPLIFIED FUNCTIONAL DESCRIPTION

The Apple /// is not an easy machine to understand. It has been designed to emulate the Apple][and has done many operations in a different manner, while adding many enhancements which contribute to its complexity. To understand the system structure it is best to start building functional blocks and gain an understanding of each separately, and then comprehensively.

There are five major parts (modules) to the Apple ///. These parts are:

1) Main Logic PCB - this board functions primarily as a processor and device controller. Many functions are integrated into the board, including the disk controller.

2) Memory PCB - this board stores data/programs temporarily (until power is removed).

3) Keyboard PCB - this is the primary input device provided to the user.

4) Disk Drive - Mass storage device for storing data.

5) Power Supply - provides the voltages and regulation required to keep everything else working.

THE MAIN LOGIC BOARD

The Main Logic Board is easily identified by its large size and mass quantities of integrated circuits (IC's).

Referring to the block diagram of Figure 1.1 we encounter the microprocessor (MPU), Boot/Monitor ROM, address decode/select circuitry, the Versatile Interface (VIA) containing the bank switch register and the sound register, the VIA containing the environmental and zero page registers, the Asynchronous Communications Interface Adapter (ACIA), analog to digital circuit (joystick inputs), the expansion I/O slots, disk controller, keyboard encoder, video generator, RAM, RAM address circuits, and the system and video timing circuits. Whooo, now you see why it's so big!

Figure 1.1 shows the Apple /// in it's simplest form and presents its expanded I/O capability. On the other hand, the System Functional Block Diagram displays the system in more detail and presents a sophisticated system using some highly unique designs. Some definitions have been provided for some of the terms used in the block diagram.

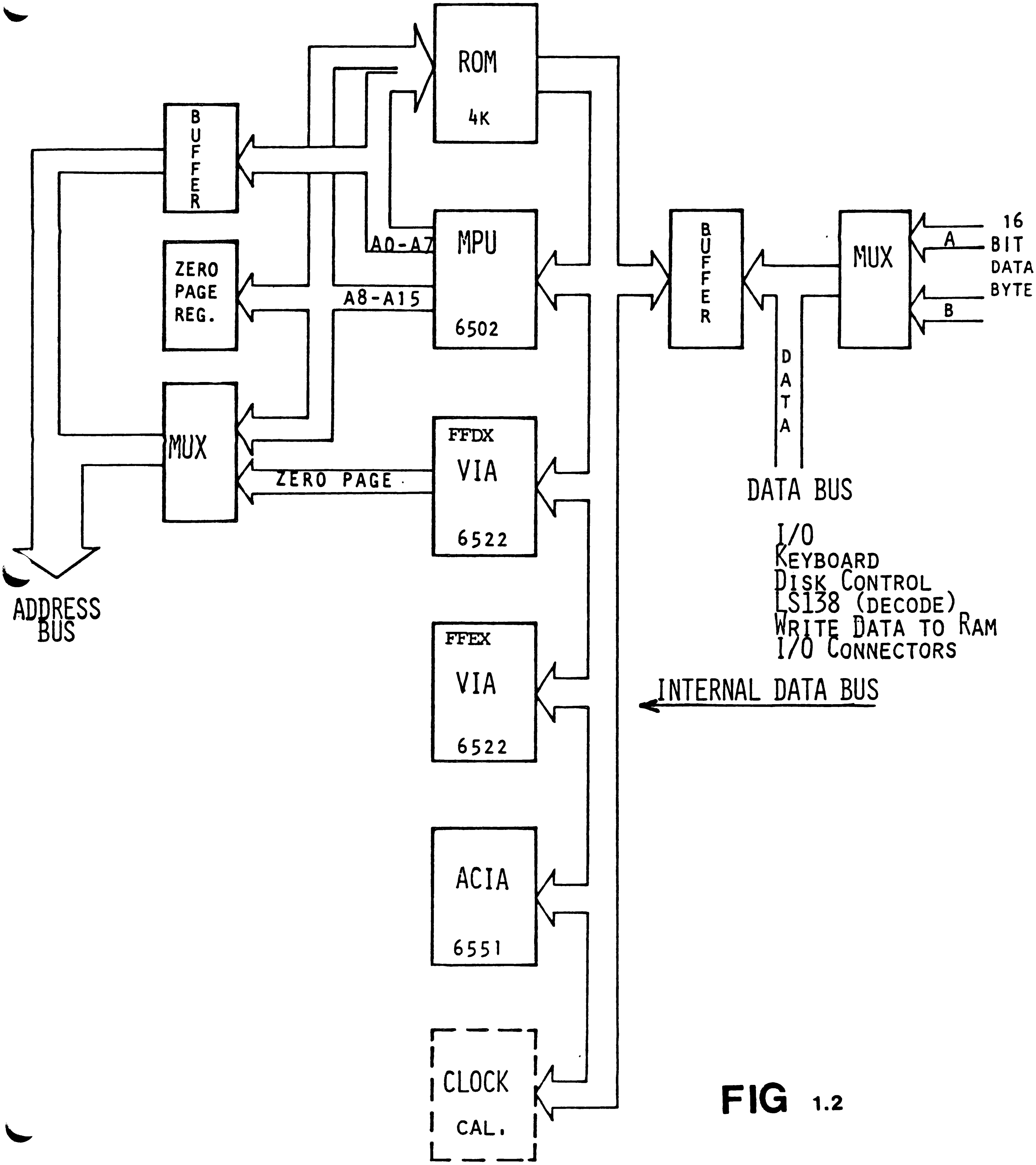

ROM
4K
BUFFER
ZERO PAGE REG.
MPU
6502
A0-A7
A8-A15
MUX
FFDX
VIA
6522
ZERO PAGE
ADDRESS BUS
FFEX
VIA
6522
ACIA
6551
CLOCK
CAL.
BUFFER
MUX
A
B
16 BIT DATA BYTE
DATA
DATA BUS
I/O
KEYBOARD
DISK CONTROL
LS138 (DECODE)
WRITE DATA TO RAM
I/O CONNECTORS
INTERNAL DATA BUS

FIG 1.2

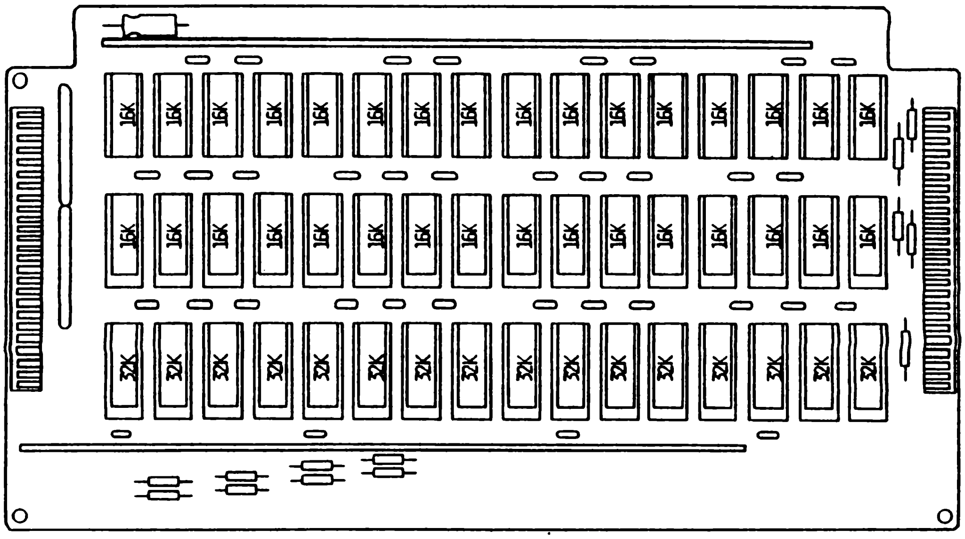
It is best to think of the Apple /// processor as more than just the MPU chip. The processor/controller is actually comprised of many components. The most significant of these are the MPU and the two VIA's. Because of the system's complexity and memory size, the MPU must have extended addressing. Extended addressing is accomplished thru bank switches, environmental register, and a zero page register.

The Apple /// system is interrupt driven. In order to efficienctly use processing time, only those devices that allow programs access to the processor are serviced. In fact the processor can even totally mask (disable) the reset key.

THE MEMORY BOARD

The other PCB in the Apple /// is the memory board. It is mounted on the Main Logic Board by two rows of pin connectors. There are two distinct types of memory boards. The early memory board version is commonly refered to as the 12V Memory Board. Below is an illustration of this board.

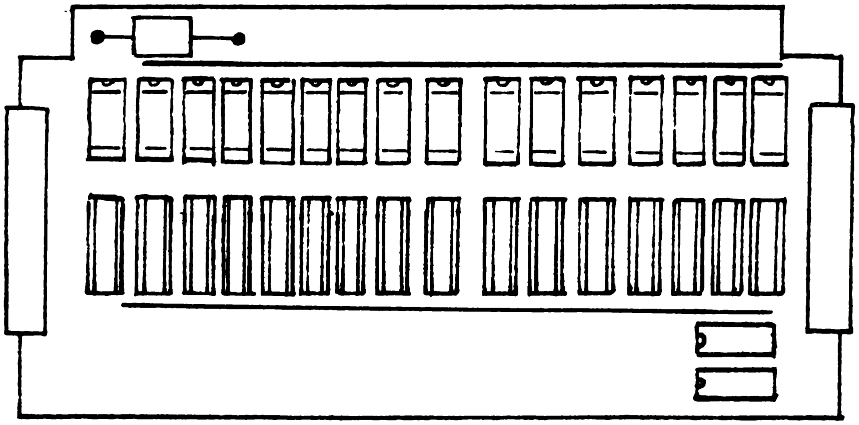
THE 12 VOLT MEMORY BOARD (128K CONFIGURATION)



With the correct Main Logic Board configuration, this board can have up to 128K RAM (without modification). The board uses 16K and 32K RAM chips.

The latest memory board version is called the 5 Volt Memory Board. This board, illustrated in the accompanying pages, can be configured for 128K or 256K RAM. The 5 Volt Memory Board, however, requires the correct Main Logic Board configuration.

THE 5 VOLT MEMORY BOARD (128K CONFIGURATION)



THE KEYBOARD PCB

This has to be one of the nicest keyboards around. The sculptured keys are a delight to touch. The Apple /// does not have an on board keyboard encoder - the keyboard encoder is on the Main Logic Board. The keyboard is basically a matrix of switches. The keyboard is connected by means of a 26 pin ribbon cable to the Main Logic Board.

THE DISK DRIVE

The disk drive is similiar to the Disk][. The major difference between the Disk][and the Apple /// drive are the door, the bezel, and the Analog Card. Disk switch detection circuitry has been added to the Disk /// Analog Card. Through daisey-chaining you can have up to three (3) external disk drives.

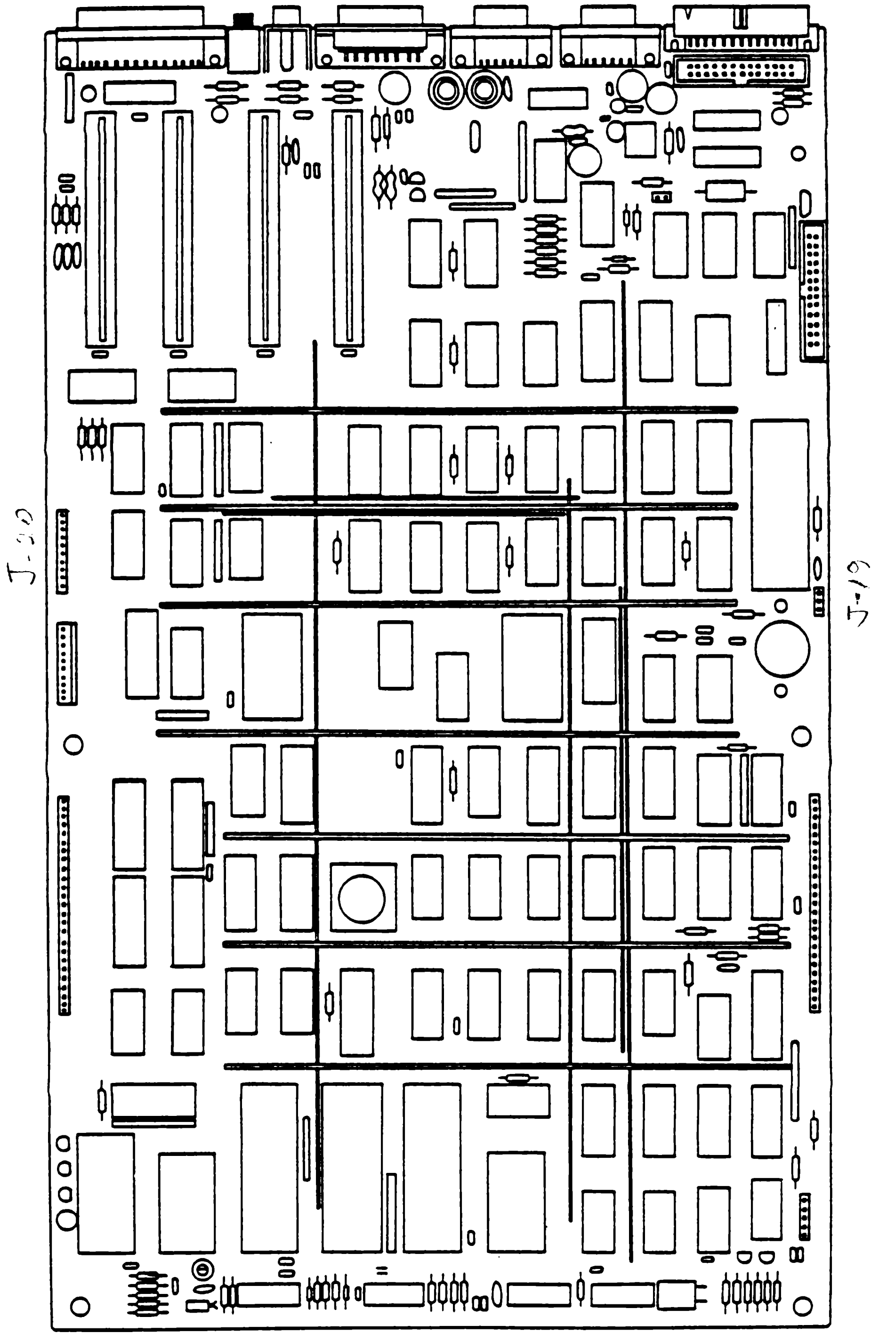
THE APPLE /// POWER SUPPLY

The power supply, accessible from the bottom of the Apple ///, is housed in the casting. It is a "switching type" power supply that supplies the following voltages:

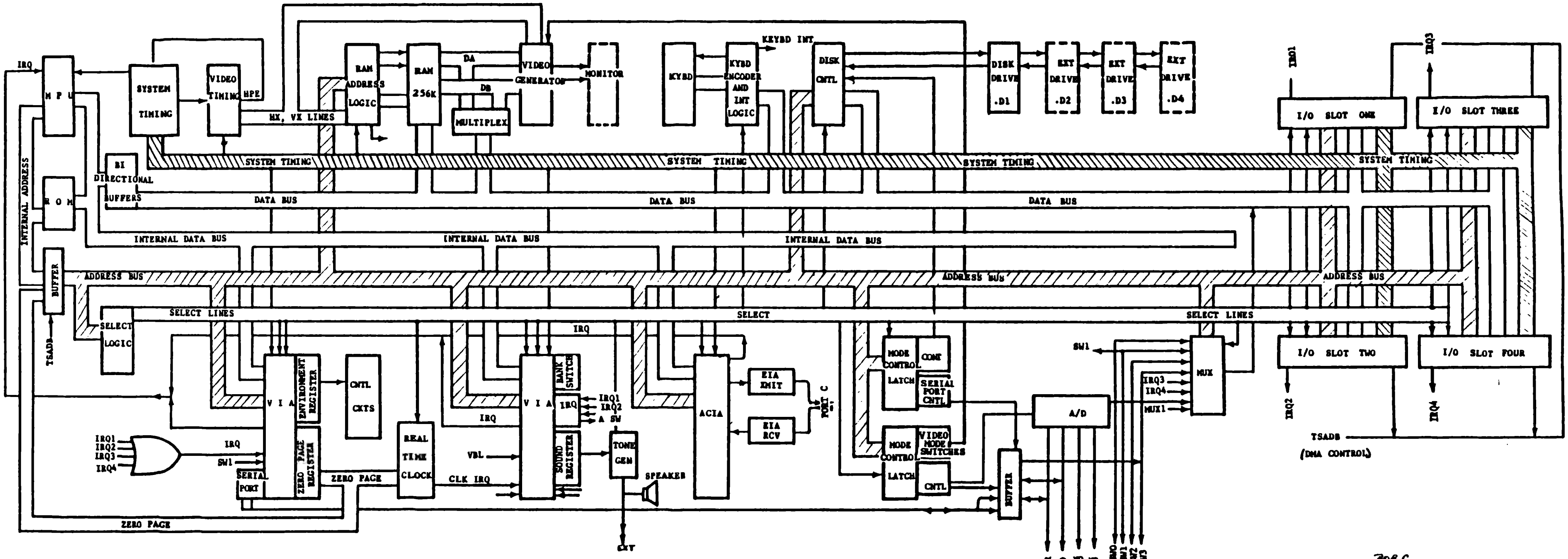
- +5.0 VDC
- +11.8 VDC
- -5.0 VDC
- -12.0 VDC

yet, it consumes less power than a 100 Watt light bulb. The power supply also has several protection features, ie. overvoltage protection.

Now that we have taken a tour of the contents of the Apple /// let us begin to learn the inner workings.



THE APPLE /// MAIN LOGIC BOARD (MODULE)


IRQ
M P U
SYSTEM TIMING
VIDEO TIMING
HPE
HX, VX LINES
RAM ADDRESS LOGIC
RAM 256K
DA
DB
MULTIPLEX
VIDEO GENERATOR
MONITOR
KYBD
KYBD ENCODER AND INT LOGIC
KEYBD INT
DISK CNTL
DISK DRIVE .D1
EXT DRIVE .D2
EXT DRIVE .D3
EXT DRIVE .D4
IRQ1
IRQ3
I/O SLOT ONE
I/O SLOT THREE
INTERNAL ADDRESS
R O M
BI DIRECTIONAL BUFFERS
SYSTEM TIMING
DATA BUS
INTERNAL DATA BUS
BUFFER
ADDRESS BUS
SELECT LINES
SELECT
TSADB
SELECT LOGIC
V I A
ENVIRONMENT REGISTER
CNTL CKTS
IRQ1
IRQ2
IRQ3
IRQ4
IRQ
SW1
SERIAL PORT
ZERO PAGE REGISTER
ZERO PAGE
REAL TIME CLOCK
CLK IRQ
VBL
BANK SWITCH
IRQ
A SW
SOUND REGISTER
TONE GEN
SPEAKER
EXT
ACIA
EIA XMIT
EIA RCV
PORT C
MODE CONTROL
LATCH
CONT
SERIAL PORT CNTL
VIDEO MODE SWITCHES
CNTL
BUFFER
A/D
SW1
MUX
MUX1
SER
XCO
YO
XO
SW0
SW1
SW2
SW3
I/O SLOT TWO
I/O SLOT FOUR
IRQ2
IRQ4
TSADB
(DMA CONTROL)

BOB C.
10/82

MEMORY & MEMORY ADDRESSING

INTRODUCTION TO THE APPLE /// MEMORY

In looking at the Apple /// and its memory we are immediately posed with the problem of how the 6502 processor can handle 128K of RAM, 4K of ROM, and a heavy array of internal and external I/O devices. The Apple /// does indeed do just that, and, further, has the hardware capability of controlling an additional 128K of memory (for a total of 256K).

This "magic" is accomplished by Bank Switching technology. At any one time, the processor can directly address 65K locations. With the addition of the Bank Switch Register, an extended addressing register, the program can call up different banks of 32K RAM space. With other software switches, ROM and all I/O locations can be replaced with RAM. [See Figure 2.1]

The first 8K of memory, from locations 0000 to 1FFF, are fixed. The 32K memory from locations locations 2000 to 9FFF are electrically switchable. The Apple /// can choose any of 15 banks to place in this area at any one time. The maximum amount of storage on the Apple ///, therefore, is equal to 15 Banks x 32K per bank + 32K fixed storage. By comparison, a 128K system would have three banks, a 256K system would have seven, etc.

In addition, the area in the fixed bank from location C000 to CFFF can be switched from RAM memory to I/O space for the slots. The area from F000 to FFFF is also switchable. When the machine is turned on, this area is ROM containing the startup program. This program runs a quick system check then loads SOS in from the internal drive. SOS then switches this area back to RAM.

The extended addressing mode allows any two adjacent banks, N and N+1, to be addressed as a contiguous 64K RAM space. Addresses 0000 to 7FFF are mapped into bank N while addresses 8000 to FFFF are mapped into bank N+1.

The Apple /// has the capability for variable Zero Page locations and Alternate Stack locations. All these features give the Apple /// great flexibility. They also provide means for very large application programs, or applications that need large amounts of RAM space for data crunching.

SIMPLIFIED MEMORY LOGIC

If we simplify the memory and memory address logic we get three basic elements:

- o the processor
- o the RAM address circuits
- o the RAM array

Apple /// Memory Map

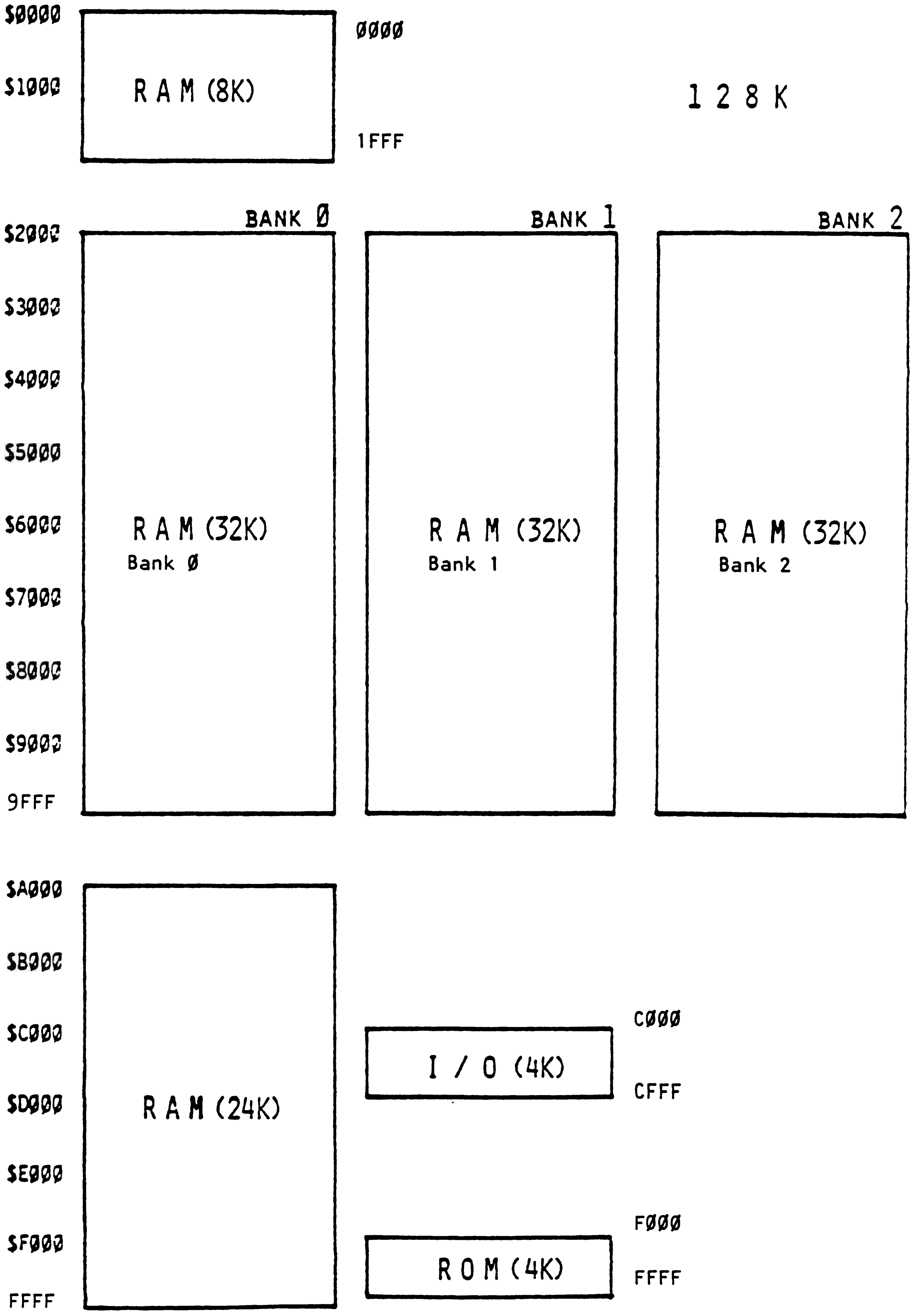


FIG 2.1

SIMPLIFIED MEMORY ADDRESS BLOCK DIAGRAM

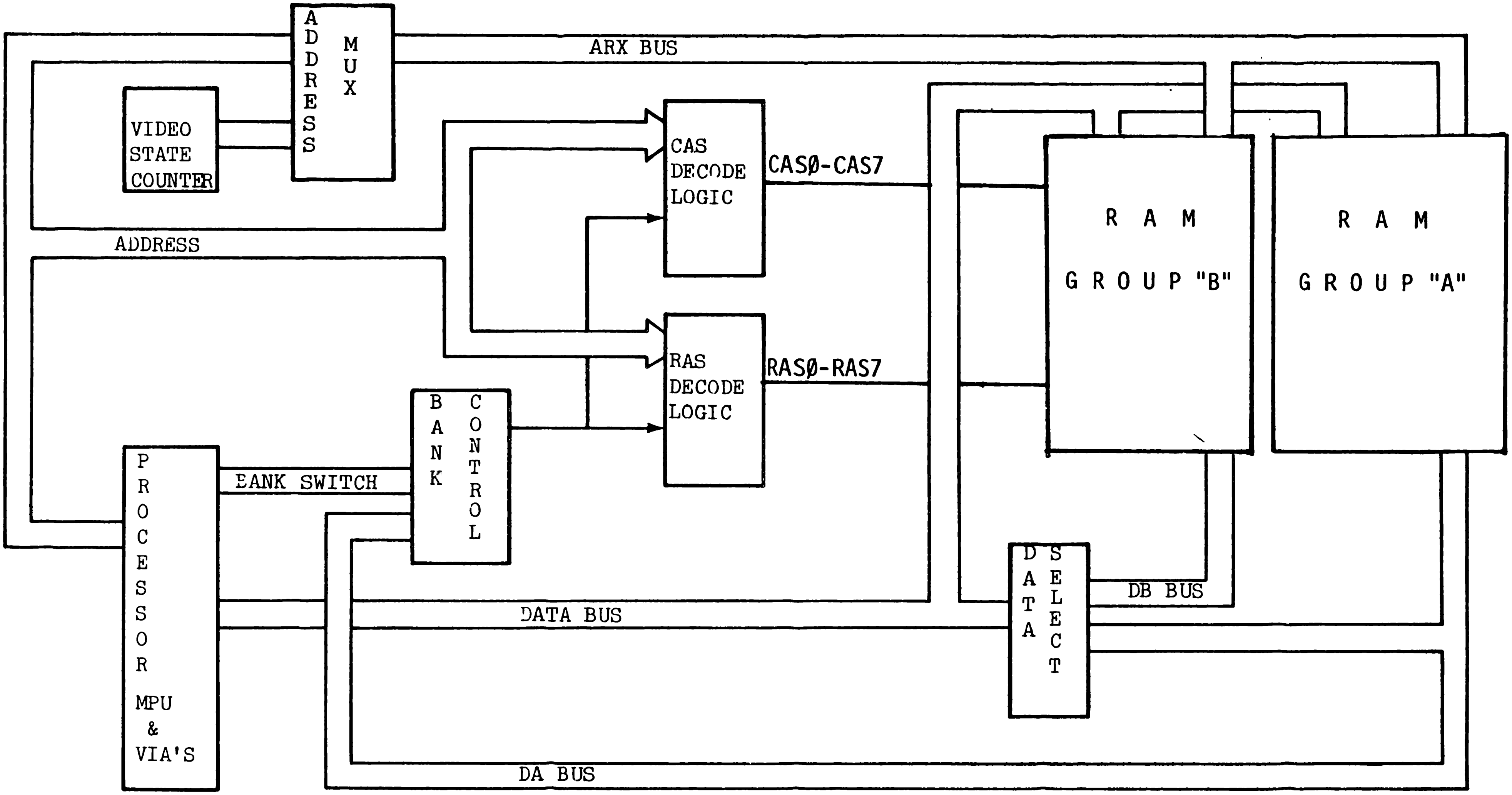


FIG 2.2

In this discussion, the processor is more than just the microprocessor chip; it also contains various external registers and control ROMs which enable the extended addressing and bank switch modes. [Refer to Figure 2.2.]

Very simply, the processor presents an address for memory cycle, which is multiplexed into the address bus, ARX, and is decoded to develop the RAS (Row Address Strobe) and CAS (Column Address Strobe) to the RAM array (RAM group A & B). The direction of the data is controlled by Read/Write*. The selection of which RAM group is being gated to the data bus is controlled by the CAS decode circuits.

The display is memory mapped, the Screen time-shares the RAM on the opposite phase of the processor clock. Both the screen and the processor are running at a 1MHz rate, which means that the RAM is running at a 2MHz rate. One new feature of the Apple /// is that the processor is able to make use of the other "phase" while the screen is off. In other words, any time the screen is off, the processor may run at a full 2MHz rate.

MEMORY ADDRESSING: BLOCK FLOW

As more detail is added, it is possible to see the basic elements of the complete memory system (For now, we are not considering any to the hardware or I/O).

- In the memory addressing logic of Figure 2.3, the processor now shows the MPU and the two registers for expanded addressing capacity:
  - the bank address register
  - zero page register
- The address circuit is comprised of two sections:
  - the address multiplexer
  - the RAS/CAS decoder
- The RAM array is expanded to show the eight RAMs.

It should be noted that this diagram depicts a 128K system (with a 12V Memory board), and that each of the RAMs shown actually represents eight RAM chips, one for each bit. Each RAM contains 16K bytes. The dotted lines indicate the row of chips that contain the 32K RAM chips. These are actually two 16K RAMs which reside on the one IC package.

THE PROCESSOR

The MPU is isolated from the rest of the memory by various buffers, muxes, and registers. The mux switches in the Zero Page register whenever the MPU is attempting to reference the zero page.

BLOCK DIAGRAM MEMORY ADDRESS LOGIC

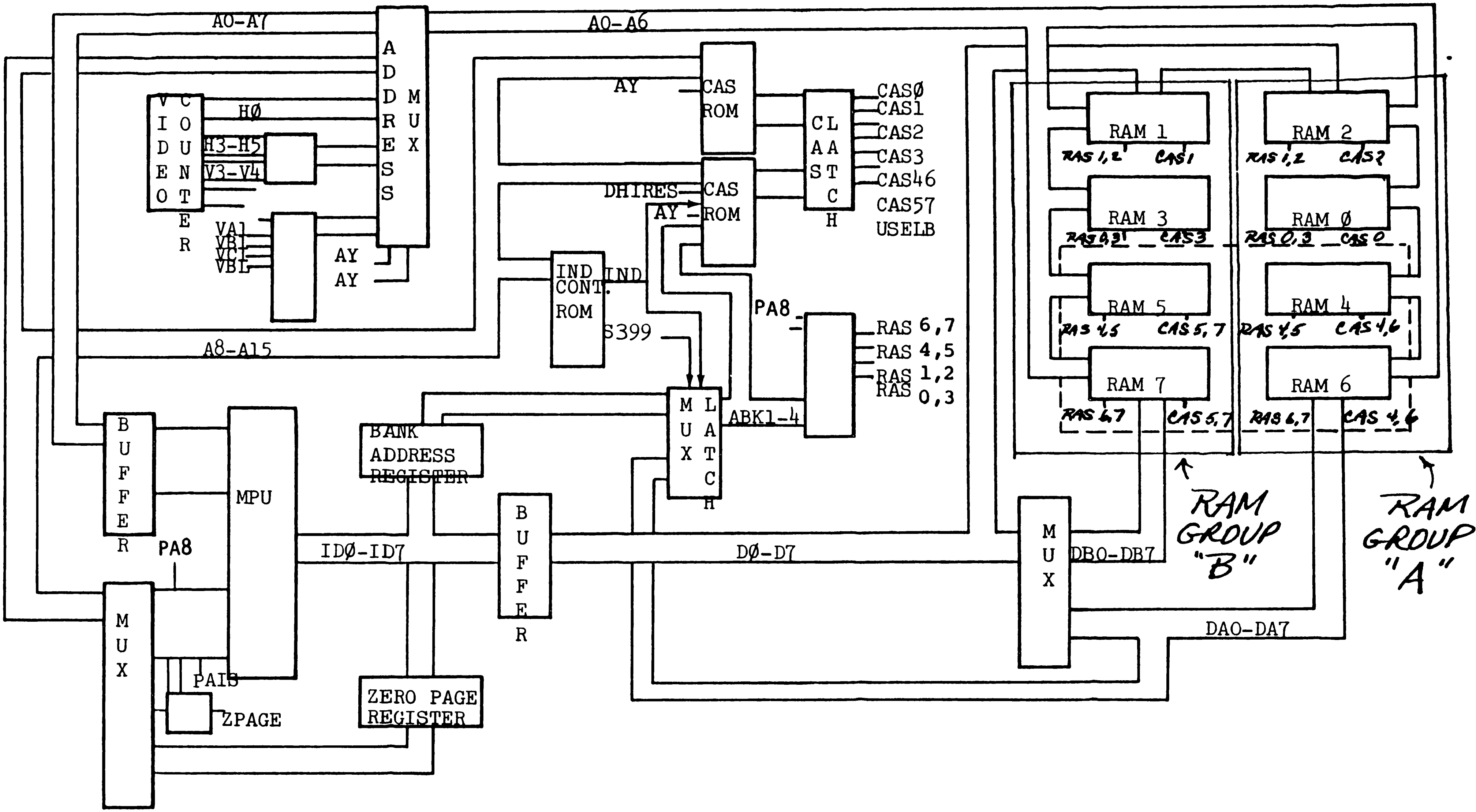


FIG 2.3

- The register may contain the true zero page or may be set to any of 255 other values, under program control.

- The zero page register resides in the VIA and is accessed at FFD0. (On the Main Logic Board this is the VIA at location B6.)

- The Bank Register is located in the other VIA and is accessed at FFEF (at location B5). Zero page selection is independent of bank selection.

MEMORY ADDRESS MULTIPLEXER

The Memory Address Mux provides the four sets of addresses to the RAM array. They are:

- MPU RAS
- Video RAS
- MPU CAS
- Video CAS

These are time multiplexed by the four states determined by AX* line which is held at a steady state, allowing the processor full access to the RAM.

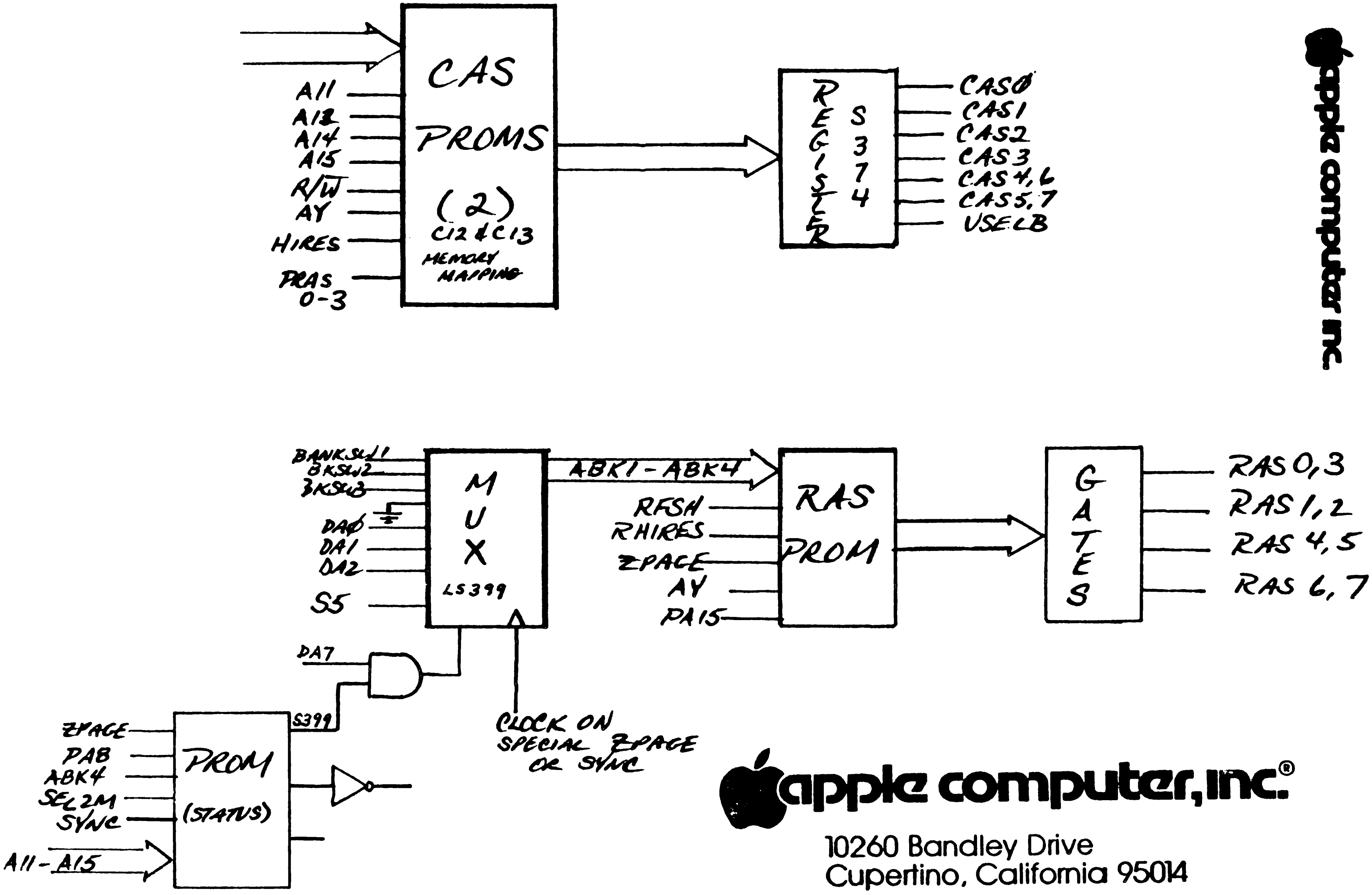
The Video addresses are much the same as in the Apple][. There is a minor difference in the Summing Circuit, but the technique of condensing undisplayed addresses is the same. There is an additional consideration in the Apple ///, which has a feature requiring additional control of the Video lines. This new feature is called slow scrolling of the screen.

Slow scrolling is accomplished in the Video Mux ROM by the arithmetic offset of the VA, VB, and VC lines. This offset causes characters to be fetched from memory in advance of where the screen actually thinks it is. The character array on the screen shifts up the number of dots determined by the binary weight of the VBX lines. The processor, by monitoring the Vertical Blanking, can then step the VBX lines and scroll the screen by moving in new lines at the bottom, removing the top line, and placing it at the bottom, thus rolling the display.

RAS/CAS DECODE

The RAS/CAS decode circuit is made from four ROMs, a latch, and a latching mux. The basic inputs to the circuit are:

- the Address Bus
- the Bank Switches
- the Zero Page Select



apple computer, inc.®
10260 Bandley Drive
Cupertino, California 95014

RAS/CAS DECODE LOGIC

BLOCK DIAGRAM

FIG 2.4

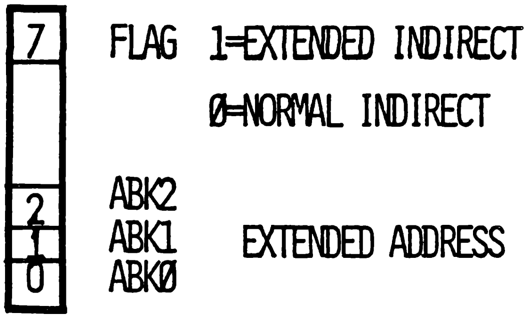
INDIRECT ADDRESSING

```
LDA (Z PAGE), Y                     Y REG = 0

2000 B1      LDA (Z PAGE), Y OP CODE
2001 05      ZPAGE ADDRESS
0005 CD      (1ST. 8 BIT BYTE) }
                               } PUT TOGETHER TO GET INDIRECT ADDRESS
0006 AB      (2ND. 8 BIT BYTE) }
ABCD         LOAD ACCUMULATOR FROM ABCD
2002         NEXT OP CODE
```

FIG 2.5

IF ZPAGE = 18-1F (IF ZERO PAGE FALLS BETWEEN THE RANGE OF 18-1F)

```
             2000  B1      LDA (ZPAGE). Y OP CODE
             2001  05      ZPAGE ADDRESS
             1805  CD
16-BIT READ  1806  AB      1406  82
             2ABCD         LOAD ACCUMULATOR
             2002          NEXT OP CODE
```



[Refer to Figure 2.4]

Normal or Direct Addressing looks at the address and current bank selection, and enables the appropriate array of 64K RAM. This Direct Addressing always uses RAM 0 and RAM 3. Bank switches determine which of the RAM pairs is used for the other 32K of RAM.

It should be noted that on any read cycle, one RAS line and two CAS lines are selected. In this way, two bytes are always presented to the video circuits and the data selector. During a write cycle only one of each is selected.

The dual byte read usually provides only the information for the new video modes, but there is a new special memory fetch cycle built into the hardware. It is a special extended Indirect Addressing scheme which places the entire memory in virtual access.

By using Indirect Addressing through the zero page containing the 16 bit address, an instruction can address any of the 64K bytes contained in the bank pair. Thus any of the 32K byte RAM banks can be paired with any of their neighbors to form a 64K byte virtual address space.

If, during a zero page reference the zero page register has a value between $18 and $1F ($ means hexadecimal), a special Indirect Mode is called up. This mode looks at the sister fetched data byte on the RAM address bus and also looks at the high order bit. See Figures 2.5 and 2.6.

This special Indirect Mode is determined by the zero page register (X page = Z page EOR $0C) If the bit is zero, the mode is not actualized and the reference continues in a normal manner in the presently selected bank arrangement. But if the High Order Bit (DA7) is high, the bank control mux latch switches to the state determined by the state of the DA0-DA2 lines. This allows the program to have access to another array of special zero pages.

When the system is in this special extended Indirect Mode, the I/O and LSI are totally disabled and the RAM is enabled to the data bus.

ALTERNATE STACK

Alternate Stack, the new feature of the Apple ///, is not shown in the block diagrams. One of the bits of the Environmental Register (from one of the VIAs) is the Alternate Stack Switch. If the Alternate Stack Switch is selected, the stack associated with that zero page is either the one after the zero page, if the zero page reference is even, or the one previous if the reference is odd (i.e., if zero page is 2B then the stack is located in 2C; if the zero page is 31 then the stack is in 30).

OTHER BANK SWITCHING

Earlier it was mentioned that the processor can access RAM associated with the addresses that are normally with I/O, ROM, and other circuits. Looking again at the Environmental Register, there are several switches that enable or disable I/O, ROM, and other circuit address decoding. If these switches are selected to disable their associated function, the control ROM, which develops the enable for the RAM data selector, senses the fact that no hardware is being selected and allows RAM data to be read on the bus. No other special enables are needed since RAM is always read for every address presented. It should be noted that a special RAM write enable is used to prevent inadvertant writing into the RAM space associated with the hardware while the hardware is enabled.

MEMORY & MEMORY ADDRESSING APPENDIX

The attached figures and illustrations are provided for your reference. Little or no explanation has been provided.

This Appendix contains:

- THE APPLE /// MEMORY MAP
- MEMORY MAP SPACE ALLOCATIONS
- ADDRESS LOGIC TRUTH TABLE
- 128K 12V MEMORY BOARD: PHYSICAL MEMORY
- THE 5V MEMORY BOARD: PHYSICAL MEMORY
- ADDRESSING LOGIC EXPRESSIONS
- MPU REGISTERS

APPLE /// MEMORY MAP

SOS MEMORY ALLOCATION

Location	Assignment
0000-1FFF	SOS and Interpreter Workspace
2000-9FFF	Bank 0 Graphics Page 1 and 2
2000-9FFF	Bank 1 Program
2000-9FFF	Bank 2 Driver and Interprter
A000-BFFF	Interpreter
C000-CFFF	I/O or SOS Kernal (Bank switchable to RAM)
D000-EFFF	SOS Kernal
F000-FFFF	Boot ROM OR SOS Kernal

ADDRESS ASSIGNMENT

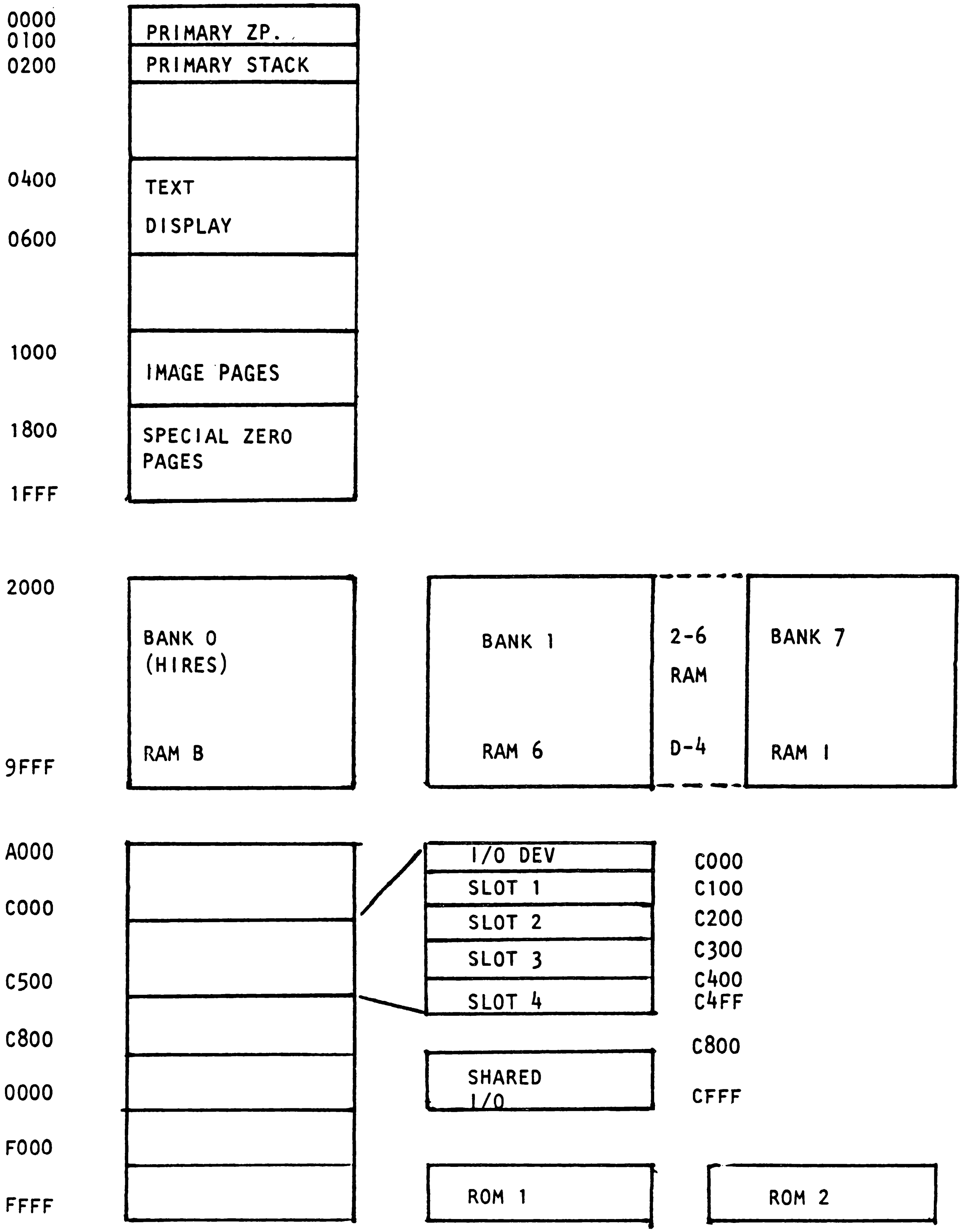
ADDRESS (HEX)	ASSIGNMENT (FUNCTION)
0000-00FF	Zero Page
0100-01FF	Stack
0200-02FF	Input Buffer
0300-03FF	Open
0400-07FF	Lo-Res Display (Primary) and text
0800-0BFF	Lo-Res Display (Secondary) and text
0C00-0FFF	Open-Reserved for system space
1000-1FFF	Open
2000-3FFF	Hi-Res Pg1 (Primary) switchable to RAM
4000-5FFF	Hi-Res Pg1 (Secondary) switchable to RAM
6000-7FFF	Hi-Res Pg2 (Primary) switchable to RAM
8000-9FFF	Hi-Res Pg2 (Secondary) switchable to RAM
A000-BFFF	Open
C000-C07F	System I/O
C000	Keyboard "A" bus data
C001-C007	Same as 0000 but not used
C008	Keyboard "B" bus data
C009-C00F	Same as C008 but not used
C010	Keyboard reset
C011-C02F	Not used in Apple III
C030	Toggle the speaker like in A-11
C031-C03F	Same as C030 but not used
C040-C040	Sound hardware beeper
C04E	Character Ram Disable
C04F	Character Ram Enable
C050	Clear Text Mode
C051	Set Text Mode
C052	Clear Mix Mode
C053	Set Mix Mode
C054	Clear PG2 Mode

C055	Set PG2 Mode	
C056	Clear HIRES Mode	
C057	Set HIRES Mode	
C058	Clear EMSOT PDL0	
C059	SET ENSOT PDL0	
C05A	Clear PDL2 (A/D Addr 2)	
C05B	Set PDL2	
C05C	Clear PDLEN (A/D Ramp Start)	
C05D	Set PDLEN	
C05E	Clear AXC0 (A/D Addr 1)	
C05F	Set AXC0	
C060,C068	Read SW0	
C061,C069	Read SW1/MGNSW	
C062,C06A	Read SW2	
C063,C06B	Read SW3/SC0	
C064,C06C	Read IRQ3	
C065,C06D	Read IRQ4	
C066,C06E	Read PDLOT (A/D Ramp Stop)	
C067,C06F	Read MUXI (PRAS Control)	
C070	Access Real Time Clock	
C071-C07F	Sames as C070 but not used	
C080-C0FF	I/O Scot Device Enable	
C08F		
C09X	NDevice Select 1	
C0AX	NDevice Select 2	
C0BX	NDevice Select 3	
C0CX	NDevice Select 4	
C0D0	Clear DS A0	A0,A1=0,0=no select
C0D1	Set DS A0	1,0=Ena 1 Exit
C0D2	Clear DS A1	0,1=Ena 2 Exit
C0D3	Set DS A1	1,1=Ena 3 Exit
C0D4	Clear Enable 1 Int	
C0D5	Set Enable 1 Int	
C0D6	Clear Side 2	
C0D7	Set Side 2	
C0D8	Clear SCR	
C0D9	Set SCR	
C0DA	Clear ENCWRT	
C0DB	Set ENCWRT	
C0DC	Clear ENSEL	
C0DD	Set ENSEL	
C0DE	Clear ENSIC	
C0DF	Set ENSIO	
C0E0	Clear DPH0 (also VAL)	
C0E1	Set DPH0	
C0E2	Clear DPH1 (also VBI)	
C0E3	Set DPH1	
C0E4	Clear DPH2 (also VCI)	
C0E5	Set DPH2	
C0E6	Clear DPH3	
C0E7	Set DPH3	
C0E8	Disable Motor Drive (strt 2 sec to) C0E9 Enable Motor Drive	
C0EA	Enable Ext	
C0EB	Enable Int	

C0EC	Clear Q6 Note:Q6,Q7 control read
C0ED	Set Q6 write, and sense write
C0EE	Clear Q7 protect
C0EF	Set Q7
C0F0r	6551 Rec Data Reg
C0F0w	6551 Xmit Data Reg
C0F1r	6551 Status Reg
C0F1w	6551 Program reset
C0F2r/w6551	Command Reg
C0F3r/w6551	Control Reg
CIXX	NIO Select 1
C100-C7FF	I/O Slot individual ROM Space
C100	Slot 1 Firmware
C1FF	
C2XX	NIO Select 2
C200-C2FF	Slot 2 Firmware
C3XX	NIO Select 3
C300-C3FF	Slot 3 Firmware
C3FF	
C4XX	NIO Select 4
C400-C4FF	Slot 4 Firmware
C500-C7FF	Run Space only
C800-CFFF	Expansion Rom Firmware
D000-DFFF	Open (system software)
E000	Bank switchable between Rom and Ram
FFCX	Always Ram
FFD0	Port B VIA-73 "Zero Page Reg"
FFD1	Port A VIA-73
FFD2	DDR B VIA-73
FFD3	DDR A VIA-73
FFD4	Timer 1 low Latch (w)/Counter (r)
FFD5	Timer 1 High Counter
FFD6	Timer 1 Low Latches
FFD7	Timer 1 High Latches
FFD8	Timer 2 Low Latch (w)/Counter (r)
FFD9	Timer 2 High Counter
FFDA	Shift Register (serial print)
FFDB	Aux Control Reg VIA-73
FFDC	Peripheral Control Register
FFDD	Interrupt Flag Register (73)
FFDE	Interrupt Enable Register (73)
FFDF	ORA/IRA With no handshake
FFE0	Port B (97) (sound and slot NMI)
FFE1	Port A (97) Banksw and IRQ's
FFE2	DDR B (97)
FFE3	DDR A (97)
FFE4	Timer 1 Low Latch/Counter
FFE5	Timer 1 High Counter
FFE6	Timer 1 Low Latches
FFE7	Timer 1 High Latches
FFE8	Timer 2 Low Latch/Counter
FFE9	Timer 2 High Counter
FFEA	Shift Register (97)
FFEB	Aux Control Register (97)

FFEC	Peripheral Control Register (97)
FFED	Interrupt Flag Register (97)
FFEE	Interrupt Enable Register (97)
FFEF	ORA/IRA with no handshake
FFE0	Ram/Rom Bank
FFF1	E/O Bank Switch
FFF2	2 MHz/MHZ Mode Switch
FFF3	Hires Bank Switch
FFF4	Screen Enable
FFF5	Display Modes
FFF6	Zero Page Register
FFF7	Interrupt Control
FFFF	

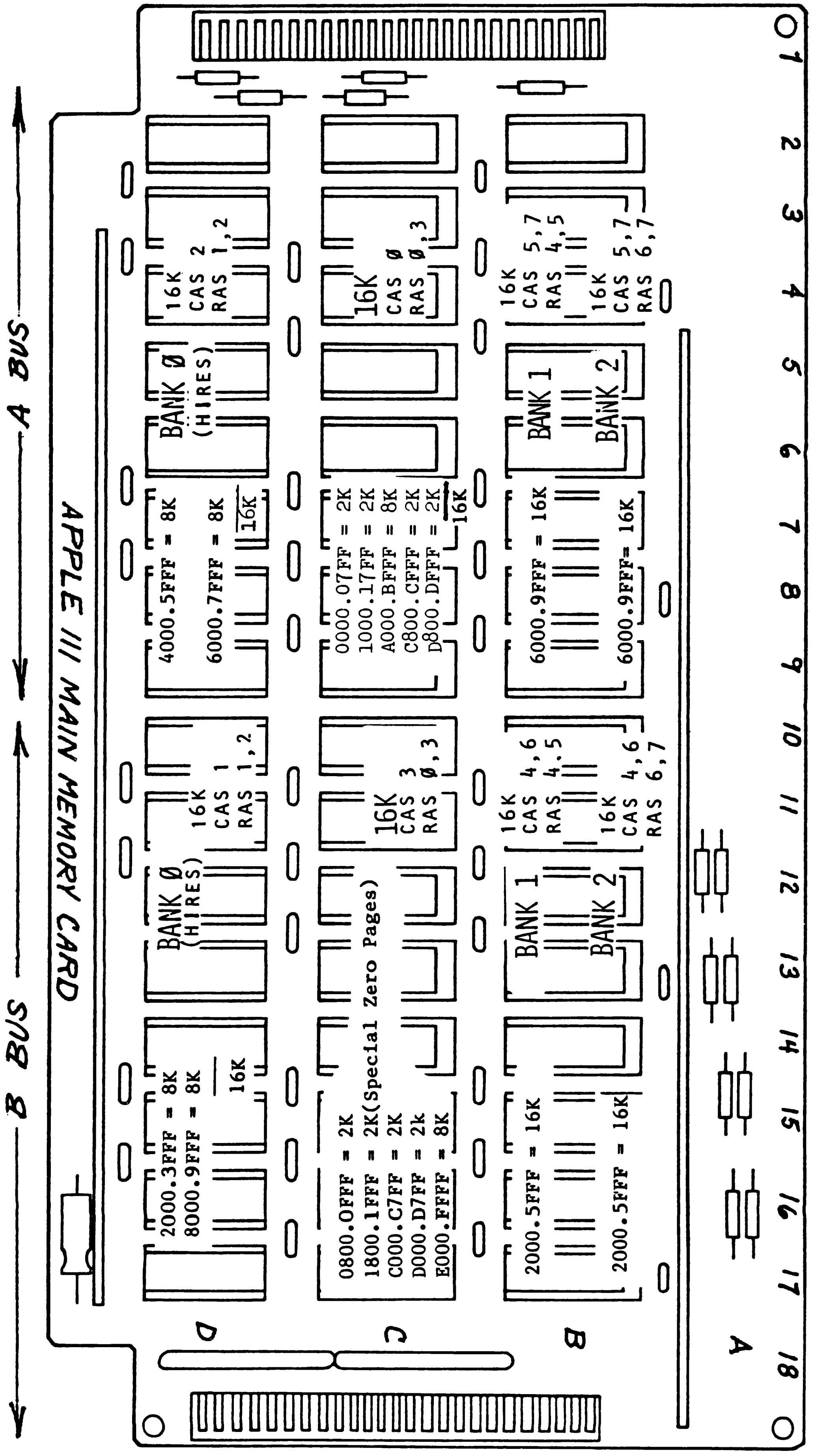
MEMORY MAP SPACE ALLOCATIONS

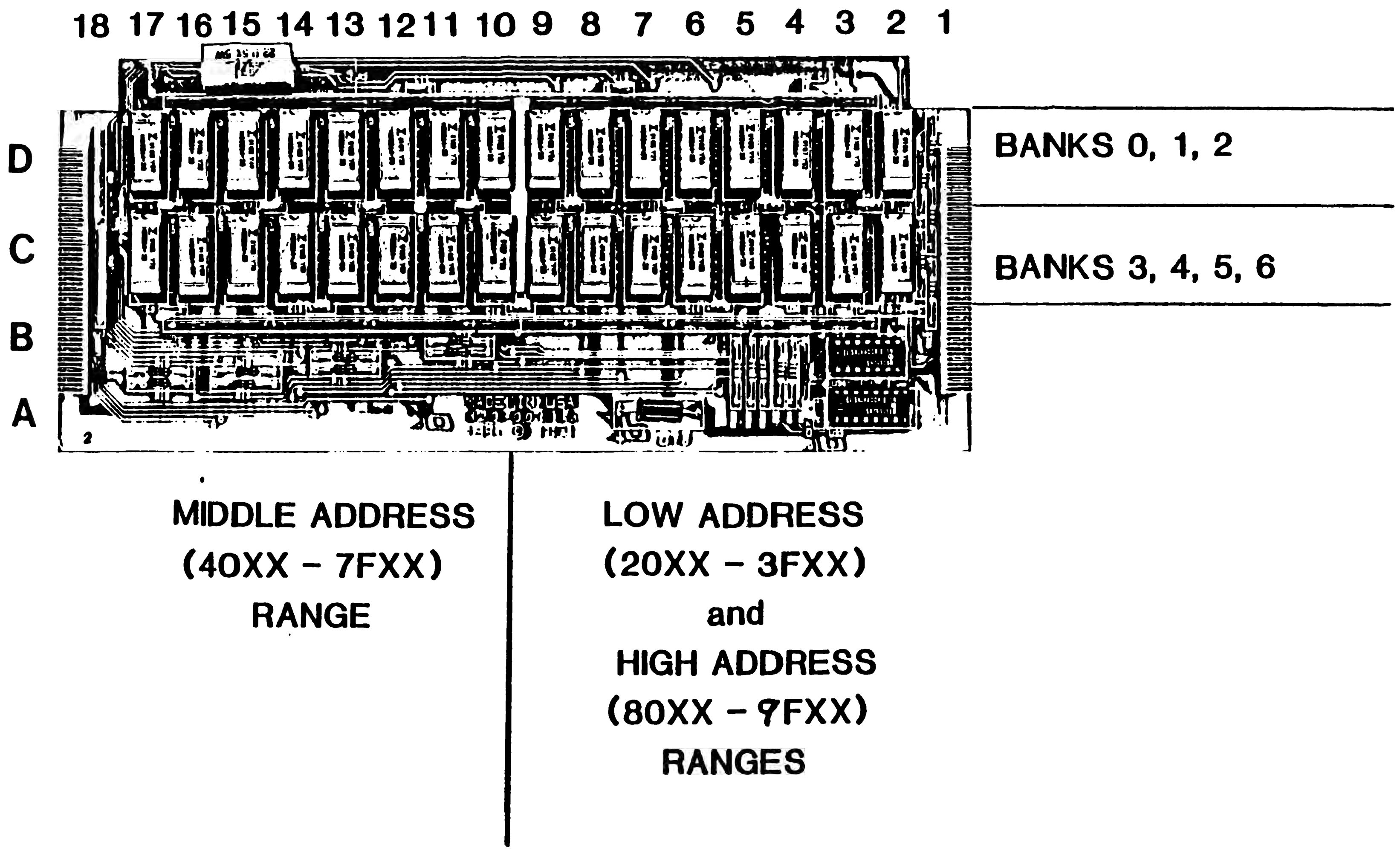


** FFCX, FFDX, FFEX ARE ENVIRONMENT ADDRESSES

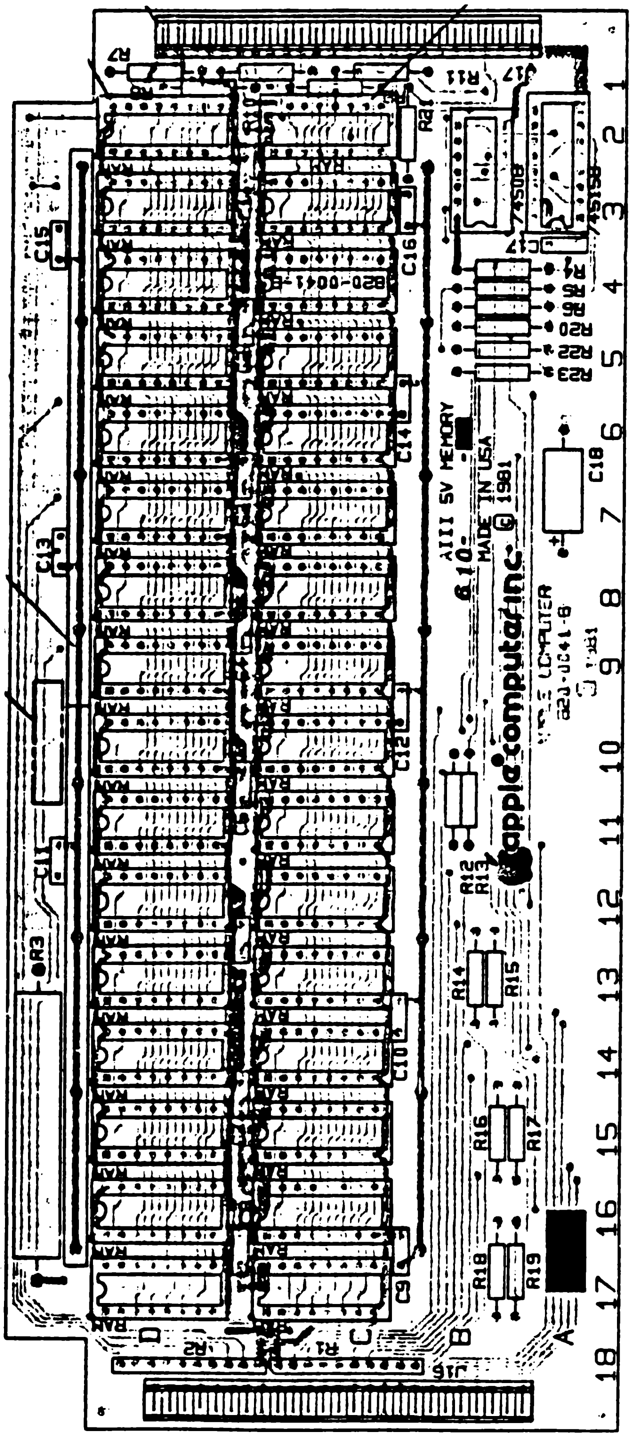
$\overline{AX}$	$\overline{AY}$	AR0	AR1	AR2	AR3	AR4	AR5	AR6	STATE FUNCTION
0	0	A0	A1	A2	A3	A4	A5	A7	MPU GEN RAS ADD.
0	1	H0	H1	H2	Σ1	Σ2	Σ3	V0	VIDEO GEN RAS ADD
1	0	A6	A8	A9	A10 ⊕ $\overline{PCAS0}$	A11 ⊕ $\overline{PCAS0}$	A12	$\overline{PCAS1}$ ⊕ (A15 ⊕ $\overline{PCAS0,3}$)	MPU GEN CAS ADD
1	1	Σ4	V1	$\dot{V}2 \cdot V5$	MUX1	MUX2	MUX3	$\overline{PG2}$	VIDEO GEN CAS ADD

ADDRESS LOGIC TRUTH TABLE


APPLE /// MAIN MEMORY CARD
A BUS
B BUS
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
A
B
C
D
16K CAS 2 RAS 1,2
BANK 0 (HIRES)
4000.5FFF = 8K
6000.7FFF = 8K
16K
16K CAS 1 RAS 1,2
BANK 0 (HIRES)
2000.3FFF = 8K
8000.9FFF = 8K
16K
16K CAS 0 RAS 0,3
0000.07FF = 2K
1000.17FF = 2K
A000.BFFF = 8K
C800.CFFF = 2K
D800.DFFF = 2K
16K
16K CAS 3 RAS 0,3
(Special Zero Pages)
0800.0FFF = 2K
1800.1FFF = 2K(Special Zero Pages)
C000.C7FF = 2K
D000.D7FF = 2k
E000.FFFF = 8K
16K CAS 5,7 RAS 4,5
16K CAS 5,7 RAS 6,7
BANK 1
BANK 2
6000.9FFF = 16K
6000.9FFF= 16K
16K CAS 4,6 RAS 4,5
16K CAS 4,6 RAS 6,7
BANK 1
BANK 2
2000.5FFF = 16K
2000.5FFF = 16K


18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
D
C
B
A
BANKS 0, 1, 2
BANKS 3, 4, 5, 6
MIDDLE ADDRESS (40XX - 7FXX) RANGE
LOW ADDRESS (20XX - 3FXX) and HIGH ADDRESS (80XX - 9FXX) RANGES

THE 5V MEMORY BOARD (256K)



HOW TO READ PROM (ROM) LOGIC EXPRESSIONS

X′ -- The single quote at the end of an expression means that the state of the signal is true when low, or it may represent the inversion of the state of the signal.

* -- Defines a logic AND operation. The expressions on either side of the asterisk is ANDed.

+ -- Defines a logic OR operation. The expression on either side of the asterisk is OR′d.

() -- Defines the boundaries of a logic expression. A new expression is defined by what ever is inside of the brackets.

RULES FOR INTERPRETATION

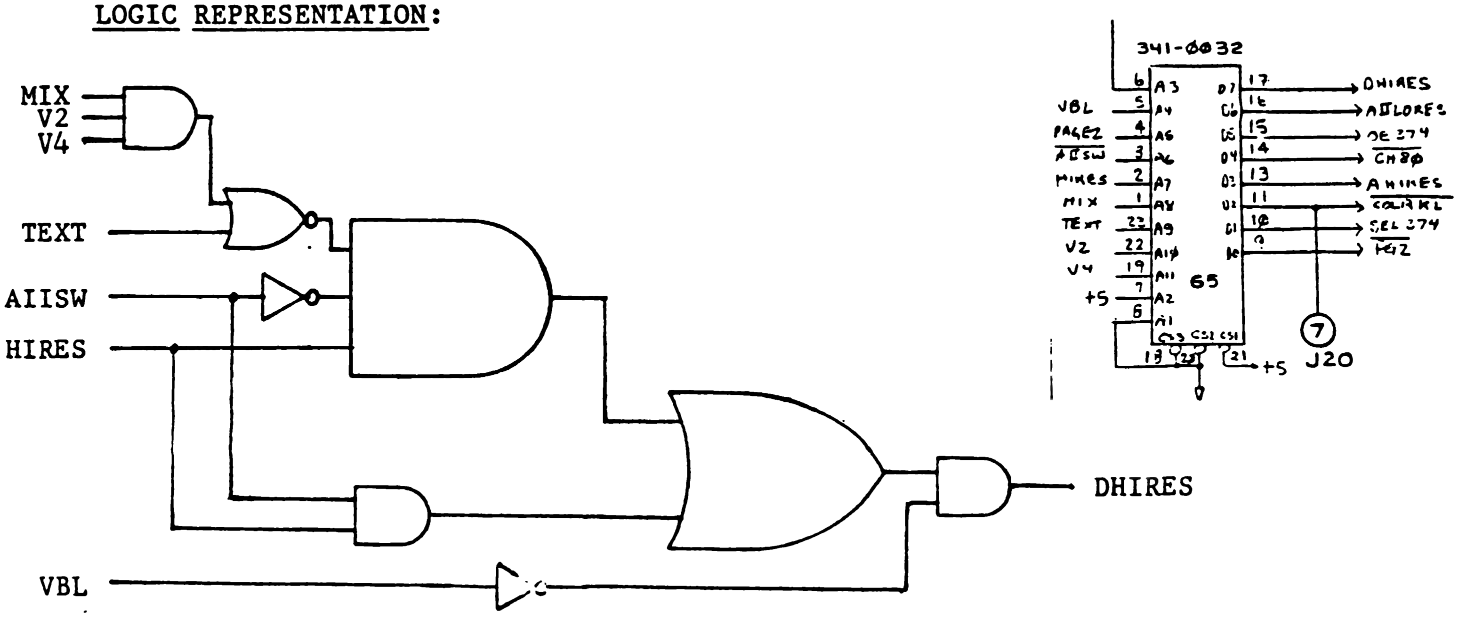
1. Always interpret (transform) the expression within the brackets first.
2. Interpret AND (*) logic operations before OR (+) operations.

EXAMPLE:

Given:	INPUTS:	AIISW′	HIRES	TEXT
		MIX	V2	V4
		VBL		

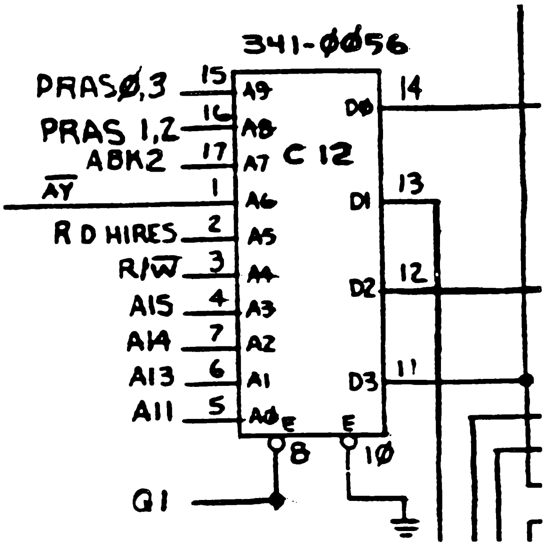
OUTPUT: DHIRES = (AIISW*HIRES*(TEXT+MIX*V2*V4)′+AIISW′*HIRES)*VBL′

LOGIC REPRESENTATION:



A=A11
B=A13
C=A14
D=A15
E=R/WN
F=DHIRES
G=AY'
H=ABK2
I=PRAS1,2
J=PRAS0,3
D0=PCAS0'
D1=PUSELB
D2=PCAS3
D3=PCAS3'

```
PCAS0'=(PRAS0, 3 * (DHIRES' *AY' +AY* (A15'* A14' * A13' *A11' *R/WN' +
      A15' *A14' *A13'* R/WN+A15*A14'*A13' *A11)))'


PUSELB=PRAS0, 3 * (A15' *A14' *A13' *A11 +A15 *A14 *A13' *A11' +A15 *A14
      *A13) +PRAS0, 3 *PRAS1, 2 *(A15' *A14' *A13+A15* A14' *A13') +PRAS0,
      3 *PRAS1,2 '*(A15' *A14' *A13+A15' *A14 *A13') +PRAS0, 3 '* PRAS1, 2
      * (A14' *A13' +A14 *A13) +PRAS0, 3 ' *PRAS1, 2 ' *A14'

PCAS3=PRAS0, 3 * (DHIRES ' *AY ' + AY* (A15' *A14' *A13' *A11 + A15 *A14
     A13' *A11' +A15 *A14 *A13))

PCAS3'=(PRAS0,3 * (DHIRES ' *AY' +AY* (A15' *A14' *A13' *A11+A15 *A14 *A13'
      *A11' +A15* A14* A13)))'
```



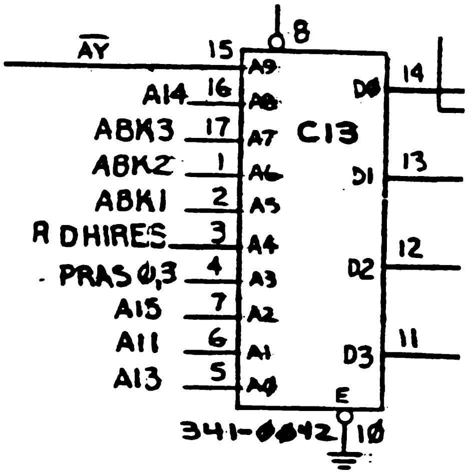
A=A13
B=A11
C=A15
D=PRAS0,3
E=DHIRES
F=ABK1
G=ABK2
H=ABK3
I=A14
J=AY'
D0=PCAS4,7'
D1=PCAS5,6'
D2=PCAS1'
D3=PCAS2

PCAS4,7'= (AY*PRAS0, 3 * (ABK1*ABK2*ABK3'+ABK3* (ABK1' + ABK2'))* (A15' *A14) +AY* PRAS0,3 '* (ABK1' *ABK2*ABK3'*A14+ABK1*ABK2*ABK3'+ABK2' *ABK3+ABK1' *ABK2*ABK3*A15') *(A14' *A13+A14*A13))'

PCAS5,6'= (AY8PRAS0,3 *(ABK1*ABK2*ABK3' +ABK3* (ABK1' +ABK2'))* (A15'*A14' *A13+A15*A14' *A14'*A13') +AY*PRAS0, /3 '*(ABK1'*ABK2*ABK3' *A15+ ABK1*ABK2*ABK3*'+ABK2'*ABK3+ABK1'*ABK2*ABK3*A15') *(A14'*A13'A14* A13))'

PCAS1' = (DHIRES *AY'+AY*PRAS0, 3 * (ABK3' * (ABK1'+ABK2') +ABK1*ABK2*ABK3) * (A15'* A14' *A13+A15*A14' *A13') +AY*PRAS0, 3 '*(ABK2' *ABK3'+ABK1' *ABK2*ABK3'*A15') * (A14'* A13'+A14*A13))'

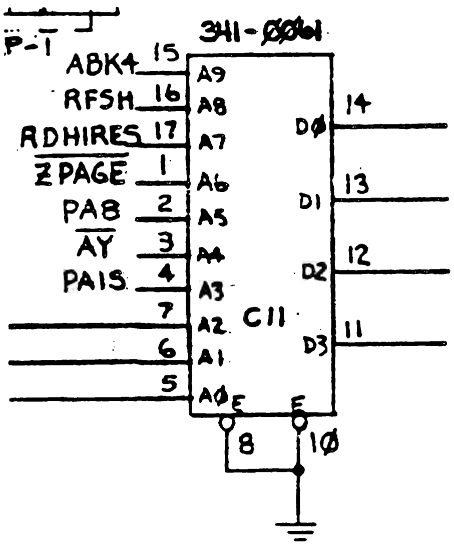
PCAS2' = (DHIRES *AY' +AY*PRAS0,3 *(ABK3'* (ABK1' +ABK2') +ABK1*ABK2*ABK3) *A15'* A14+AY*PRAS0,3 '*(ABK2'*ABK3'+ABK1'*ABK2*ABK3'*A15) *(A14' *A13+A14*A13'))'



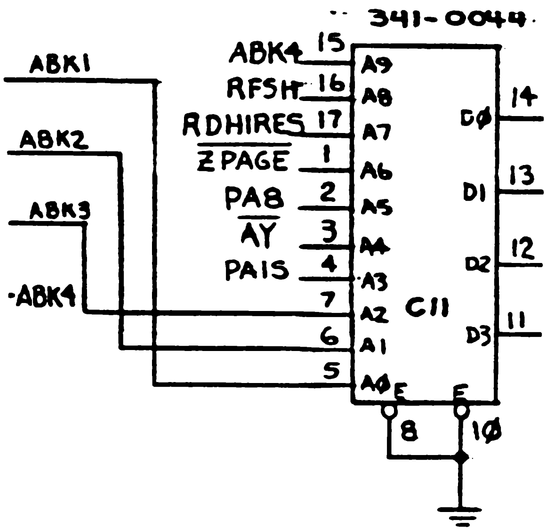
RAS 258

A=ABK1
B=ABK2
C=ABK3
D=PA15
E=AY'
F=PA8
G=ZPAGE'
H=DHIRES
I=RFSH
J=ABK4
D0=PRAS0,3
D1=PRAS1,2
D2=PRAS4,5
D3=PRAS6,7

```
PRAS0,3 = AY'* (DHIRES' +RFSH) + ((ABK4* (ZPAGE*PA8')')'+ABK4* (ZPAGE*PA8)'
          '*ABK1* ABK2*ABK3)*AY PRAS1,2=AY'+AY PRAS4,5=AY'+AY*(ABK4* (ZPAGE*
          PA8')')'*(ABK1*ABK2*ABK3'+ABK1'*ABK2*ABK3' *PA15+ABK1'* ABK2'*PA15'
          +ABK1*ABK2*ABK3)  PRAS6,7 +AY'*DHIRES'+AY* (ABK4*(ZPAGE*PA8')')'*
          (ABK1* (ABK2' +ABK3')) +AY*ABK4* (ZPAGE*PA8')'* (PA15'*ABK1* (ABK2'
          +ABK3') +PA15*ABK1'* (AKB2' + ABK3'))
```



```
RAS.2.TEXT

A-ABK1
B=ABK2
C=ABK3
D=PA14 5
E-AY'
F=PA8
G=ZPAGE
H=DHIRES
I=RFSH
J=ABK4
D0=PRAS0,3
D1-PRAS1,2
D2=PRAS4,5
D3=PRAS6,7

PRAS0, 3 =AY'* (DHIRES'+RFSH) + ((ABK4* (ZPAGE*PA8')') ' +ABK1*ABK2*ABK3)
         *AY

PRAS1,2  =AY'* (DHIRES+RFSH) =AY* (ABK1'* AKB2'*ABK3'* (ABK4* (ZPAGE*PA8')
         '**PA15)'+ABK1*ABK2*ABK3) +AY*ABK3'* (ABK1'* ABK2* ABK4* (ZPAGE*
         PA8') '*PA15+ABK1*ABK2*(ABK4* (ZPAGE*PA8') *PA15)')

PRAS4,5 =RFSH*AY'+AY*ABK2'*ABK3'* (ABK1'*ABK4* (ZPAGE*PA8') 'PA15+ABK1*
        (ABK4* (ZPAGE*PA8') '*PA15)')

PRAS6,7 =RFSH*AY'+AY*ABK3'* (ABK1*?BK2'*ABK4* (ZPAGE*PA8') '*PA15+ABK1'*
        ABK2* (ABK4* (ZPAGE*PA8') '*PA15)')
```

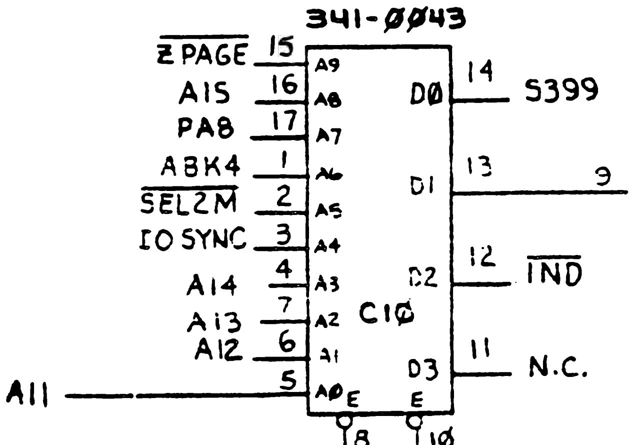


A=A11
B=A12
C=A13
D=A14
E=IOSYNC
F=SEL2M′
G=ABK4
H=PA8
I=15
K=PAGE′
D0=S399
D1=PRDY′
D2=IND′

S399=ZPAGE*PA8′ *A15′ *A14′ *A13′ *A12* A11

PRDY′=IOSYNC *SEL2M *ABK4

IND′= (ABK4* (ZPAGE* PA8′) ′)′



U175 1. TEXT

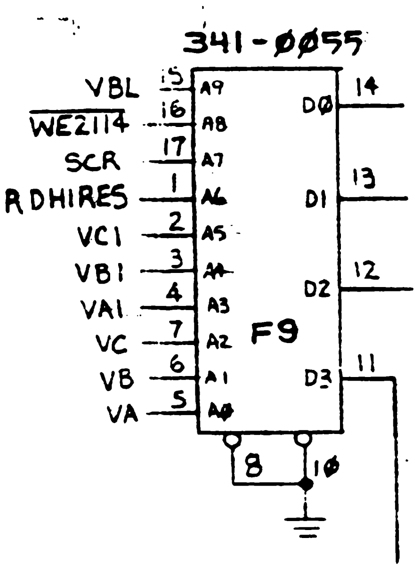
A=VA
B=VB
C=VC
D=VA1
E=VB1
F=VC1
G=DHIRES
H=SCR
I=WE2114'
J=VBL
D0=MUX1
D1=MUX2
D2=MUX3
D3=ENHREG'

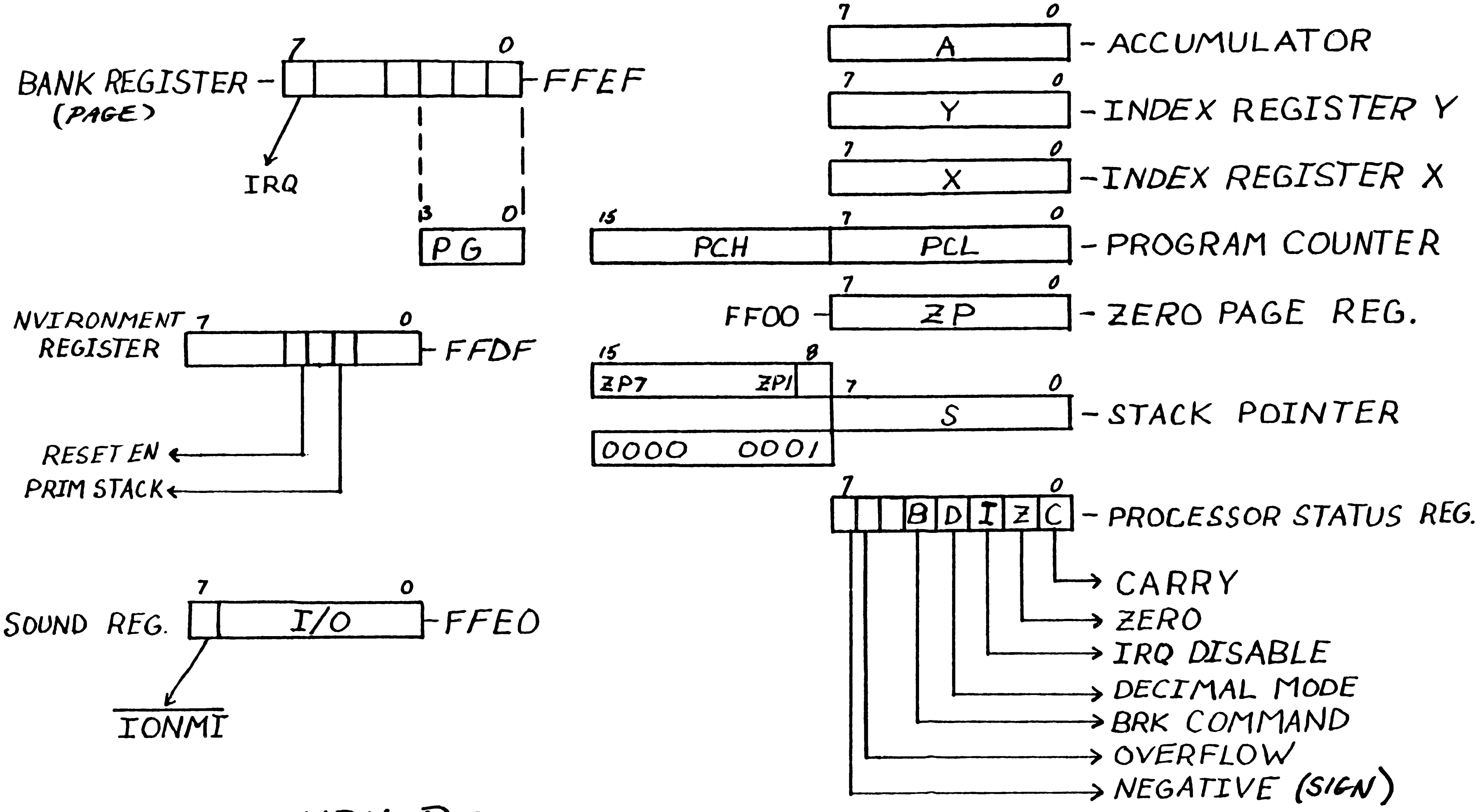
MUX1=(DHIRES' +SCR * (VA* VA1' +VA' *VA1) + SCR' *VA) * (VBL' + WE2114) +VBL * WE2114'

MUX2=DHIRES* (SCR* (VA* VA1* (VB* VB1' +VB'* VB1)'+ (VA* VA1)'* (VB* VB1' +VB * VB1)) +VB* SCR')

MUX3=DHIRES * (SCR* ((VA* VA1* (VB+ VB1) +VB* VB1) * (VC* VC1'+VC'* VC1) '+(VA* VA1* (VB+ VB1) +VB * VB1) '*(VC * VC1)) +VC* SCR')

ENHREG'=DHIRES' *WE2114'





MPU REGISTERS

I/O DEVICE STROBES

0X	KEYBOARD READ
1X	RESET KEYBAORD
2X	N.C .
3X	Speake Toggle
4X	Beeper
5X	Display Regiater
6X	Switch Register
7X	Real Time Clock
8X	N.C.
9X	
AX	Slot 1-4
BX	DEVSEL
CX	
DX	I/O CONTROL REGISTER
EX	DISK REGISTER
FX	ACIA

C0XX

KEYBOARD DATA

0	ASCII0
1	ASCII1
2	ASCII2
3	ASCII3
4	ASCII4
5	ASCII5
6	ASCII6
7	KBO FLAG

C000

KEYBOARD STATUS

0	ANY KEY DOWN
1	SHIFT
2	CONTROL
3	CAPSLOCK
4	APPLE I
5	APPLE II
6	KEYBOARD PRESENT
7	ASCII7

C008

VIA

CA1	SLOT INT.
CA2	SWI/MARGIN INT.
CB1	SERVICE CLOCK
CB2	SERVICE DATE/PDLO

SILENTYPE

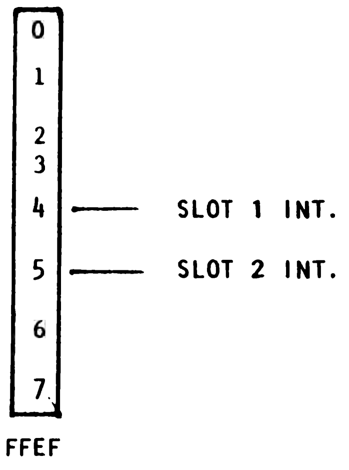
FFDX

VIA

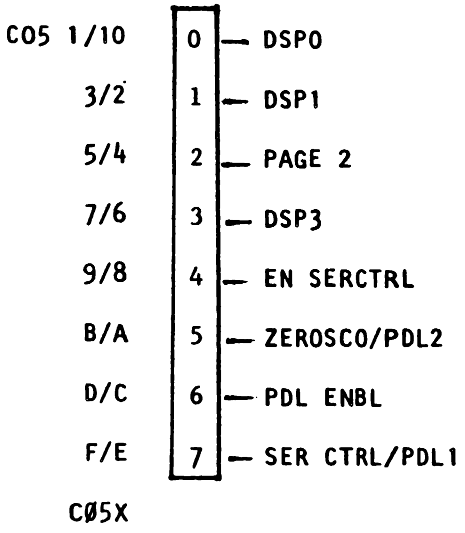
CA1	RT CLOCK INT.
CA2	KEYBOARD UNIT
CB1	VERTICAL BLANKING
CB2	VERTICAL BLANKING

FFEX

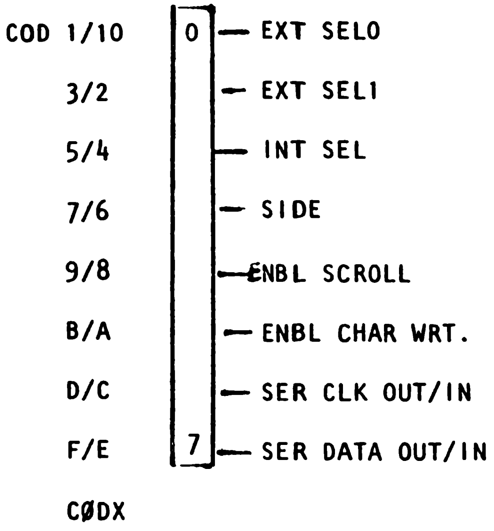
BANK PAGE REGISTER



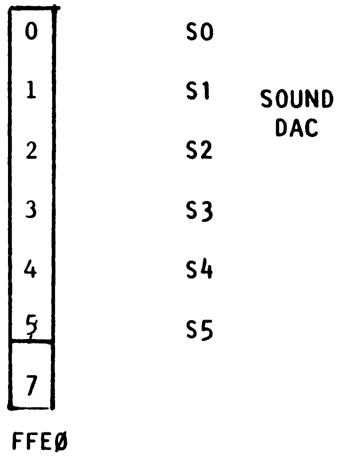
DISPLAY REGISTER



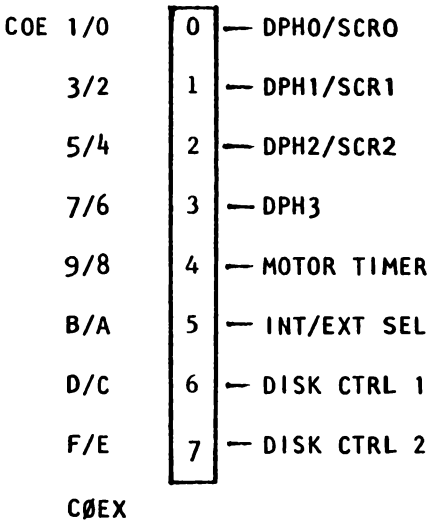
I/O CONTROL REGISTER



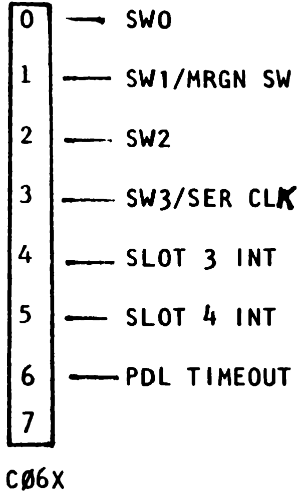
SOUND REGISTER



DISK REGISTER



SWITCH REGISTER



THE VERSATILE INTERFACE ADAPTER

GENERAL

The Versatile Interface Adapter (VIA), as used in the Apple ///, is a very flexible I/O control device which minimizes the discrete control circuitry on the Main Logic Board. There are two VIAs used in the system.

Each VIA contains two 8-bit I/O ports, a serial port, and two 16-bit interval timers, as shown in the VIA Block Diagram. Each of the sections is very flexible and can be utilized in many operating modes. In the Apple ///, however,some of these modes cannot be used because of certain hardware design considerations.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves, or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register, and a pair of function control registers are provided.

Before we get into a functional description of how the VIA is used in the Apple ///, let´s first go through a pin description of the it.

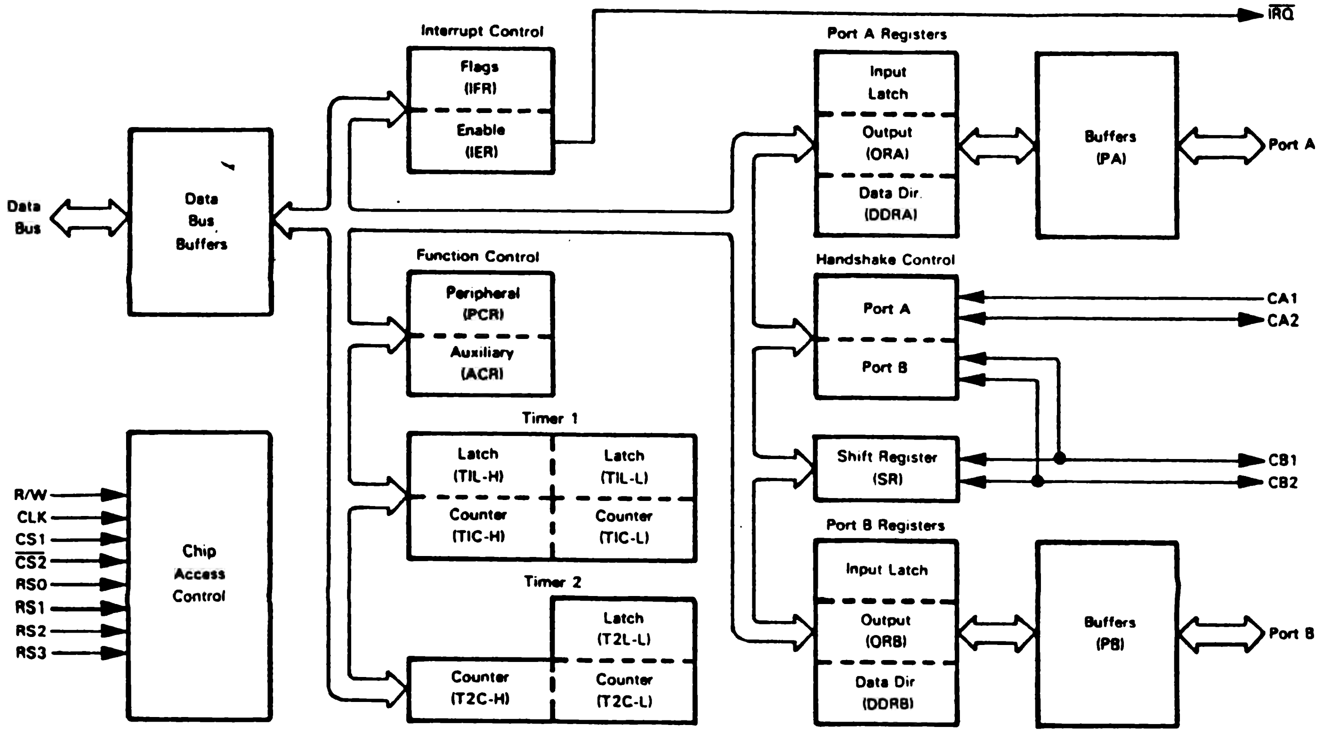
VIA [6522] PIN DESCRIPTIONS

RES* (Reset) (34)

The Reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters, and the shift register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc., and disables interrupting from the chip. On both VIAs this pin (34) is connected to the RESET* of the system. The system generates the reset at power on, or at depression of the Reset switch in conjunction with the Control key. (Note the latter may be disabled.)

02 (Input Clock) (25)

The Input Clock is the system PRE1M (PRE-1 MHZ) clock which operates at 1MHZ and is used to trigger all data transfers between the system processor and the VIA. The PRE1M, developed in the system timing circuits, is used within the device to clock the various functions of the registers and timers.



Block Diagram of the 6522 Versatile Interface Adapter

Addressing 6522 VIA Internal Registers

Label	Select Lines				Addressed Location
	RS3	RS2	RS1	RS0	
DEV	0	0	0	0	Output register for I/O Port B
DEV+1	0	0	0	1	Output register for I/O Port A, with handshaking
DEV+2	0	0	1	0	I/O Port B Data Direction register
DEV+3	0	0	1	1	I/O Port A Data Direction register
DEV+4	0	1	0	0	Read Timer 1 Counter low-order byte Write to Timer 1 Latch low-order byte
DEV+5	0	1	0	1	Read Timer 1 Counter high-order byte Write to Timer 1 Latch high-order byte and initiate count
DEV+6	0	1	1	0	Access Timer 1 Latch low-order byte
DEV+7	0	1	1	1	Access Timer 1 Latch high-order byte
DEV+8	1	0	0	0	Read low-order byte of Timer 2 and reset Counter interrupt Write to low-order byte of Timer 2 but do not reset interrupt
DEV+9	1	0	0	1	Access high-order byte of Timer 2; reset Counter interrupt on write
DEV+A	1	0	1	0	Serial I/O Shift register
DEV+B	1	0	1	1	Auxiliary Control register
DEV+C	1	1	0	0	Peripheral Control register
DEV+D	1	1	0	1	Interrupt Flag register
DEV+E	1	1	1	0	Interrupt Enable register
DEV+F	1	1	1	1	Output register for I/O Port A, without handshaking

R/W* (Read/Write) (22)

The direction of the data transfers between the 6522 and the system processor is controlled by the R/W* line, which is driven by the Internal Read/Write, I R/W*, signal generated by the processor.

If pin 22 is low, data will be transferred out of the processor into the selected VIA register, as in a write operation.

If R/W is high, data will be transferred out of the selected 6522 register, as in a read operation.

DBO-DB7 (Data Bus) (33-26)

The eight bi-directional data bus lines (in the Internal Data Bus) are used to transfer data between the VIA and the system processor.

- o During read cycles, the contents of the selected register are placed on the data bus lines and transferred into the processor.
- o During the write operation, these lines are high-impedance inputs and data is transferred from the processor into the selected register.
- o When the 6522 is unselected, the data bus lines are at high-impedance. These lines are connected to the Internal Data Bus and are not accessable from the outside world.

CS1, CS2* (Chip Selects) (24,23)

These two chip select lines are connected to direct decodes of the processor's address bus.

- o CS1 on both VIAs is controlled by the signal CS6522, a signal which is qualified by other system consideration.
- o CS2 is driven by the signal FFDX for IC at location B5, and FFEX for IC9 at location B6. The selected VIA register will be accessed when CS1 is high and CS2 is low.

RSO-RS3 (Register Selects) (38-35)

The four Register Select inputs permit the system processor to select one of the 16 internal registers, each of which performs a specific function, of the VIA as shown in the accompanying table.

IRQ (Interrupt Request) (21)

The Interrupt Request output goes low whenever an internal (to the VIA) flag is set and the corresponding interrupt enable bit is at 1. This output is "open-drain" to allow the interrupt request signal to be "wired-OR'ED" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port) (2-10)

The PA port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a data direction register.

The output is controlled by an output register. Input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers.

On standard TTL load, these lines are present in the input mode. Conversely, on standard TTL load, they will drive in the output mode.

CA1, CA2 (Peripheral A Control Lines) (40,39)

The two PA control lines can act as interrupt inputs (as used in the Apple ///) or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit.

PB0-PB7 (Peripheral B Port) (11-17)

The PB port consists of 8 bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port.

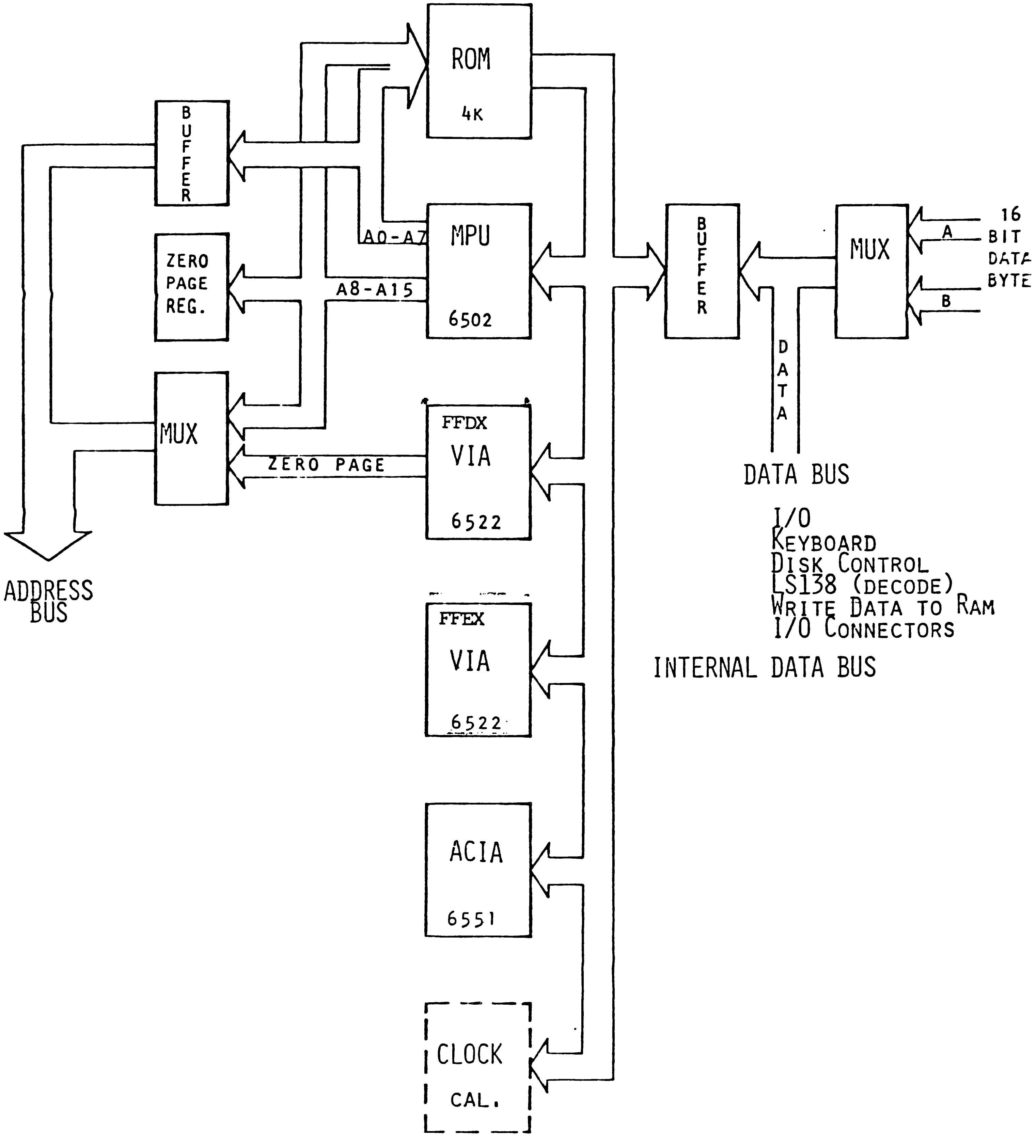
The polarity of the PB7 output signal can be controlled by one of the interval timers, while the second timer can be programmed to count pulses on the PB6 pin.

Peripheral B lines represent one TTL load in the input mode and drive one standard load in the output mode.

CB1, CB2 (Peripheral B Control Lines) (18-19)

The PB control lines act as interrupt inputs or as handshake outputs. As with the CA lines, each line controls an interrupt flag.

These lines also act as a serial port under control of the Shift Register. They have loading and driving characteristics identical to the CA control lines.


ROM
4K
BUFFER
MPU
6502
A0-A7
A8-A15
ZERO PAGE REG.
MUX
FFDX
VIA
6522
ZERO PAGE
FFEX
VIA
6522
ACIA
6551
CLOCK
CAL.
ADDRESS BUS
BUFFER
MUX
A
B
16 BIT DATA BYTE
DATA
DATA BUS
I/O
KEYBOARD
DISK CONTROL
LS138 (DECODE)
WRITE DATA TO RAM
I/O CONNECTORS
INTERNAL DATA BUS

VIA FUNCTIONAL DESCRIPTION

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register for specifying whether the Peripheral pins are to act as inputs or outputs.

- A "0" in a bit of the DDR causes the corresponding peripheral pin to act as an input.
- A "1" causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register and a bit in the Input Register. When the pin is programmed as an output, the voltage on the pin is controlled by the corresponding bit of the output Register. A one in the ORX causes the output to go high; a zero causes the output to go low.

Data may be written into ORX bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

The IRB Register operation is similar to that of the IRA. For pins programmed as outputs, however, there is a difference. When reading the IRB, it is the bit stored in the ORB that is sensed. That means the buffering and gating on the two ports differ in respect to pins programmed as outputs.

See the figures below detailing the data bytes programmed into the DDRs and the two control registers for each of the VIAs. Compare these with the environments of each device.

Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16 bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at the rate of PRE1M.

Upon reaching zero, an interrupt flag will be set; if the interrupt is enabled, the IRQ* will go low. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement.

In addition, the timer may be programmed to invert the output signal on a peripheral pin each tme it "times out." Each of these modes is discussed below.

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the write T1C-H (FFD5, FFE5) operation and generation of the processor interrupt is a direct function of the data loaded into the timer.

In the one-shot mode, writing into the high order latch has no effect on the operation of Timer 1. However, it is necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation.

When the processor writes into the high order counter

- the T1 interrupt flag is cleared;
- the contents of the low order latch are transferred into the low order counter;
- the timer again begins to decrement at the PRE1M rate.

After the timer reaches its time out, it continues to decrement until it is reset with the proper write operation.

The processor may read the current count of the timer to determine how long it has been since the interrupt has been set. Reading the counter does not reset the interrupt flag or the timer.

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts. These interrupts are accomplished in the "free-running mode."

In the free-running mode, the interrupt flag is set each time the counter reaches zero. However, instead of continuing to decrement from zero, the timer automatically reloads the contents of the high and low latches, and continues to decrement from there. In this mode, the interrupt flag can be cleared by writing T1C-H, or reading T1C-L, or by writing directly to the interrupt flag.

It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out. All of the interval timers are "retriggerable." Rewriting the counter will always re-initialize the time-out period.

Timer 2 Operation

Timer 2 operates as an interval timer in the one-shot mode only, or as a counter of negative pulses on the PB6 peripheral pin. A single bit in the ACR is provided for this mode selection.

Timer 2 is comprised of a write-only low order latch, a read-only low order counter, and a read/write high order counter.

Timer 2 One Shot-Mode

As an interval timer, T2 operates very much like T1 in the one-shot mode. Setting of the interrupt flag, however, will be disabled after the first time out, and it will not be set again until the write T2C-H operation.

The flag can be reset by reading T2C-L, or by writing T2C-H.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on the P6 pin. This is accomplished by first loading a number into T2, which clears the interrupt flag and allows the counter to be decremented by the pulses on PB6. The interrupt flag will be set when T2 is decremented to zero. The counter will continue to decrement.

Note that it is necessary to rewrite the timer to re-enable the subsequent interrupt flags.

Shift Register Operation

The Shift Register performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which set the various register modes are located in the ACR. In total, there are eight modes for this register. The primary use of the shift register is control of the serial printer port.

In the FFEX VIA, the shift register can be activated to "count" 8 VBL (Vertical Blanking) pulses. The shift register sets its interrupt flag each time it completes 8 shifts.

Refer to the figure below for descriptions of the various modes of the shift register.

Interrupt Operation

Controlling interrupts within the VIA involves three principal operations. These are:

- flagging the interrupts
- enabling the interrupts
- signalling the processor that an interrupt condition has occurred.

Interrupt flags are set by interrupting conditions which exist within the chip, or on inputs to the chip. These flags normally remain set until the interrupt has been serviced by the processor. To determine the source of an interrupt, the processor must examine these flags in order from highest to lowest priority.

Procedure:

1. Read the flag register into the accumulator.

2. Shift it right or left.

3. Use conditional branch instructions to detect an active interrupt.

Associated with each flag bit is an enable bit. This can be set or cleared by the processor to enable or disable the flag respectively. If a flag bit is enabled and set, it will cause the IRQ* output to go low, thus sending a direct request to the processor. In addition, bit 7 of the flag register is set to allow quick determination of which chip contains an interrupt condition.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register controls are applied to the chip, the contents of the IFR are placed on the Data Bus. Bit 7 indicates the condition of the IRQ output, however it cannot be directly cleared; all other bits must be cleared in order for this bit to become inactive.

For each interrupt flag in the IFR there is a corresponding bit in the Interrupt Enable Register. This is accomplished by writing to the IER. There are two steps to consider: the enabling write cycle and the disabling write cycle. The cycle is determined by the logic state of bit 7:

- o If bit 7 and the corresponding 0-6 bits are at "1", the 0-6 bits enable their matching flag.

- o If bit 7 is a 0, then the 0-6 bits containing a "1" disable the matching flag.

Refer to the figures to see the data byte configuration and device.

onment and Control

n so far has been very general and has not completely detailed
of the two VIAs within the Apple ///. However, one must be
the many registers and modes to understand how the VIA is
ow it can be configured for various operations.

figures and tables detail the environment and address locations
registers and I/O pins for the two chips. (Many of the signals
trols or busses; their descriptions relate to both devices.)

pins of the VIA are connected to the associated pins of the
bus. When the chip is properly addressed and selected, each of
gisters may be accessed for reading or writing data, control
or timer states. It is this bus through which all data passes
and/or processor.

connected to the RESET line. The system generates the reset at
en the Reset switch is depressed with the Control key.

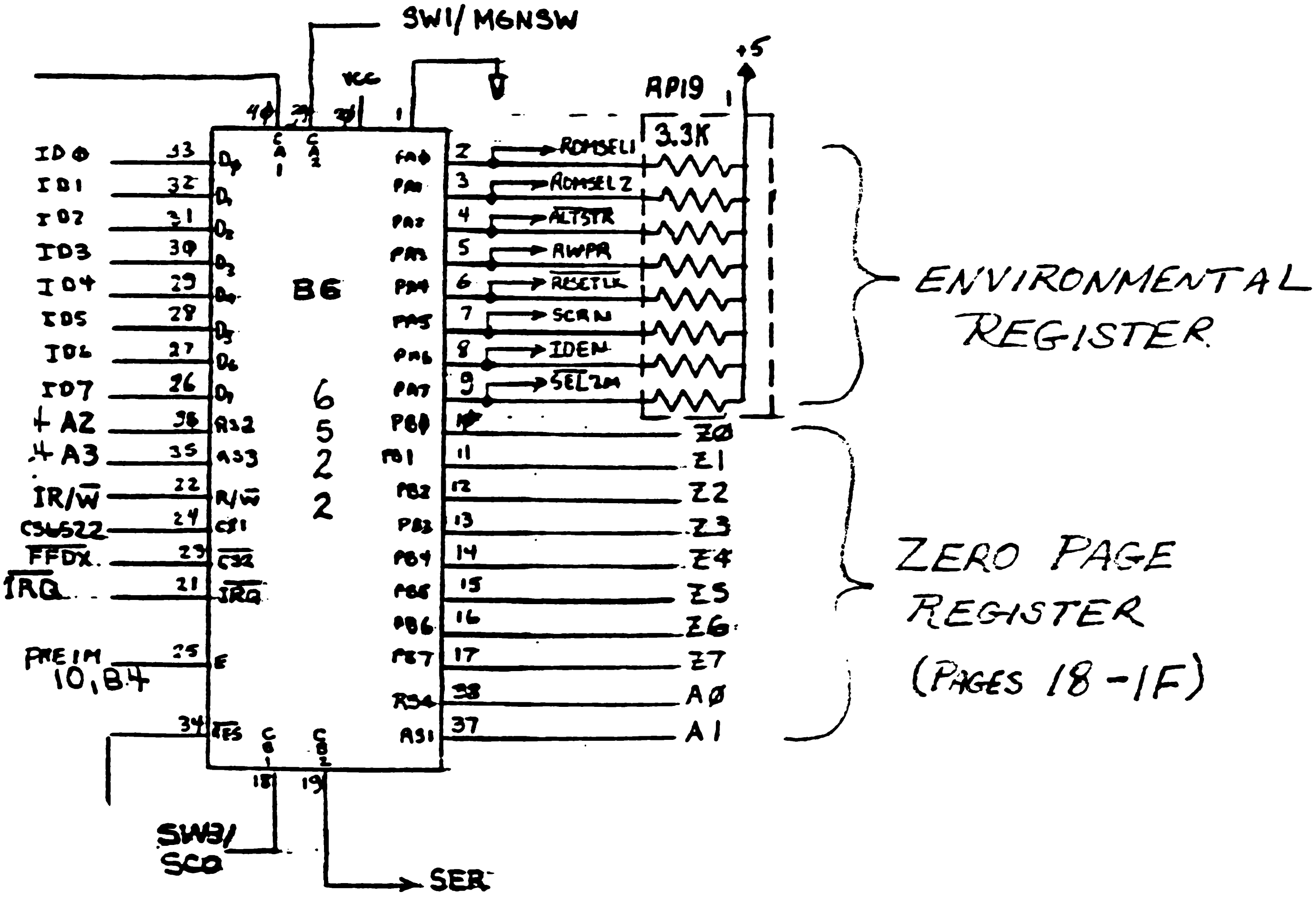
ntrol key may be software disabled.)

is connected directly to the processor's internal Read/Write
gnal cannot be accessed from the outside world. It is obviously
l the direction of the data to or from the device.

in is driven by the PRE1M signal developed in the system timing
is used within the device to clock the various functions of the
timers.

developed under Rom decode of various address states or ranges
selections, and drives the CS1 line of both VIAs.

s address lines directly drive the Register Select input lines.



ADDRESS	Register Number	RS Coding				Register Desig.	Description	
		RS3	RS2	RS1	RS0		Write	Read
FFD0	0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
FFD1	1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
FFD2	2	0	0	1	0	DDRB	Data Direction Register "B"	
FFD3	3	0	0	1	1	DDRA	Data Direction Register "A"	
FFD4	4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
FFD5	5	0	1	0	1	T1C-H	T1 High-Order Counter	
FFD6	6	0	1	1	0	T1L-L	T1 Low-Order Latches	
FFD7	7	0	1	1	1	T1L-H	T1 High-Order Latches	
FFD8	8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
FFD9	9	1	0	0	1	T2C-H	T2 High-Order Counter	
FFDA	A 10	1	0	1	0	SR	Shift Register	
FFDB	B 11	1	0	1	1	ACR	Auxiliary Control Register	
FFDC	C 12	1	1	0	0	PCR	Peripheral Control Register	
FFDD	D 13	1	1	0	1	IFR	Interrupt Flag Register	
FFDE	E 14	1	1	1	0	IER	Interrupt Enable Register	
FFDF	F 15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No "Handshake"	

SY6522 Internal Register Summary

These four addresses, along with the two chip select lines, activate the chip for access to and from the data bus. You can see that the decimal equivalent of the address (Register Select) lines equals the register number, as detailed in the port address tables.

To determine the complete I/O location:

- Express the A0-A7 bits in Hex
- Substitute the Hex expression for the "x" in the signal name applied to the CS2 input.

IRQ*

The Interrupt Request line is a wire OR'ED bus, shared with the other LSI devices within the system which directly interrupt the processor. The VIA can generate an interrupt due to internal status and can be configured to interrupt on various input conditions. Each VIA provides indirect interrupts to the processor for the other devices in the system, including the slot interrupts. By polling the VIAs, the processor can quickly determine which device or group of devices needs servicing.

VIA (FFDX)

This VIA has the following responsibilities:

- Environmental Register
- Zero Page Register
- Global Interrupt Request
- Serial Data Port Interrupt & Clocking (Silentype)

The signals of the IC at location B6 which are not common to both 6522s are either the port I/Os or the chip select line, CS2.

FFDX

This signal comes from the Device Select logic, and is true for the 16 address states, FFD0 through FFDF.

The table below shows how the signal FFDX (CS2) and the Address Lines on the Register Select Inputs access each of the 16 registers within the VIA.

Port A Description

The ORA for this device is also called the "Environmental Register" by the system. It is programmed to all outputs, and contains various control mode states which may be software modified.

PA0 and PA1 are used as software switches to control which set of Roms are to be used by the system, and also to indicate there is an expanded set of Rom in the system.

PA2 provides the software switch that enables the Apple /// to switch between two memory stacks.

PA3 is a software switch which will enable or disable the system for writing into the Ram. It can be set for entire banks or it can be set at will to disallow writing into memory.

PA4 is a software switch which will cause the function of the Reset switch to be ignored, and will simultaneously disable the Non-Maskable Interrupts from the I/O slots.

PA5 contains the switch "Scrn" (Screen) which is used to modify the Blanking signal.

Global IRQ

The CA1 line is connected to "OR" function of the slot IRQs. If any slot is requesting an interrupt, this line will toggle. The VIA then generates an IRQ and sets the associated Interrupt flag.

Sw1/Mgnsw

This line connected to the CA2 line can be programmed to cause an interrupt on either edge of transition. It could be used to have a Function Only run while the switch is depressed, or vice versa.

SCO/SER

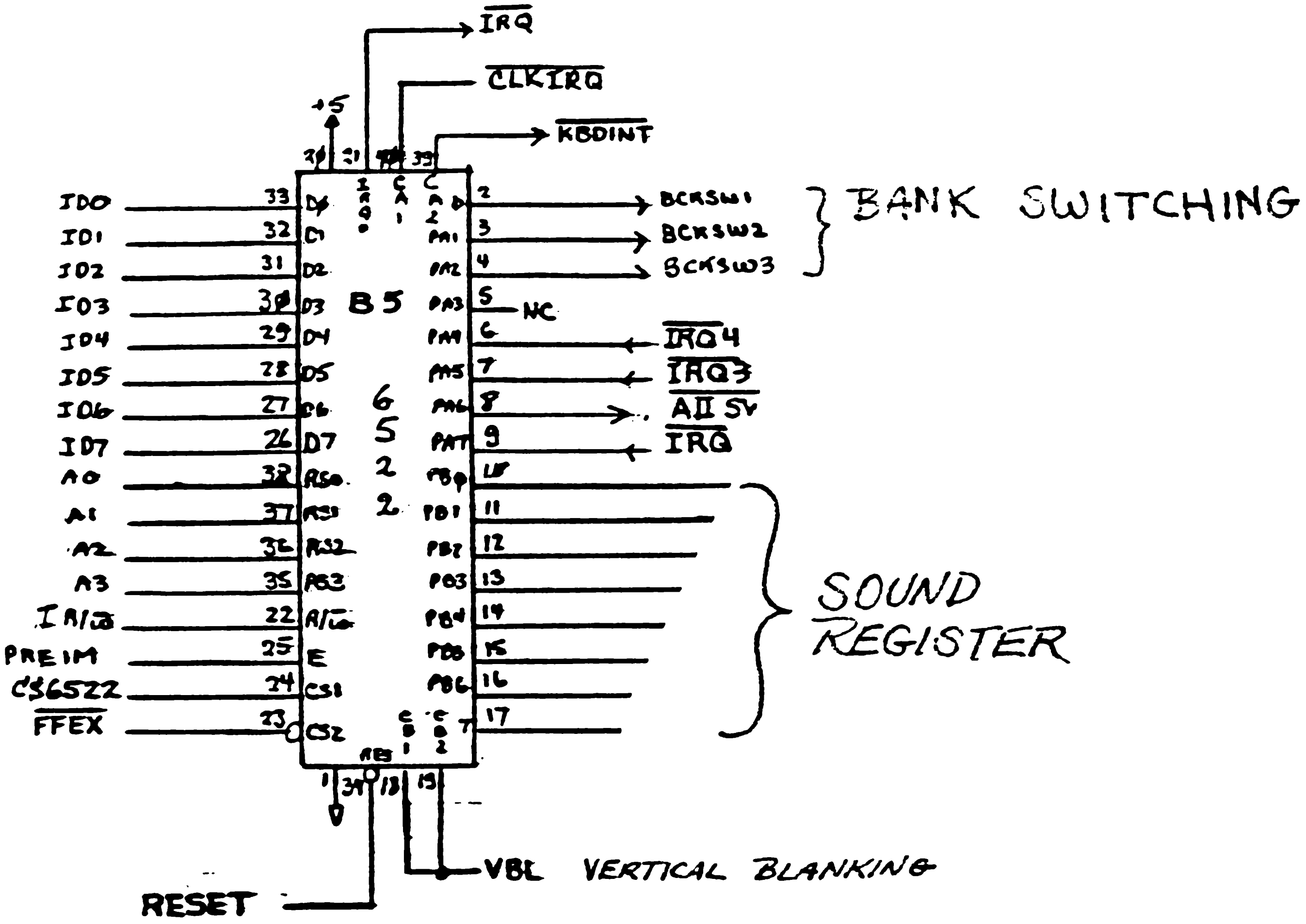
These two signals form a very elementary serial data port. They are usually programmed as data, and strobe to a serial RO printer.

The port may also be configured as a serial input register or simply as interrupts for the two external lines.

SCO/SER are connected to CB1 and CB2 respectively.

Z0-Z7 (Zero Page Register)

VIA FFEX



ADDRESS	Register Number	RS Coding				Register Desig.	Description	
		RS3	RS2	RS1	RS0		Write	Read
FFE0	0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
FFE1	1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
FFE2	2	0	0	1	0	DDRB	Data Direction Register "B"	
FFE3	3	0	0	1	1	DDRA	Data Direction Register "A"	
FFE4	4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
FFE5	5	0	1	0	1	T1C-H	T1 High-Order Counter	
FFE6	6	0	1	1	0	T1L-L	T1 Low-Order Latches	
FFE7	7	0	1	1	1	T1L-H	T1 High-Order Latches	
FFE8	8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
FFE9	9	1	0	0	1	T2C-H	T2 High-Order Counter	
FFEA	10	1	0	1	0	SR	Shift Register	
FFEB	11	1	0	1	1	ACR	Auxiliary Control Register	
FFEC	12	1	1	0	0	PCR	Peripheral Control Register	
FFED	13	1	1	0	1	IFR	Interrupt Flag Register	
FFEE	14	1	1	1	0	IER	Interrupt Enable Register	
FFEF	15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No "Handshake"	

:eferred to as the Zero Page Register. In other words, its is to store the current "Zero Page" of the memory. The Apple f moving the Zero Page, a feature which greatly enhances the ıe system.

a secondary function; it also serves as the address register e Clock. The RTC must have the addresses stable for an extime, so instead of adding another latch in the hardware, the s port for control.

me the port is used for the RTC function it must be restored ro Page setting.

providing the following:

- o Bank Switching
- o Sound Register
- o Interrupt Recognition-clock, keyboard

cted to the VIA located at B5 which are not common to both

- o the A and B port I/Os,
- o the port control lines, and
- o the CS2 line.

esponds to FFDX in that it is true for a group of 16 the corresponding table for the complete detail of the ocations.

are configured as outputs and contain the software switches . Currently, the system segregates the 128K memory into decimal decode of the binary bit weight reveals the bank.

are configured as inputs. Slot 1 and 2 IRQs, the Solid the IRQ line itself form the respective inputs.

ed, the processor will poll the VIAs first to get a quick ıe system. It can then identify and service the requesting ce it doesn't need to poll each individual device.

The processor can, at certain times, read this port for the status of the special Apple switch on the keyboard without disturbing the keyboard circuit.

The IRQ* signal is wrapped around to the PA7 line for special diagnostic purposes.

CLK IRQ*

The Real Time Clock's interrupt is connected to the CA1 line, which is programmed to be a negative edge active input. When the clock generates an interrupt, it will set the IRA flag in the IFR. The PA port is conditioned for non-latching, however, resulting in a basically independent interrupt for the clock.

Keyboard Interrupt

The keyboard's interrupt is connected to the CA2 input, which is programmed to be an independent negative edge interrupt. It will set Bit 0 in the IFR and cause the IRQ* line to go low.

Note: The keyboard can, for the most part, be disabled by disabling the interrupt flag for the CA2 line.

VBL (Vertical Blanking)

This input can perform two functions, depending on how the CB1, CB2, and Shift Register are programmed.

- The system may want to be interrupted at each vertical blanking cycle. If so, you would program the CB2 line to be an independent interrupt OR let it strobe the IPB and set the corresponding bit flag.
- The system may want to synchronize an operation to the display, but may not want to be interrupted at each VBL. If this is the case, the system can configure the Shift Register to count 8 occurrences of the VBL signal. An interrupt will then occur after each set of 8 Vertical Blanking cycles (about once every second), in sync with the display scan.

PB Port Description

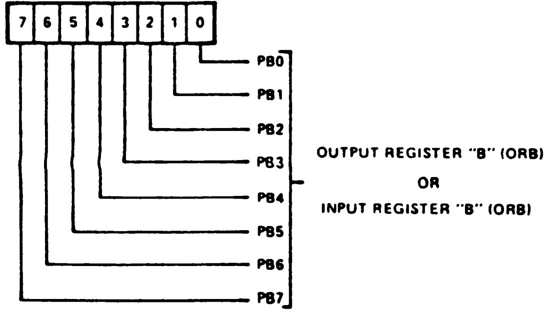
The first 6 lines of the B port are configured to be outputs. They are inputs to the sound Generator.

- The tone generated at the speaker can be varied by changing the bit values of these lines.
- There are 127 possible tone combinations; the missing one turns the tone off completely.

PB6 is connected to the I/O Count line. Depending on the device in the slots, the VIA may be programmed to count a certain number of pulses generated or to determine that only one pulse occurred. Either way, the VIA will generate an IRQ and set the appropriate bit flag.

The last bit is used to monitor the NMI (Non Maskable Interrupt) line generated by the devices in the I/O slots.

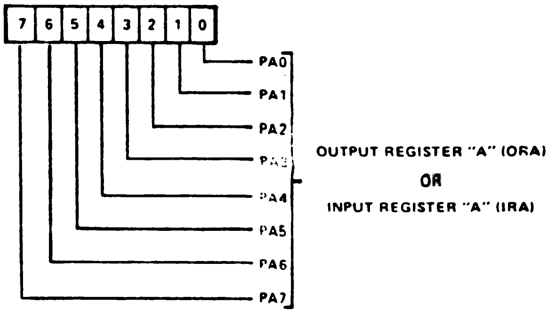
REG 0 – ORB/IRB **FFD0/E0**



Pin Data Direction Selection	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no affect.
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 9. Output Register B (ORB),
Input Register B (IRB)

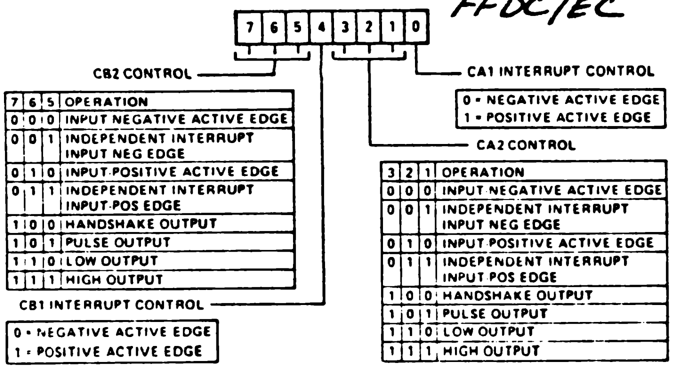
REG 1 – ORA/IRA **FFE1/D1**



Pin Data Direction Selection	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 10. Output Register A (ORA),
Input Register A (IRA)

REG 12 – PERIPHERAL CONTROL REGISTER FFDC/EC



7	6	5	OPERATION
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE
0	1	0	INPUT-POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT-POS EDGE
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

CB1 INTERRUPT CONTROL

0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

CA1 INTERRUPT CONTROL

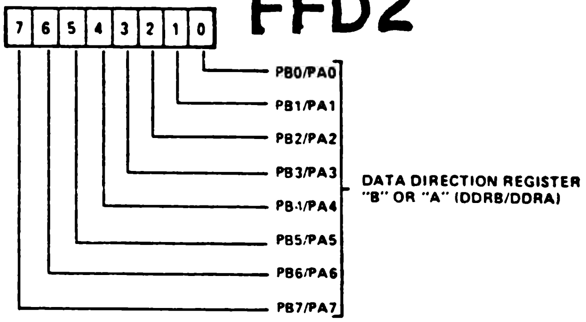
0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

CA2 CONTROL

3	2	1	OPERATION
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT POS EDGE
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

Figure 14. CA1, CA2, CB1, CB2 Control

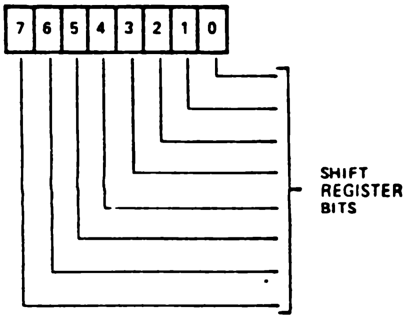
REG 2 (DDRB) AND REG 3 (DDRA) **FFD2**



"0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH IMPEDANCE)

"1" ASSOCIATED PB/PA PIN IS AN OUTPUT, WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT.

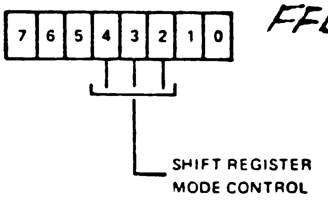
REG 10 – SHIFT REGISTER FFEA/DA



NOTES:

1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

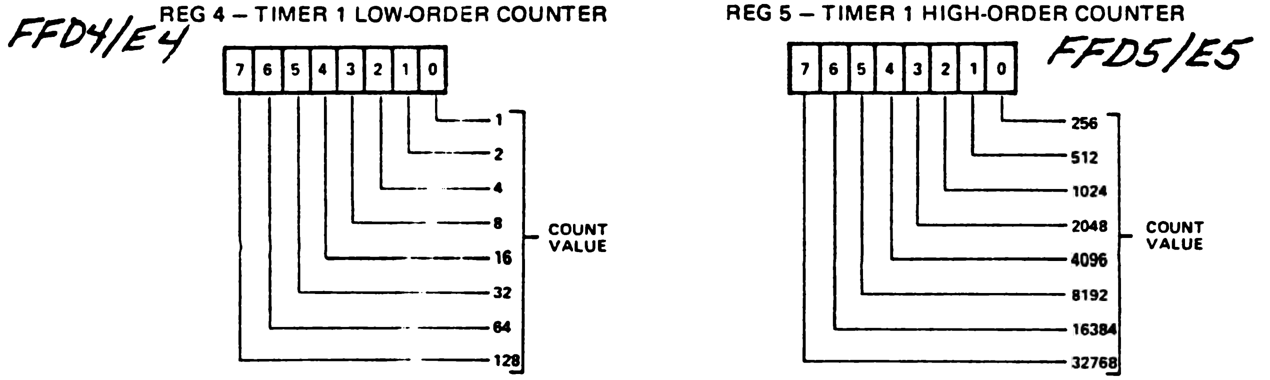
REG 11 – AUXILIARY CONTROL REGISTER FFDB/EB



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF ϕ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF ϕ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes. The four possible modes are depicted in Figure 17.



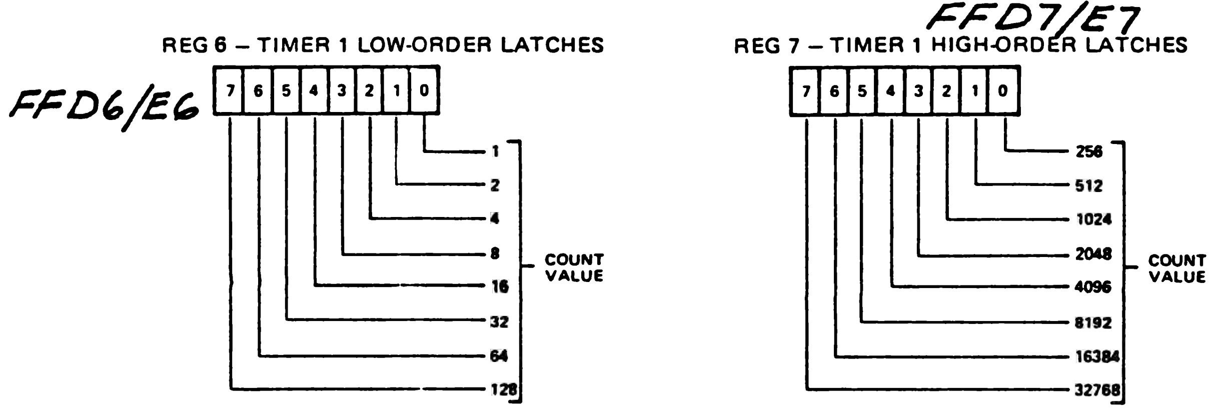
WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.

READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers



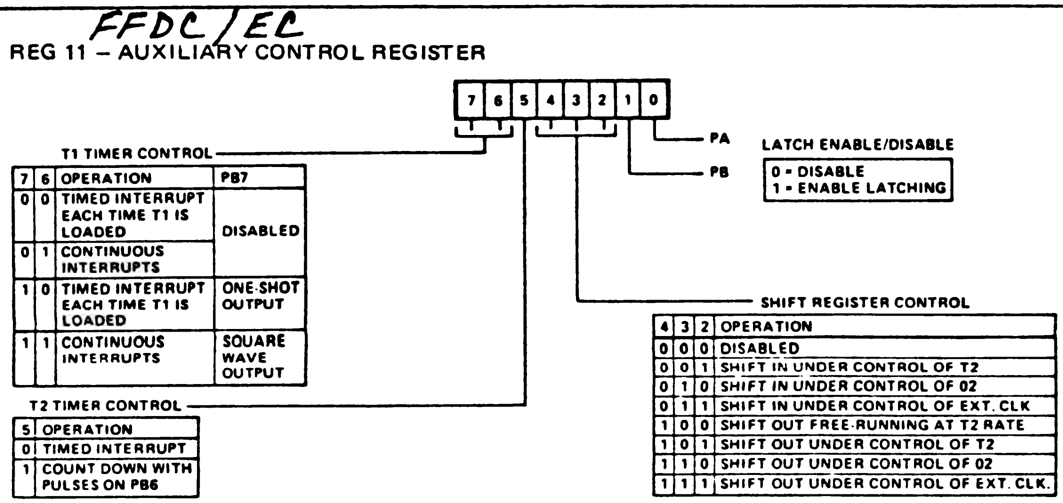
WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4.

READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers



T1 TIMER CONTROL

7	6	OPERATION	PB7
0	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	DISABLED
0	1	CONTINUOUS INTERRUPTS	
1	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	ONE-SHOT OUTPUT
1	1	CONTINUOUS INTERRUPTS	SQUARE WAVE OUTPUT

T2 TIMER CONTROL

5	OPERATION
0	TIMED INTERRUPT
1	COUNT DOWN WITH PULSES ON PB6

LATCH ENABLE/DISABLE

0 = DISABLE
1 = ENABLE LATCHING

SHIFT REGISTER CONTROL

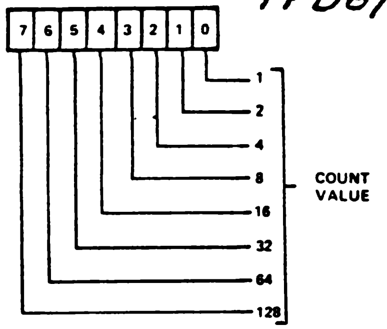
4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF 02
0	1	1	SHIFT IN UNDER CONTROL OF EXT. CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF 02
1	1	1	SHIFT OUT UNDER CONTROL OF EXT. CLK.

Figure 17. Auxiliary Control Register

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

REG 8 – TIMER 2 LOW-ORDER COUNTER

FFD8/E8

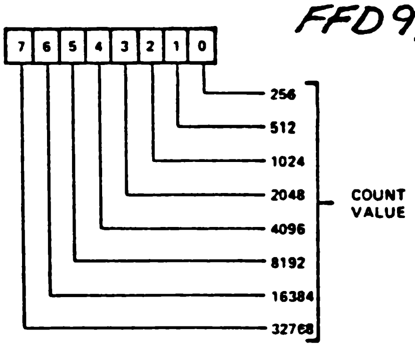


WRITE – 8 BITS LOADED INTO T2 LOW-ORDER LATCHES.

READ – 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

REG 9 – TIMER 2 HIGH-ORDER COUNTER

FFD9/E9

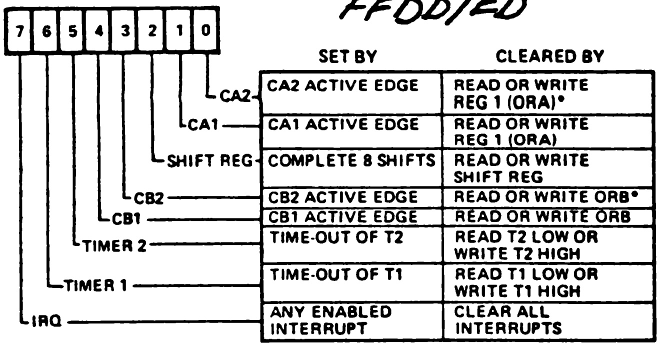


WRITE – 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER. IN ADDITION, T2 INTERRUPT FLAG IS RESET.

READ – 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

REG 13 – INTERRUPT FLAG REGISTER

FFDD/ED

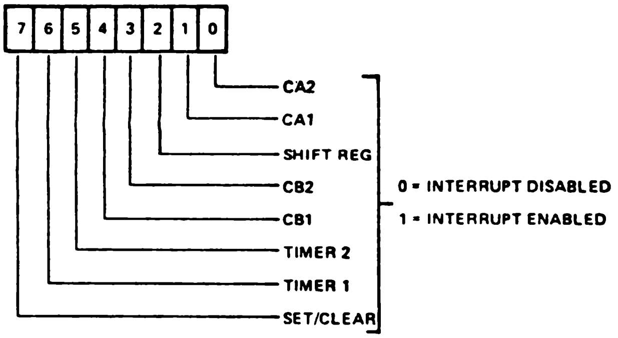


	SET BY	CLEARED BY
CA2	CA2 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)*
CA1	CA1 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)
SHIFT REG	COMPLETE 8 SHIFTS	READ OR WRITE SHIFT REG
CB2	CB2 ACTIVE EDGE	READ OR WRITE ORB*
CB1	CB1 ACTIVE EDGE	READ OR WRITE ORB
TIMER 2	TIME-OUT OF T2	READ T2 LOW OR WRITE T2 HIGH
TIMER 1	TIME-OUT OF T1	READ T1 LOW OR WRITE T1 HIGH
IRQ	ANY ENABLED INTERRUPT	CLEAR ALL INTERRUPTS

* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

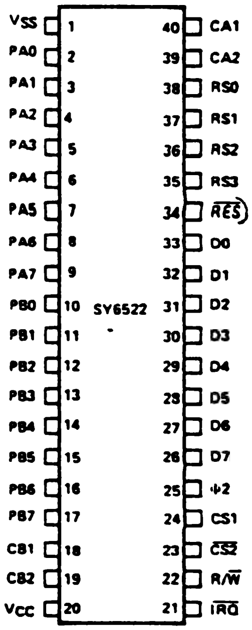
Figure 25. Interrupt Flag Register (IFR)

REG 14 – INTERRUPT ENABLE REGISTER



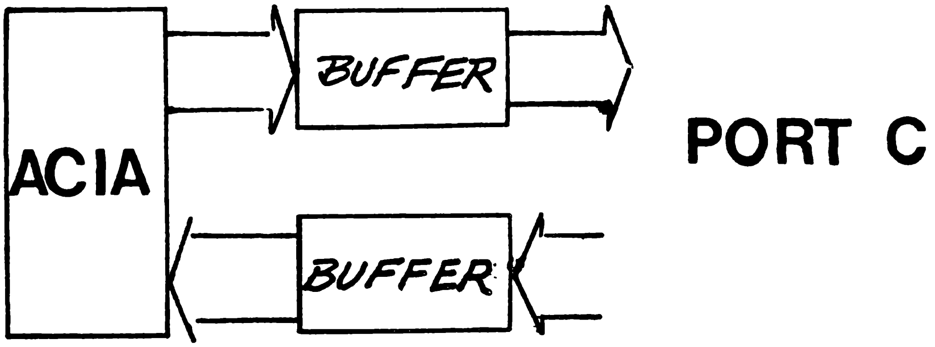
NOTES:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "0" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

PIN CONFIGURATION



THE 6551 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER

As you know, the Apple /// can be used to communicate to all devices that use the RS-232-C standard communications format. This means the Apple /// can communicate with letter-quality printers, modems, high speed data collection devices, and other computers. The Apple /// has a built in Asynchronous Communications Interface Adapter (ACIA). It is located at addresses C0F0 through C0F3. This device is solely for use as a serial port input/output controller. This RS-232-C protocol, specified by the Electrical Industries Association (EIA), is provided at port C connector through two buffer devices as shown below.



The 6551 contains seven registers and five control circuits dealing with the control, timing, and interrupt logic of transmitting amd receiving data through the serial EIA port. A block diagram of the 6551 ACIA is shown in Figure 1.

Before using the 6551, the system (or programmer) must initialize it for the I/O mode. Once initialized it will be set to transmit and/or receive data within the parameters set in the control bytes.

The Apple /// I/O addresses for data and control are presented in the following discussions. The function of the data byte (depending on location) will also be shown. The characters in parentheses next to each register represent the function of the associated pin of the ACIA (i.e. R=Read,W=Write).

RECEIVE DATA REGISTER (RxD)

The Receive Data Register is accessed with I/O location C0F0 (r). The contents of the Receive Data Register will be the data bits of the completely received serial input character. This register is used as temporary data storage for the 6551 receive circuit. The first data bit received will be the LSB of the data byte (Bit 0).

C0F0 (R) RECEIVE DATA REGISTER

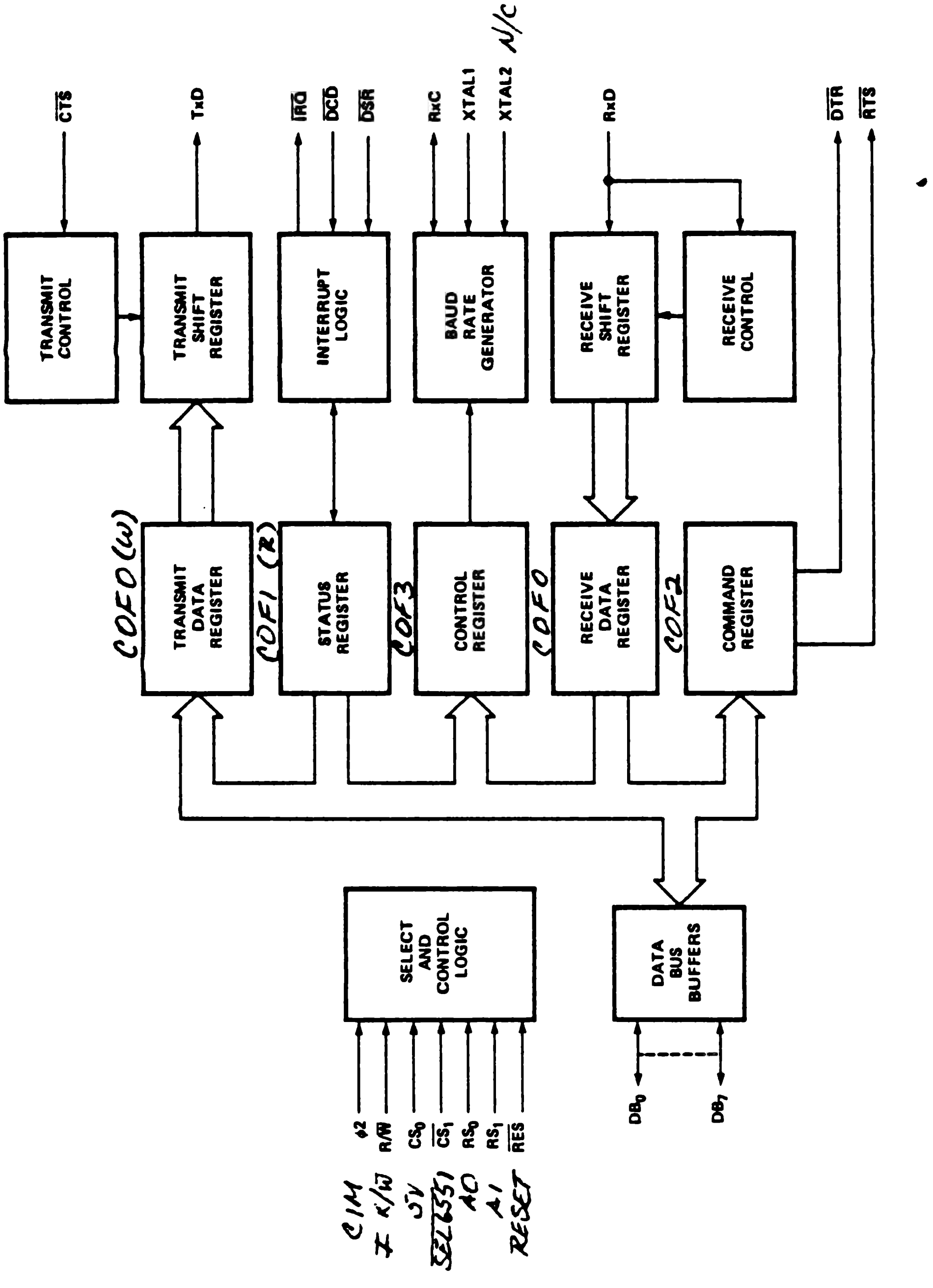


FIG 1

THE ACIA BLOCK DIAGRAM

TRANSMIT DATA REGISTER (TxD)

To load a byte to be transmitted out the serial EIA port, I/O location COFO (w) must be accessed. The LSB will be the first data bit transmitted.

COFO (w) TRANSMIT DATA REGISTER (w)

STATUS REGISTER

The 6551 continually monitors the condition of the registers and the quality of the incoming data. When I/O location COF1 (R) is accessed the contents of the Status Register is placed on the data bus. The meanings of the eight bits of the status byte are detailed following the illustration.

COF1 (R) STATUS REGISTER

IRQ--Bit 7 indicates that the 6551 generated an IRQ to the system for one of the folllowing conditions:

1. Change of status of the DCD line.
2.. Change of status of the DSR line.
3. The Transmit Register has emptied.
4. The Receive Register has filled with a new incoming character.

(Note: the third and fourth conditions are program controlled as to whether or not they inititate an IRQ).

DSR---Bit 6 indicated the status of the DSR line from the interface. 0=DSR is low and ready. 1=DSR is high and not ready.

DCD---Bit 5 shows the condition of the Data Carrier Detect line from the interface. 0=DCD is low and the carrier is detected. 1=DCD is high and not ready.

TDRO--Bit 4 informs the host that the Transmit Data Register has transferred its contents to the outputs shift register and now ready to accept another character (byte). 0=not empty, 1=empty.

RDRF1-Bit 3 indicates that the Received Data Register has been filled with a character from the line. 0=not full, 1=full.

OVERR-Bit 2 shows that there has been an overrun error, that is, a new character has been transferred to the Received Data Register before the previous received character was taken by the program and the RDRF1 flag reset. This error will not generate an IRQ but should be checked by the program so that tht lost data can be recovered. 0=no overrun, 1=overrun has occurred.

FRMERR-Bit 1 informs the program that the incoming data did not conform to the parameters set in the Control Register. That means usually that when the 6551 checked for the position and number of stop bits if found a descrepency. This error most often happens when the remote device is transmitting at a different baud rate. 0=no framing error, 1=framing error detected. This error does not generate an IRQ.

PARERR--Bit 0 indicates that there has been a parity error in the incoming data. This error does not cause an IRQ to be generated. 0=no parity error,1=parity error detected.

PROGRAMMED RESET

By accessing COF1 (w) the Status Register will be reset to all 0's. The data byte on the bus at that cycle does not have to be any particular structure.

COF1 (w) PROGRAMMED RESET (w)

COMMAND REGISTER

To access the Command Register to initialize or modify the Command byte a COF2 (w) must be executed with the data byte configured for the desired effect. To inspect the contents (or current command structure) a COF2 (R) will cause the 6551 to place the contents of the Command Register on the data bus. The meaning of each bit is explained below.

COF2 (r/w) COMMAND REGISTER (r/w)

Parity ck ctrls--Bits 7 through 5 command the 6551 in regard to parity checking. Bit 5 is parity enable. Bit 7 determines whether the parity bit position will have odd/even or fixed one/zero function. Bit 6, depending on the condition of Bit 7 selects either odd or even parity, or fixed mark (one) or fixed zero (space). Table -- below clearly shows the conditions of these bits.

ECHO--Bit 4 determines whether the 6551 will echo (transmit a duplicate image of what is received) the received data to the remote device. 0=no echo, 1=echo data.

TRANS CTRLS--Bits 3 and 2 control the 6551 in three (3) functions. They are Transmit Interrupt, the state of the RTS line, and the Transmit BRK (break, a continuous space on the line for approximately 200 milliseconds). Table -- shows which state controls which function.

INT--Bit 1 command the 6551 to either enable or disable interrupt on Received Data Register full (bit 3 of the status byte). 0=IRQ on RDRF1, 1=no interrupt.

DTR--Bit 0 enable the 6551 to transmit and receive or not. It also changes the state of the DTR output to match the condition of the 6551. 0=disable xmit/rcv (DTR high), 1=enable Xmit/Rcv (DTR low).

CONTROL REGISTER

The final I/O location on the 6551 is the Control Register. By writing to CPF3 (w) with a properly structured date byte four functions are controlled. They are Number of Stop bits appended to outgoing data byte (and checked for on the incoming date byte), the source of the receiver clock, and the baud rate selection. By reading location COF3 (x) the current control configuration can be seen on the data bus.

COF3 (R/W) CONTROL REGISTER (R/W)

STOPB--Bit 7 controls the number of stop bits that will be added to the transmitted data word. 0=1stop bit, and depending on the word length selection 1=2 stop bits or 1 bit if word length is 8 and parity is selected, or 1/2 bits if word length is 5 and no parity is selected.

WORD LEN--Bits 6 and 5 determine the number of data bits that will be transmitted or received in the data word. The values (6,5) are as follows: 0,1=7 bits; 1,0=6 bits; 1,1=5 bits.

'XCLK--Bit 4 indicates the source of the receiver clock. 0=external clock source, 1=baud rate generator (internal). When the internal selection is made the RxC pin becomes an output.

BAUD RATE--Bits 3 through 0 select the baud rate at which the 6551 will operate. Table -- details the various selections available based on a standard 1.8432 MHZ clock input. It should be noted that 0,0,0,0 selects the external clock as the baud rate source but the clock rate is actually dividied by 16 so the external clock should be 16x the desired baud rate.

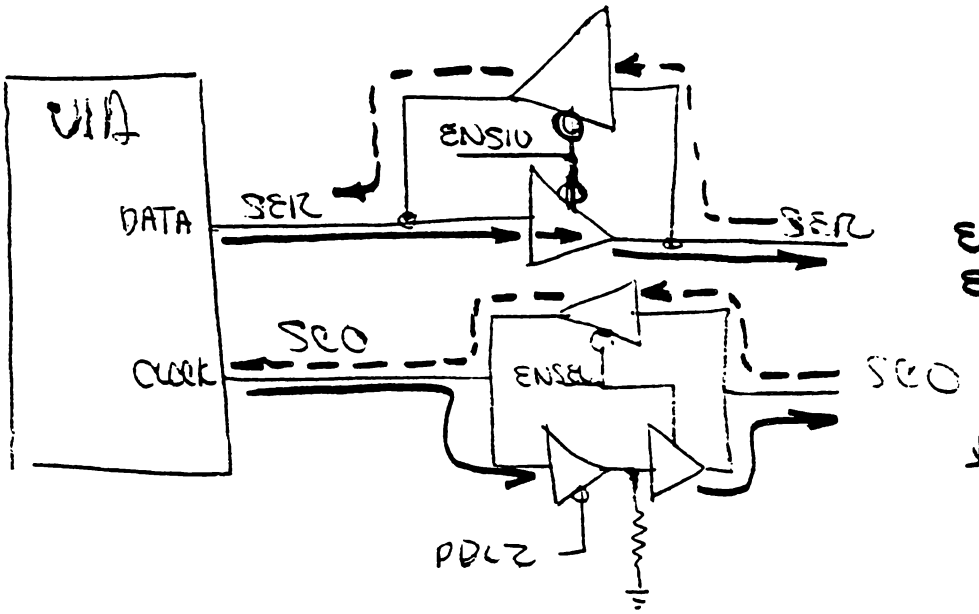
SIMPLE SERIAL PORT

Incorporated into the A /// logic design is a provision for a simple serial port. Its main purpose is to support a Silentype printer. However, it is not a dedicated port since it shares the same connector with one of the joysticks. The user has the option of having the Silentype or a second joystick. For most applications, one joystick is more than enough since the A /// is not really intended for a "games" player. The joystick would be used more for applications like cursor control.

The serial port is actually derived from a feature of the VIA. Two of the port control lines (PB1, PB2) can be configured to be a shift register, hence a simple serial port (see the section on VIA's and read the spec sheet in the appendices). In the system certain other software controlled switches must be set to enable the port. These switches are found in another addressable latch (U177). They control the direction of data and clock to and from the board. The VIA is programmed internally to determine its function.

The signal ENSIO when high enables data from the VIA to the port, when low it enables data from the port to the VIA. The signal ENSEL determines the direction of the clock, high enables clock from the VIA to the port (if and only if PDL2 is low), low enables the port to supply the clock to the VIA. ENSEL when high also enables the AXCO signal to the port, this can be used as a select or acknowlege to the remote device. The remote device may put status bits on the "switch" line which can be used to notify the processor of some requirement mutually agreed upon.

— SIMPLE SERIAL PORT —



DATA
ENSIO=1 = OUT
ENSIO=0 = IN

CLOCK
ENSEL=1= OUT*
ENSEL=0= IN

* IF PDL2=0
IF PDL2=1
THE OUTPUT
HELD LO.

NOTE: THE VIA MAY SEND DATA USING IT'S OWN CLOCK OR IT MAY BE SHIFTED WITH A REMOTE CLOCK.

ALSO IT MAY STROBE DATA IN WITH IT'S OWN CLOCK OR IT MAY BE STROBED IN WITH A REMOTE CLOCK.

PINOUT OF THE RS-232-C SERIAL INTERFACE (PORT C)

PIN	NAME	DESCRIPTION
1	SGND	Shield GrouND.
2	TXD	Transmitted Data; serial data output from the Apple.
3	RCD	ReCieved Data; serial input to the Apple.
4	RTS	Request To Send output; this indicates that the Apple is ready to transmit data. This line is active whenever the Serial Card emulation is used.
5	CTS	Clear To Send input; this acknowledges that the Apple may begin transmission. This line is ignored by the Serial Card emulation.
6	DSR	Data Set Ready input; this acknowledges that the remote device is operational. The Serial Card emulation checks this line and will not send characters if this line is held inactive. This can be used to prevent the Apple from overflowing a printer input buffer.
7	GND	Signal GrouND.
8	DCD	Data Carrier Detect; this acknowledges that the remote device is ready to transmit data. The Serial Card emulation checks this line and will not send characters if this line is held inactive. This line can be used to prevent the Apple from overflowing a printer input buffer.
9-19		No connect.
20	DTR	Data Terminal Ready output; this indicates that the Apple is on and operational. This line will be active anytime the Serial Card emulation is used.

THE ACIA

The Apple /// has a built-in 6551 ACIA (Asynchronous Communication Interface Adapter). It is located at addresses $C0F0 thru $C0F3 (decimal -16144 to -16141). The ACIA has five registers: transmit data, receive data, status, command, and control.

The transmit register ($C0F0) is used to send data out the Apple /// to an external device, such as a modem or a printer. A byte is transmitted by setting the control and command registers appropriately and then polling the status register. When bit 4 of this register is one the ACIA is ready to shift the next byte out. Often bits 5 and 6 are tested for zero to assure the Data Carrier Detect and Data Set Ready are valid as some printers use these lines as handshake signals.

Care must be taken when writing to the transmit data register as it is at the same address as the receive data register. The 6502 will do false reads when certain address modes are used, thus discarding whatever was in the receive data register.

The receive data register ($C0F0) contains the last byte received from an external source, such as a modem. Bit 3 of the status register is one whenever this register is full.

The status register ($C0F1) indicates the states of Data Set Ready, Data Carrier Detect, whether the transmit and receive registers are full, and whether a framing, overrun or parity error has occured on input.

The command register ($C0F2) sets the parity, echo mode, transmit and receive enables, and BRK transmission.

The control register ($C0F3) sets the number of stop bits, data word length, receiver clock source, and baud rate.

PHYSICAL PINOUT OF THE RS-232-C SERIAL INTERFACE

13 12 11 10 9 8 7 6 5 4 3 2 1

25 24 23 22 21 20 19 18 17 16 15 14

RS232 CONNECTOR USAGE (PORT C)

The Apple /// is classified as Data Terminal Equipment (DTE) under the EIA RS-232-C interface specification. It can be directly connected to a piece of Data Communications Equipment (DCE), such as a modem. To connect the Apple to another piece of Data Terminal Equipment (such as a printer), you must use a modem eliminator.

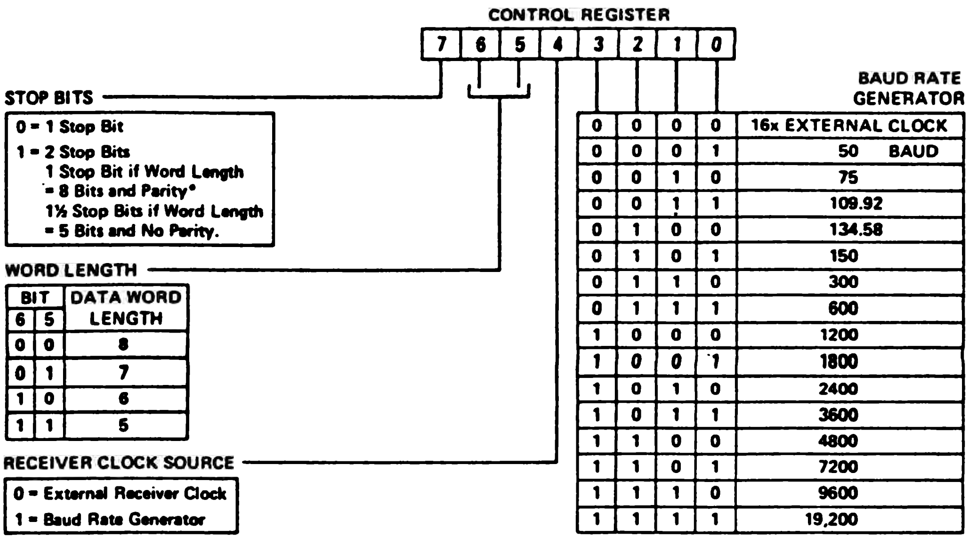
All output levels are minimum +6 volts when logic 0 and maximum -6 volts when logic 1, measured into a 3K ohm load.

All inputs have a turn-on positive going threshold of +1.25 volts and a turn-off negative going theshold of +.8 volts, typical. All inputs sink a 10 mA current, maximum.

CONTROL REGISTER

The Control Register is used to select the desired mode for the SY6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

C0F3



STOP BITS

0 = 1 Stop Bit
1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1½ Stop Bits if Word Length = 5 Bits and No Parity.

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

BAUD RATE GENERATOR

3	2	1	0	
0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

*This allows for 9-bit transmission (8 data bits plus parity).

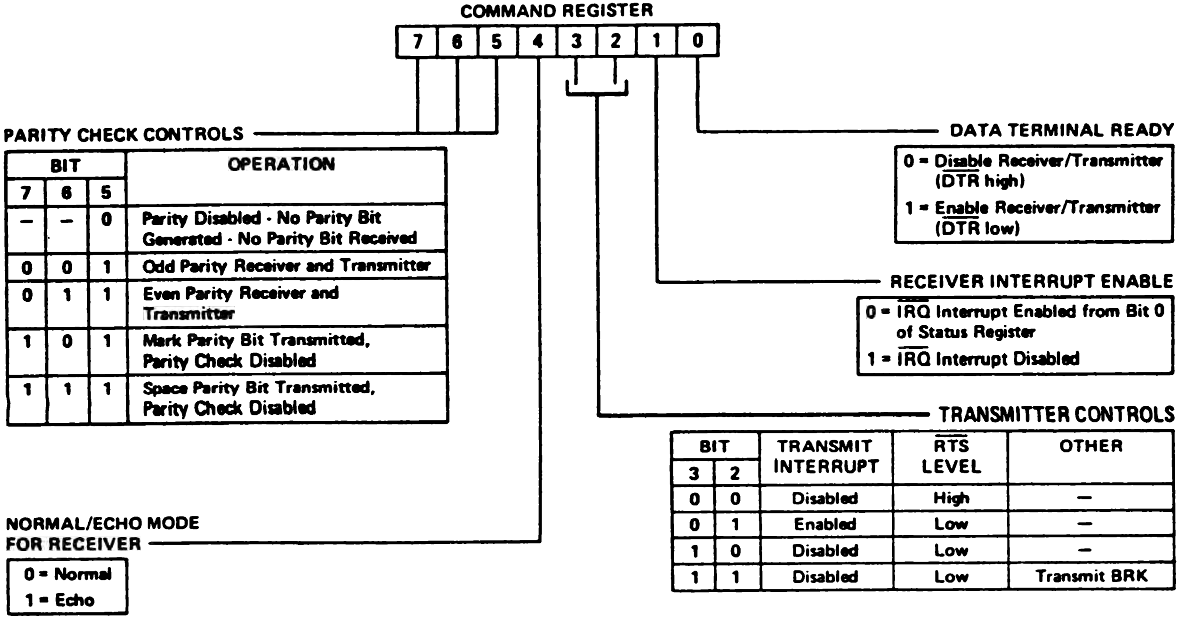
	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

Figure 6. Control Register Format

COMMAND REGISTER

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

C0F2



PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
–	–	0	Parity Disabled - No Parity Bit Generated - No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

DATA TERMINAL READY

0 = Disable Receiver/Transmitter ($\overline{DTR}$ high)
1 = Enable Receiver/Transmitter ($\overline{DTR}$ low)

RECEIVER INTERRUPT ENABLE

0 = $\overline{IRQ}$ Interrupt Enabled from Bit 0 of Status Register
1 = $\overline{IRQ}$ Interrupt Disabled

TRANSMITTER CONTROLS

BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	OTHER
0	0	Disabled	High	–
0	1	Enabled	Low	–
1	0	Disabled	Low	–
1	1	Disabled	Low	Transmit BRK

NORMAL/ECHO MODE FOR RECEIVER

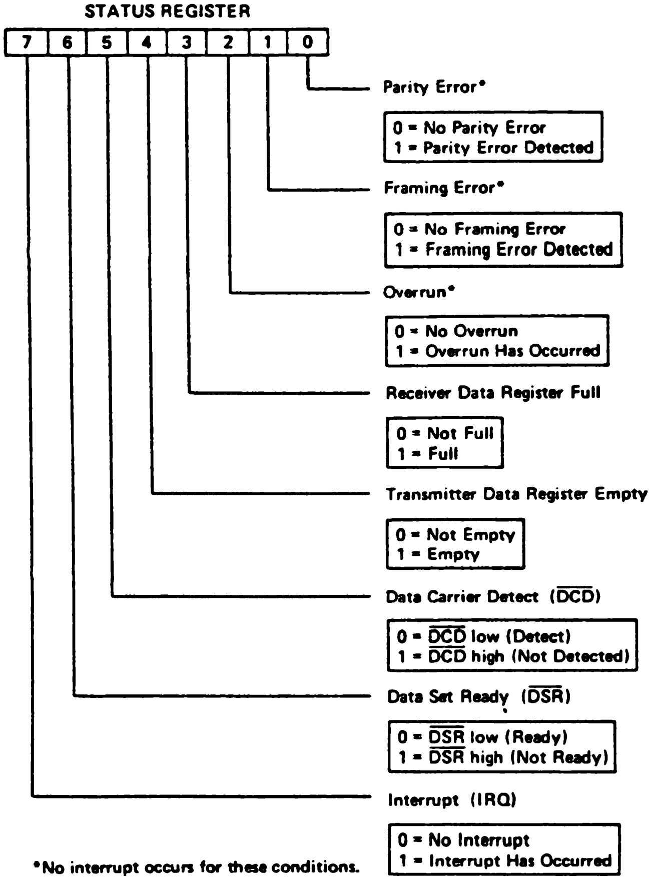
0 = Normal
1 = Echo

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	1	0
PROGRAM RESET	–	–	–	0	0	0	1	0

Figure 7. Command Register Format

STATUS REGISTER C0F1

The Status Register is used to indicate to the processor the status of various SY6551 functions and is outlined in Figure 8.

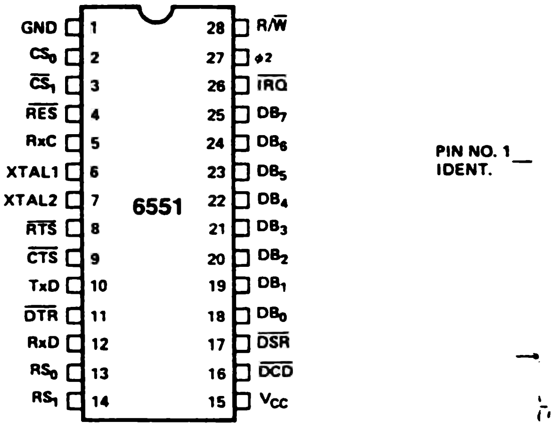

STATUS REGISTER
7
6
5
4
3
2
1
0
Parity Error*
0 = No Parity Error
1 = Parity Error Detected
Framing Error*
0 = No Framing Error
1 = Framing Error Detected
Overrun*
0 = No Overrun
1 = Overrun Has Occurred
Receiver Data Register Full
0 = Not Full
1 = Full
Transmitter Data Register Empty
0 = Not Empty
1 = Empty
Data Carrier Detect ($\overline{DCD}$)
0 = $\overline{DCD}$ low (Detect)
1 = $\overline{DCD}$ high (Not Detected)
Data Set Ready ($\overline{DSR}$)
0 = $\overline{DSR}$ low (Ready)
1 = $\overline{DSR}$ high (Not Ready)
Interrupt (IRQ)
0 = No Interrupt
1 = Interrupt Has Occurred

*No interrupt occurs for these conditions.

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

Figure 8. Status Register Format

PIN CONFIGURATION



SYSTEM CLOCKS & TIMING

MAIN CLOCK (C14M)

The Apple /// has as its master clock a 14 megahertz crystal controlled oscillator. The active components of the clock circuitry are Q10, Q11, and Y1. The exact frequency of the oscillator is 14.318 MHz. The slight increase over 14 MHz is compensated for in other logic. Device B13 provides buffering and power amplification to drive all the other loads on the C14M and C14M* lines.

FREQUENCY DIVIDER

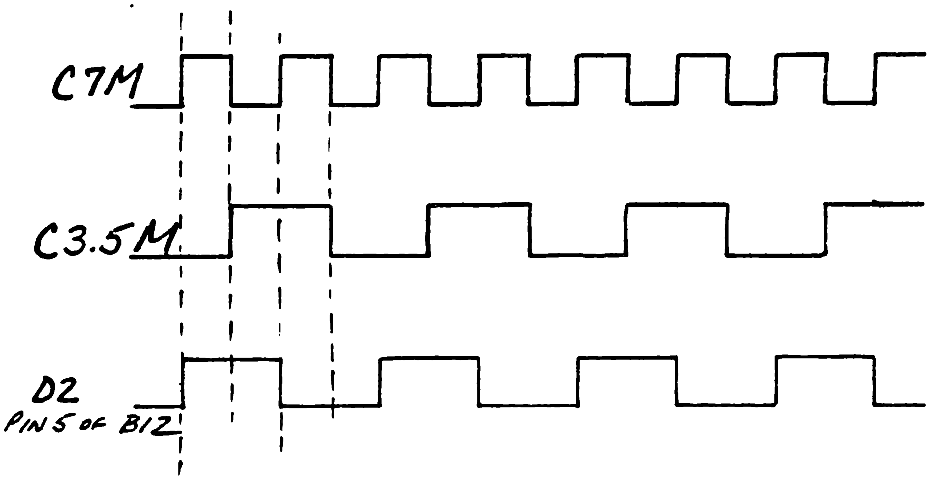
The next circuit in the system clock section is the frequency divider formed by device B12 and B13. This develops both the C7M* and the C3.5M*.

The C7M signal is developed by clocking the Q* output into the data input of a D-type latch. This results in a divide-by-two function of the clock frequency.

The C3.5M clock is developed in the same manner. However, the data input to the latch is an Exclusive-Or function of C7M and C3.5M at B13. This accomplishes two functions:

- it divides the C14M clock by 4, and
- it gives a definite phase relationship of C7M to C3.5M clocks.

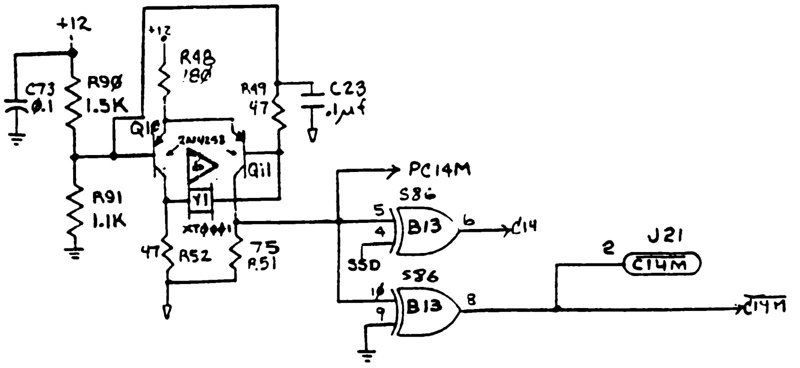
Looking at the timing diagram below we see that the D2 input of B12 is high if either the C7M or the C3.5 clock is high but not when both are high. This function is effectively at 3.5 MHz which toggles on the positive edge of the 7MHz clock. The true C3.5M signal toggles on the negative edge of the C7M clock.



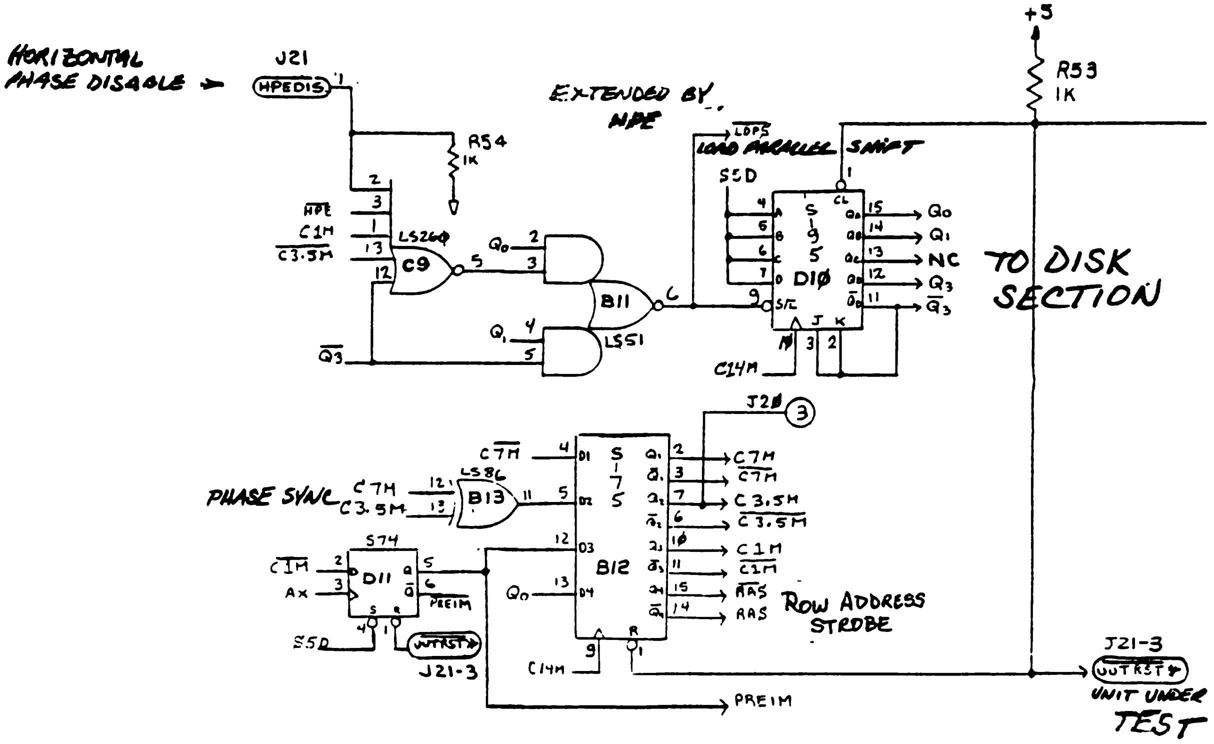
"Q" TIMING

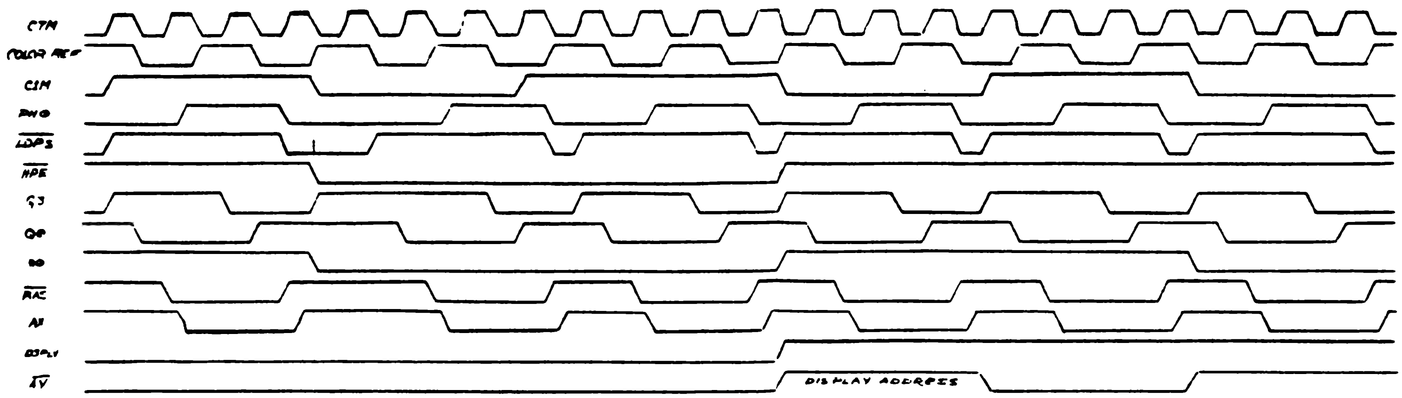
The Q clocks are a series of 2 MHz clocks which are out of phase with one another by one clock time (refer to the Apple /// Timing diagrams). The rest of the system timing depends on the states of the "Q" outputs. They provide the basis

MAIN CLOCK - 14MHz

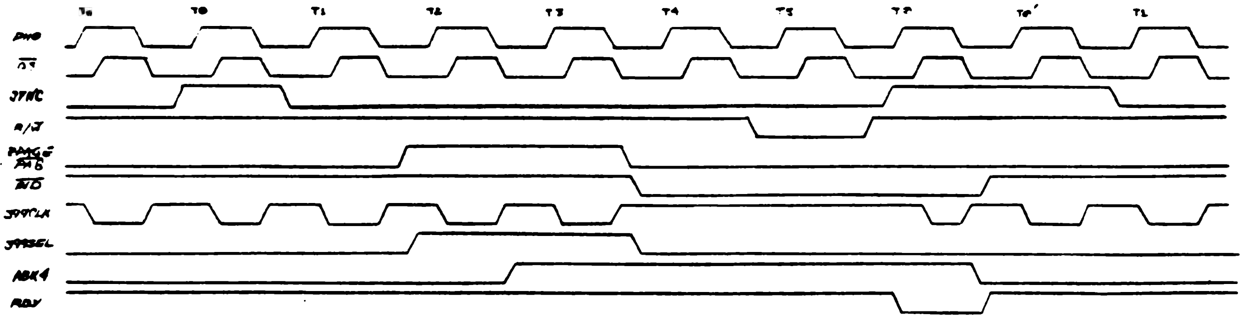


FREQUENCY DIVIDER.

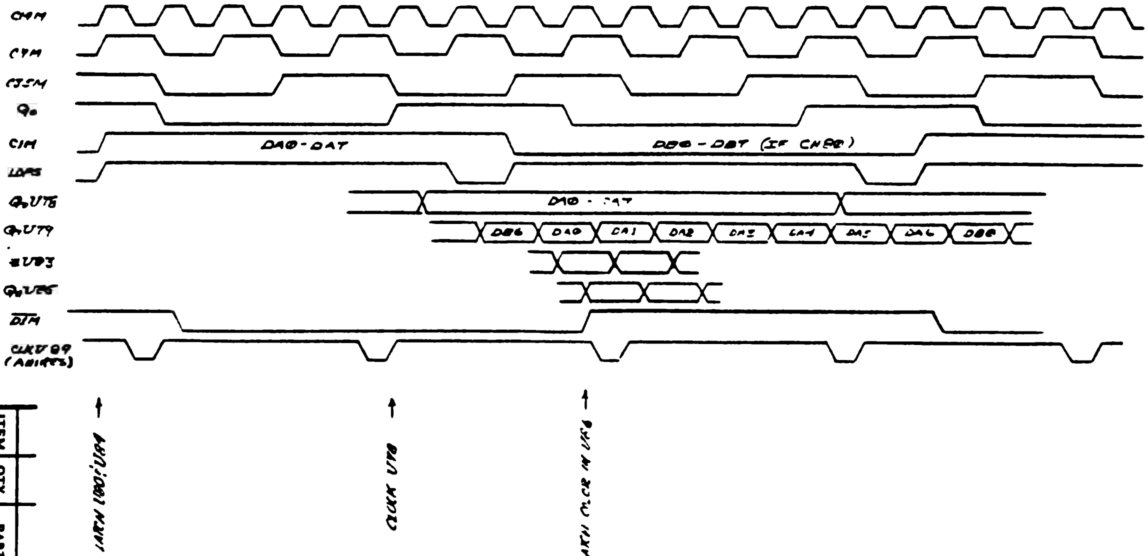




EXTRA HPE CYCLE & DISPLAY TIMING



INDIRECT ADDRESS TIMING



VIDEO SIGNALS

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

NEXT ASSY.

FINISH:

MATERIAL:

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ___
.XX ± ___
.XXX ± ___
ANGLES ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESIS
ARE IN MILLIMETERS.

ITEM | QTY | PART NUMBER | DESCRIPTION

DRAWN BY DATE
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer

TITLE

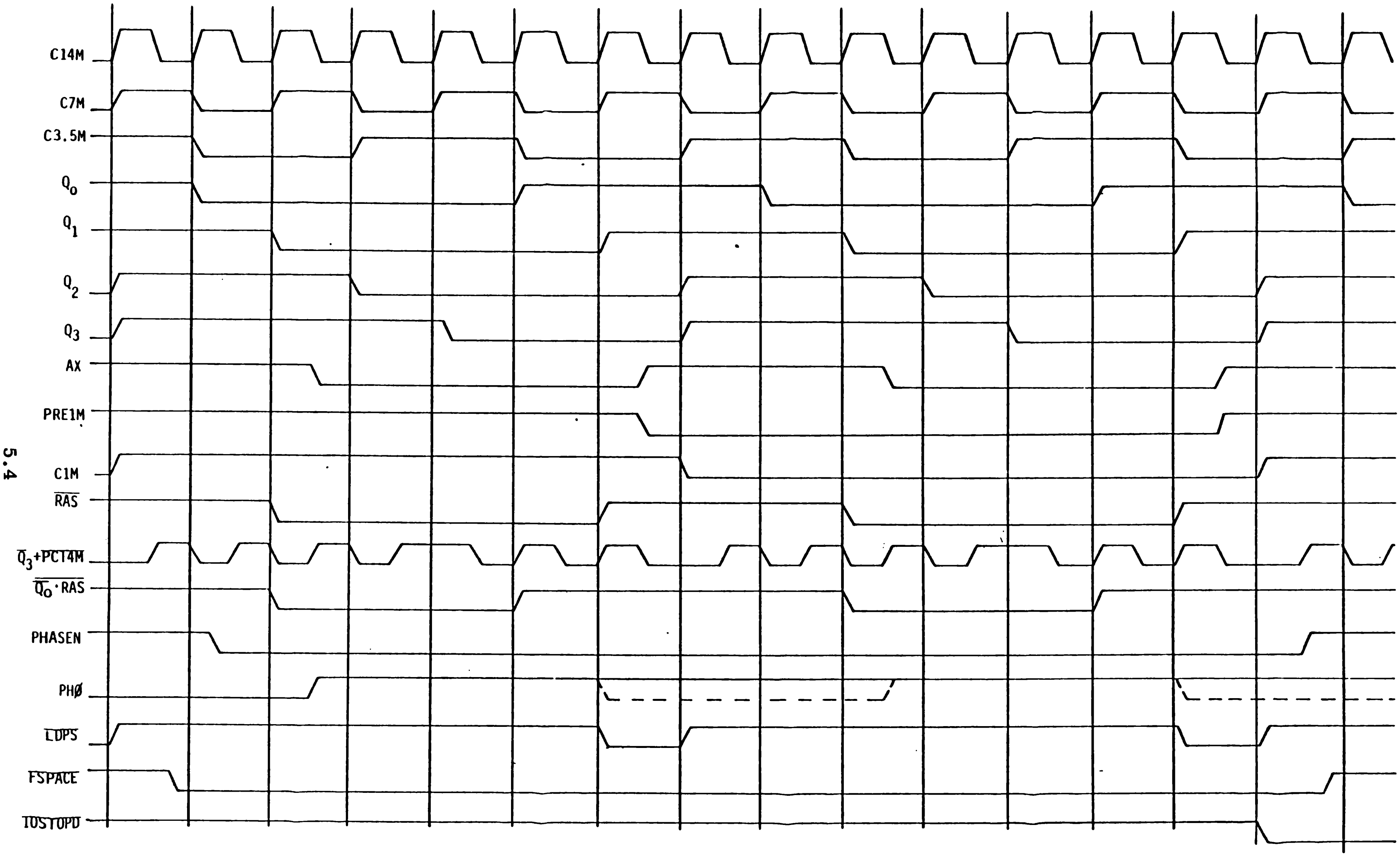
A /// SYSTEM TIMING

SIZE C

DRAWING NUMBER

SCALE:

SHEET



APPLE III TIMING

for processor and RAM address timing.

The Q clocks are initialized with each Load Parallel to Serial pulse (LDPS), which changes the mode of the LS195 (D10) from a shift register to a parallel loaded register when low. At each load, all of the bits are set high. When LDPS* returns high the next clock will shift the zero of Q3* across the register. This means that Q0 will stay high for one clock cycle. Q1 will stay high for 2 clocks, etc. When the Q3* goes high at the forth clock edge after LDPS the JK input will now see a "1". Subsequent clocks will start shifting that one across the register. When Q1 goes high again, LDPS* will be enabled low and another load will be accomplished at the next clock edge. The waveforms are assymmetrical. Each of Q0-Q2 are up for three clocks and down for four. Q3 is up for four and down for three.

This type of cycling will continue for 128 cycles. Then the Horizontal Phase Disable (HPE*) "freeze" will occur.

HPE* FREEZE

The HPE* signal will cause the Q states to extend their next cycle by two clock times. The purpose of the shift is to shift the phase of the color reference signals to the data in the video generator. A detailed discussion of this phenomenon is described in the video generator section. How this shift occurs is discussed below.

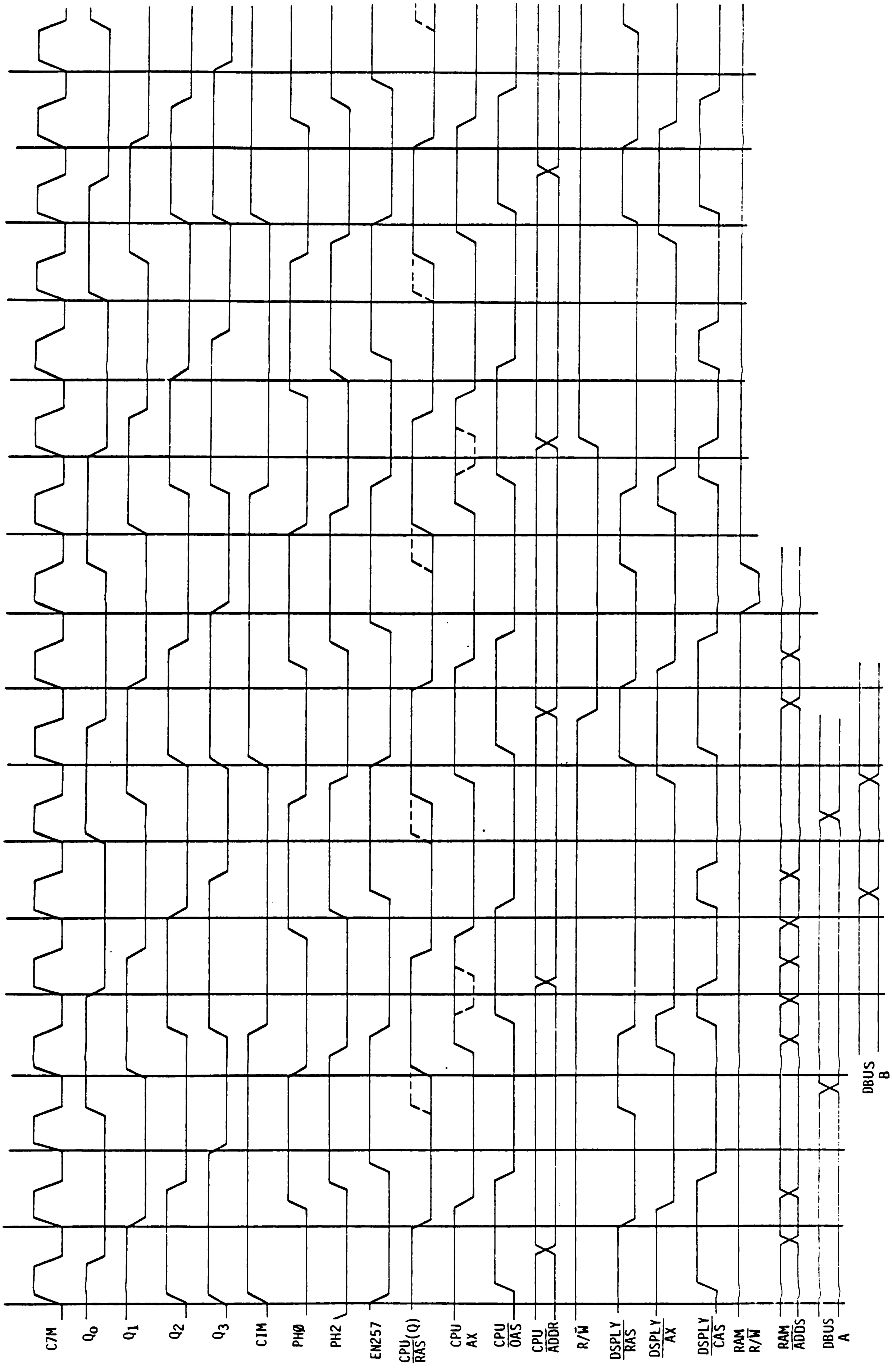
Looking at the gate array of C9 and B11 we see that since HPE* is normally high, the output of C9 is normally low. This de-gates the And inut shared with Q0, and allows LDPS to function as usual. But when HPE* goes low, which will always coincide with C14M going low, the And gate shared with Q0 will become enabled and cause the extension of the LDPS* for two extra clock cycles. This state will exist until C3.5M returns high and relieves LDPS*. The next clock will change the state of Q0 and that will not be able to "disrupt" the clocks until the next HPE pulse.

AX, PRE1M, & C1M

The AX, RAM address (the signal used to select which addressing source [row or column] is presented to the RAMs: see RAM Address Logic) is another 2 Mhz signal which lags Q1 by one half clock cycles. It is developed at A11 pin 9.

PRE1M can toggle at each positive edge of AX, if the data input to the latch is at the opposite state. Looking at D11 (C1M*) we will be able to see just that. If PRE1M has just toggled low, one half clock cycle later C1M* will toggle high which forms the data input to the PRE1M Flip-Flop. But remember, the clock to the flip-flop is AX, a 2 MHz signal. D11 pin 5 acts much like B12 pin 2 in that the data is always opposite to the "Q" output of the latch at the time of the clock edge, therefore we have a "clock divided by 2" function, of a 1 MHZ output.

RAS (Row Address Strobe)


C7M
Q0
Q1
Q2
Q3
C1M
PHØ
PH2
EN257
CPU RAS(Q)
CPU AX
CPU OAS
CPU ADDR
R/W
DSPLY RAS
DSPLY AX
DSPLY CAS
RAM R/W
RAM ADDS
DBUS A
DBUS B

The RAS signal is Q0 delayed by one clock and inverted. This is acccomplished at D10 pin 15 & 14. (Note: the inversion is done by calling the "Q" output the active low signal RAS*, clever huh?) RAS is used in the RAM address logic to develop the "row select" signals for the RAMs.

VIDEO HORIZONTAL & VERTICAL STATE COUNTERS

This circuit is made up of four 4-bit binary counters, (F10, F11, G11, G12), which develop the essential signals for partitioning the screen and addressing the RAM for all the video data.

Basically, there are two sections of the circuit:

1 - horizontal postion counter

2- vertical position counter

These two counters form the X and Y coordinates of each addressable byte on the screen. Each byte contains 7 bits or dots in 40 character modes.

From the various discussions about the Apple ///, we have learned that in the 40 character mode there are 280 dots across the horizontal line that can be defined, and 192 of these horizontal line (280 X 192). In the Apple /// modes there are 560 dots in the horizontal line, however, there are still only 192 horizontal lines (560 X 192).

The Video Counter works identically in either of these modes. It provides the resolution of 40 by 192 matrix. Each one of the 40 horizontal positions defines either 7 or 14 dots (40 or 80 character modes, respectively). These dots are actually bits of data bytes in memory that are parallel loadedd into a shift register and shifted out serially to the video monitor. In the 40 character modes the system loads the shift register at a 1 MHz rate and shifts at a 7 MHz rate. In the 80 character modes it loads at a 2 MHz rate and shifts at a 14 Mhz rate. It is interesting to note that in either mode the state counter increments at a 1 Mhz rate.

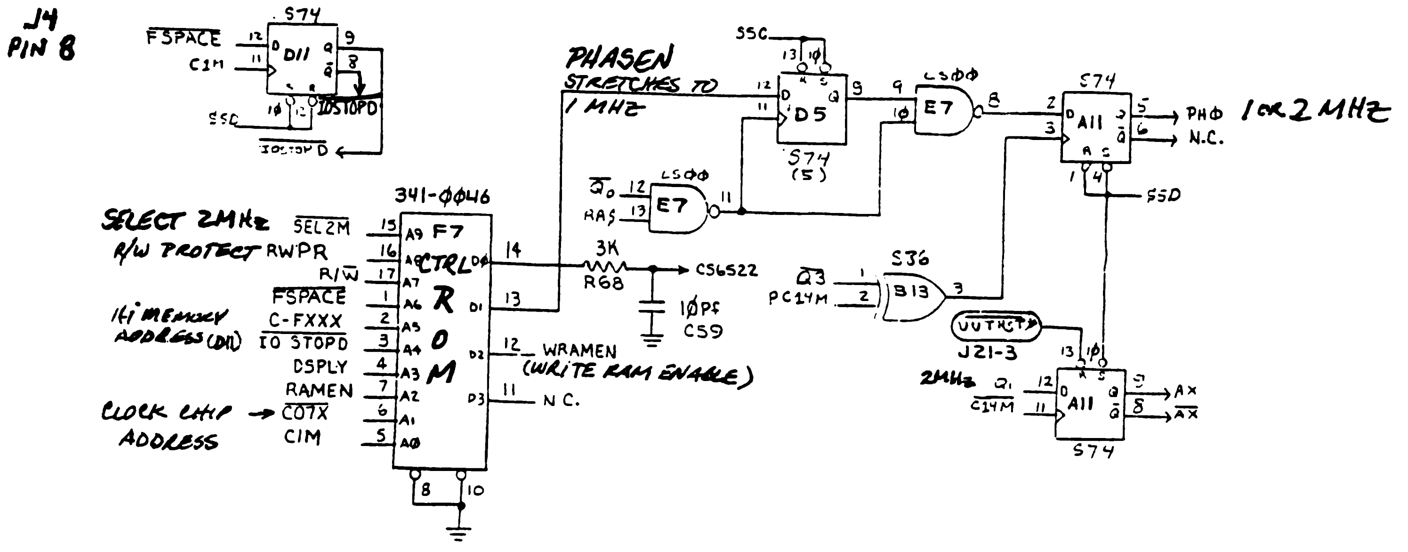
The system provides two complete accesses for the video output per increment of the state counter, but in the 40 character modes one of these are masked out.

HORIZONTAL SECTION

The Horizontal section of the state counter uses 7 of the counter stages and develops the H0 through H5 and the HPE* signals. The remaining 9 stages of the counter develop the Vertical states VA, VB, VC, and V0 through V5.

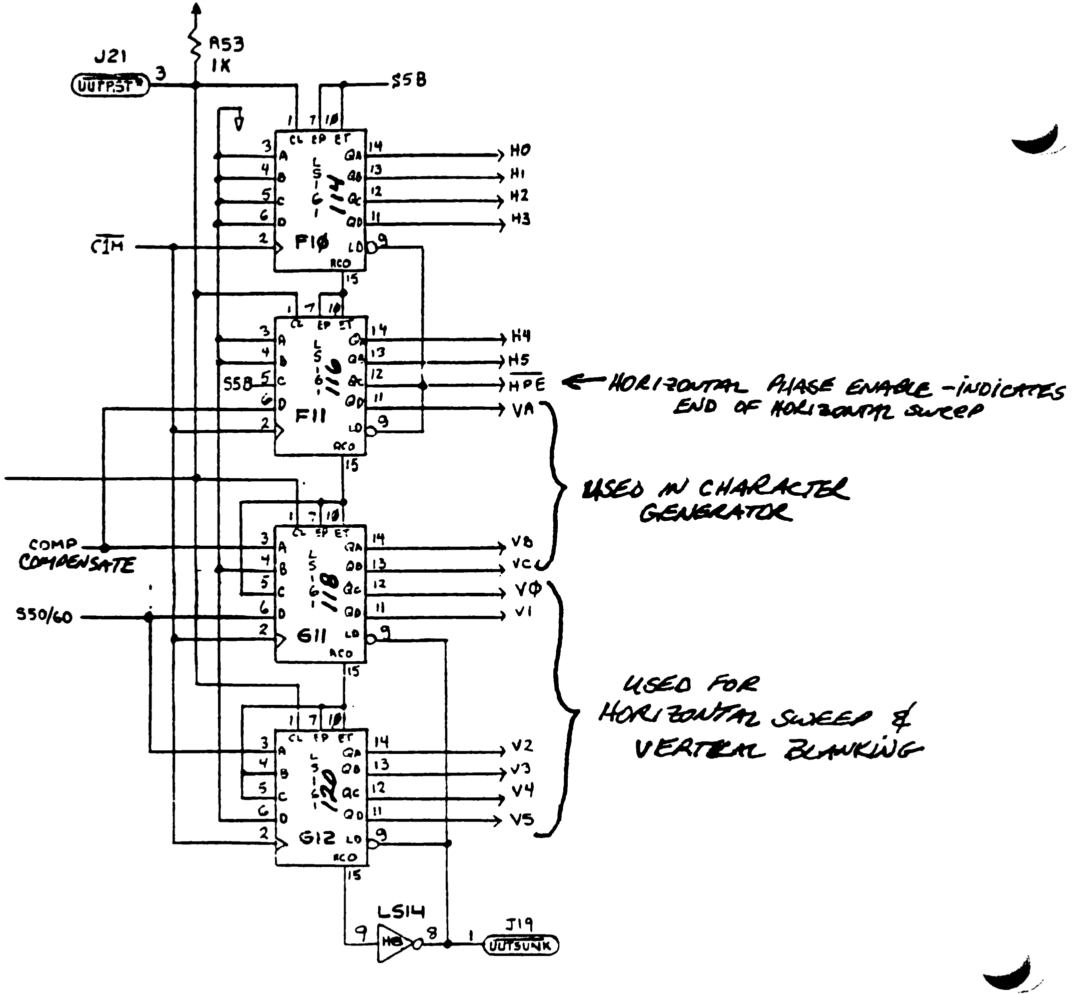
The Horizontal section provides the capability of a 128 state counter, however, it only provides 65 states. This is due to the action of the most significant stage, HPE*. The counter actually counts from 64 to 128 then resets to count 64. Simply, HPE* starts high and when the counter increments HPE* low after 64 counts it is then reset to state 64 after the next clock input, this yields

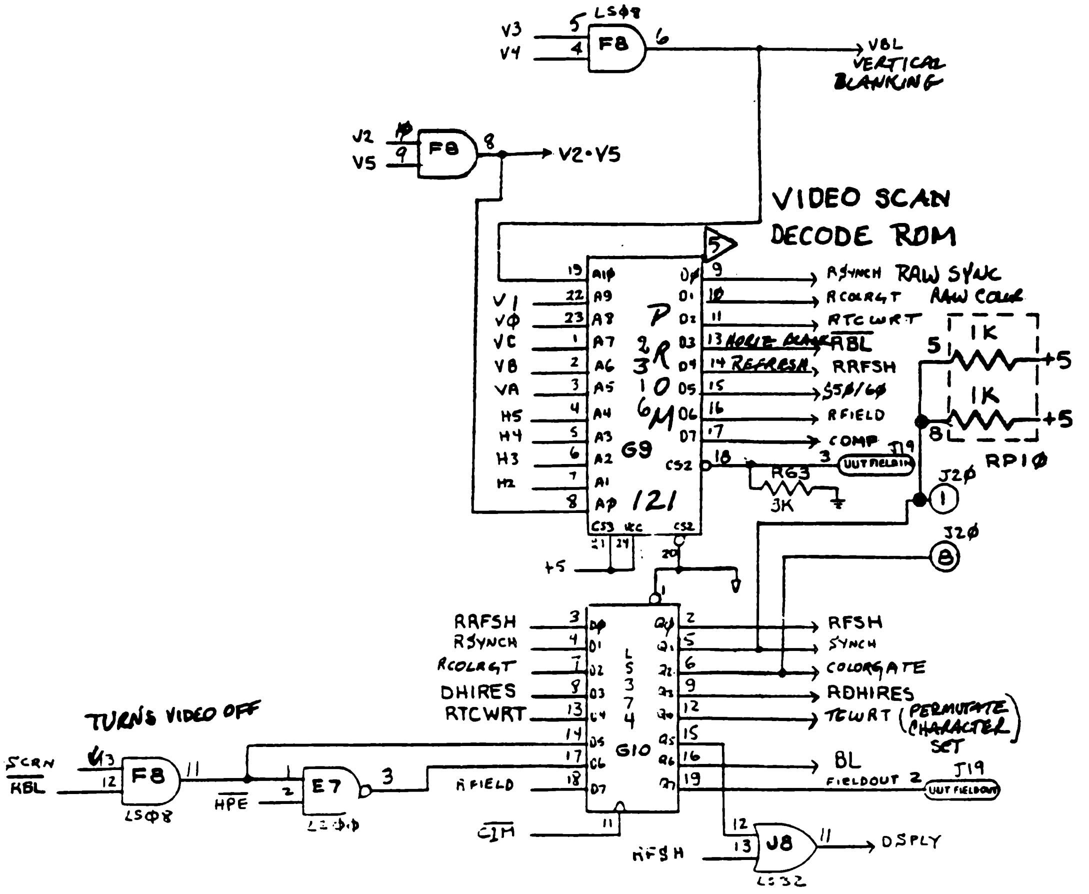
1 TO 2 MHz GEARSHIFT



$\overline{\text{FSPACE}}$ - RESULTS WHEN YOU ADDRESS THE VIA'S, THE ACIA, OR THE INTERNAL CLOCK (C07X)

VIDEO STATE COUNTER




LS08
V3
V4
F8
VBL
VERTICAL BLANKING
V2
V5
F8
V2•V5
VIDEO SCAN
DECODE ROM
5
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
V1
V0
VC
VB
VA
H5
H4
H3
H2
P
2
R
3
10
6
M
G9
121
CS3
VCC
CS2
+5
D0
D1
D2
D3
D4
D5
D6
D7
CS2
RSYNCH
RAW SYNC
RCOLRGT
RAW COLOR
RTCWRT
~~HORIZ BLANK~~ RBL
~~REFRESH~~ RRFSH
S50/60
RFIELD
COMP
J19
UUT FIELD IN
R63
3K
1K
1K
+5
+5
RP10
J20
1
J20
8
RRFSH
RSYNCH
RCOLRGT
DHIRES
RTCWRT
LS374
G10
RFSH
SYNCH
COLORGATE
RDHIRES
TCWRT (PERMUTATE CHARACTER SET)
BL
FIELDOUT 2
J19
UUT FIELDOUT
TURNS VIDEO OFF
SCRN
RBL
F8
LS08
HPE
E7
LS00
RFIELD
C1M
RFSH
J8
LS32
DSPLY

65 states all together.

Looking at F11 we see that the HPE* output is connected to the "load" input of F10 and F11. At the next clock input these two devices will be loaded with the state determined by what is on the data inputs. All inputs except pin 5 of F11 are tied low (disregard the input to pin 6 of F11 at this time). This binary state equals 64. So rather than starting back at "zero" the counter jumps to 64.

For real time considerations of the monitor, it takes 25 states or 25 microseconds for the sweep to return from the right hand side to the left side. So the system ignores the first 25 states and blanks the video output and the returning trace is not shown. The boolean expression for the horizontal blanking would be expressed:

(H4* and H5*) or (H4 and H3*)

This logical function is done within the G9 Control ROM. Refer to page 10 of 10 of the schematic diagram.

In summary, the horizontal counter provides the address necessary for the display. It divides the horizontal line into forty (40) sections, and yields the timing for horizontal blanking. The HPE* signal is used to momentarily "freeze" some of the system timing.

VERTICAL SECTION

The Vertical State Counter provides the Y-axis of the display matrix. The nine stages, if left alone to count, would provide 512 states. As in the horizontal counter, it is preset to count higher than zero eadch time it reaches the "terminal count". Also, some of the states are used to blank the video while the trace returns from the bottom of the screen to the top (VBL).

The vertical counter effectively counts the number of HPE*'s that have occurred, or simply, the number of horizontal lines that have been generated in this scan.

At this time the counter is reset to count 250. Look at the timing diagram of the vertical counter. One can see that all vertical signals would normally go low, but instead the counter is loaded with the data inputs. VA will not be affected by the teminal count/load and will continue as discussed before. VB will be loaded to the present state of "comp" (or VA) which is high. VC and V5 will be loaded to a low and the rest of the bit states wil be loaded to "1". This will decode to decimal 250.

Six counts later VA through V4 will toggle low and V5 will toggle high. This is the point where the logic assumes to be at scan line "zero". It will now take 256 counts to reach the terminal count sequence and start again. Using some math we see that the counter defines 262 states (256+6 = 262).

Vertical blanking takes 70 of the 262 states developed by the counter. The boolean expresssion for the vertical blanking signal would be:

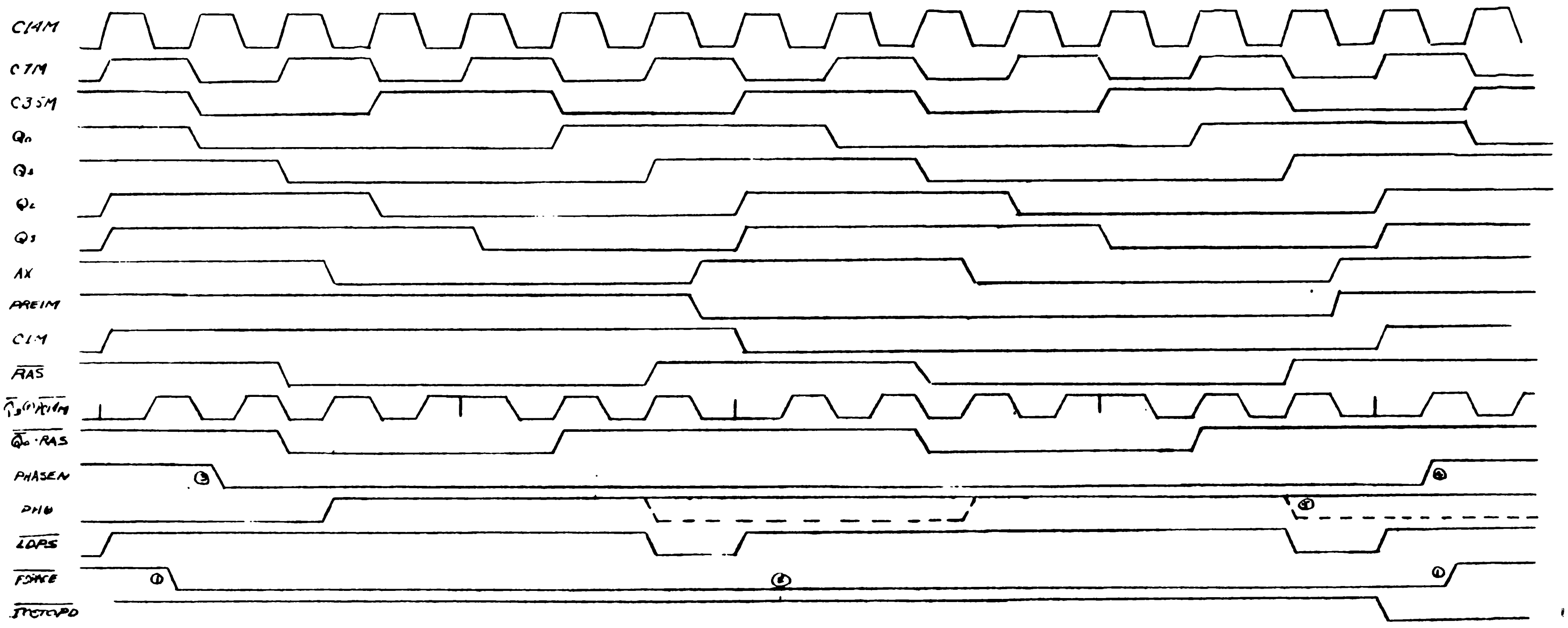
(V3 and V4)

This signal is developed at F8 pin 6 and is used in the system to indicate that a complete scan of the current display page has occurred. It is also an input to the Control Rom, G9, and therefore is a modifier to its outputs.

We were looking for the majic number of 192. Well, if you´ve been keeping track, it´s simply the difference of 272-70.

REV.	ZONE	ECO #	REVISION

NOTE: UNLESS OTHERWISE SPECIFIED



APPLE /// SYSTEM TIMING

① ADDRESS TIME FROM PHØ
② FSPIKE MAINTAINED BY PHØ STRETCH
③ PHASEN CASE: SEL2M·$\overline{IOSTOPD}$·FSPIKE
④ PHASEN GOES HIGH DUE TO $\overline{IOSTOPD}$
⑤ PHØ HELD HIGH ANOTHER CYCLE
TO SYNCH 6522'S TO C1M

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ±
.XX ±
.XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS
ARE IN MILLIMETERS

DRAWN BY DATE
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple compu

TITLE APPLE /// TIMI

MATERIAL:

NEXT ASSY.

FINISH:

SIZE B

DRAWING NUMB

SCALE:

SHEET

DISPLAY MODES

- 40 CHARACTER APPLE II : 40x24 CHARACTER B/W TEXT (2K BYTES RAM)
- 40 CHARACTER APPLE ///: 40x24 CHARACTER COLOR TEXT - 16 BACKGROUND, 16 TEXT COLORS
- 80 CHARACTER BLACK & WHITE APPLE ///: 80x24 CHARACTER B/W TEXT
- BLACK & WHITE HIRES: 280x192 B/W HIRES (8K RAM)
- MEDIUM RESOLUTION 16 COLOR GRAPHICS APPLE ///: 280x192 16 COLOR HIRES WITH 40x192 BACKGROUND/FOREGROUND RESOLUTION
- SUPER HIRES APPLE ///: 560x192 B/W HIRES
- APPLE /// HIRES: 140x192 16-COLOR HIRES
- RAM CHARACTER GENERATOR (128 CHARACTER)

APPLE /// VIDEO

INTRODUCTION

The Apple /// has 11 defined video modes of operation. There are 5 Apple][modes and 6 new Apple /// modes. There are now 3 text modes and 8 graphics modes. Though the Apple /// can emulate all of the Apple][video modes, there are many differences in the video hardware between the Apple][and Apple ///, including:

- o 80 column text with full upper and lower case character capability
- o New color text mode
- o Super high resolution black and white graphics
- o 2 new color hires modes

AND

- o A modifiable character set

The modifiable character set is a major new feature of the Apple ///. You can now change the character set by changing the pattern in the character generator. This is possible because of a ram, instead of a fixed rom configuration.

There are also improved video outputs. An NTSC (National Television Standards Committee) composite Black and White and color composite, plus the primary video signals, are available at the back panel for mixing into the input of a high quality RBG monitor.

The Apple][emulation mode has the very same video modes as the Apple][. The Apple ///, while in its native mode, can have the following modes.

40 Character Apple][

This mode is equivalent to the Apple][text mode. The only difference is it has upper and lower characters.

- o The screen is divided into 40 horizontal columns and 24 vertical lines.
- o The characters are usually white dots on a black background.
- o This mode has inverse video and flashing characteristics.
- o This mode has no color.

- This mode has two screen pages mapped into memory:
  - Page 1 is located at 0400-07FF
  - Page 2 is located at 0800-0BFF.

40 Character Apple ///

This second 40 character text mode is the most interesting and, in a way, the most powerful. This is the only color text mode. It has the same screen resolution as the Apple][, and the same video attributes. BUT it also has the ability to select both the color of the foreground (dots) and the color of the background. Sixteen (16) colors are available as in the Apple][Lores Graphics.

- The color resolution can be selected for each character and can change for each character.
- It is interesting to note that by down loading a character set, a new low resolution graphics mode can be manufactured from a text mode.

The page mode is different for this mode since both pages are used at once. Why? Because the first page contains the character data and the second page contains the color information. The page 2 mode reverses the mapping, that is, the characters in page 2 are stored where the color was stored in page 1, and vice versa.

In the color byte, bits 4-7 set the foreground color and bits 0-3 set the background color. The mapping between color and character is 1:1. That is, a character located in 0409, for example, has its foreground color determined by the byte in location 0809.

In the page 1 mode the mapping is as follows:

0400-07FF contain the characters

0800-0BFF contain the color information.

In the page 2 mode:

0800-0BFF contain the characters.

0400-07FF contains the color.

80 Character Black & White Apple ///

This new text mode is the same as the 40 column mode with the obvious exception that it has 80 columns instead of 40. This 80 column display has full upper and lower case, and inverse video.

Unlike the 40 character mode, it does not have 2 distinct pages. It uses both pages to hold the characters.

The memory mapping for Page 1 utilizes:

0400-07FF for the primary fetch

0800-0BFF for the secondary.

In this mode, location 0400 contains the first character and 0800 contains the second. The third and the fourth characters come from locations 0401 and 0801 respectively.

In the Page 2 mode the primary fetch is from 0800-0BFF and the secondary from 0400-07FF. Therefore, the first and third characters come from 0800 and 0801 and the second and fourth come from 0400 and 0401.

Black & White Hires

This is a new graphics mode that has a 280 by 192 resolution in Black and White only.

It has two distinct pages:

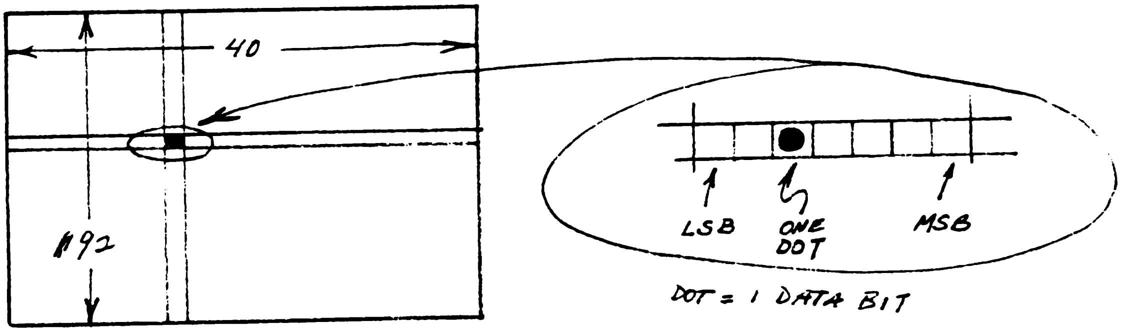
Page 1 is located at 2000-3FFF

Page 2 is located at 4000-5FFF.

Medium Resolution 16 Color Graphics Apple ///

This is a new graphics mode for the Apple ///. It has the same dot resolution as the Apple][Hires (280 by 192), but it has an expanded color capability of 16 background colors. The B/W Output will yield 16 levels of grey scale.

The screen is divided into a 40 wide by 192 high matrix. That is, the color selection for foreground and 16 background can change for each 7 dot [ooooooo] pixel segment. You can think of each segment as a one-bit-high slice across a character space, as illustrated below.



The memory mapping is as follows:

Page 1:	2000-3FFF	each byte represents 7 pixels in the segment
	4000-5FFF	each byte represents the foreground and background colors for the corresponding 2000-3FFF byte.
Page 2:	2000-3FFF	each byte represents the colors
	4000-5FFF	each byte represents 7 pixels.

Super Hires Apple ///

This is the Apple /// Hires equivalent of 80 character mode. It is a Black and White mode which has the dot resolution of 560 Horizontal by 192 vertical spaces.

There are two distinct screen pages, each with a primary and secondary page. Because it is like the 80 character modes, this mode draws its information from alternating ram. Each memory byte contributes 7 pixels. In Page 1 mode, the primary contains the odd dot groups and the secondary contains the even dot groups. The primary (first 7 pixels) is located at 2000-3FFF, and the secondary (second 7 pixels) is found at 4000-5FFF. In Page 2 the primary is at 6000-7FFF, and the secondary is 8000-9FFF.

In each byte the Most Significant Bit (MSB) is ignored and the data is displayed with the Least Significant Bit (LSB) first from left to right.

Apple /// Hires

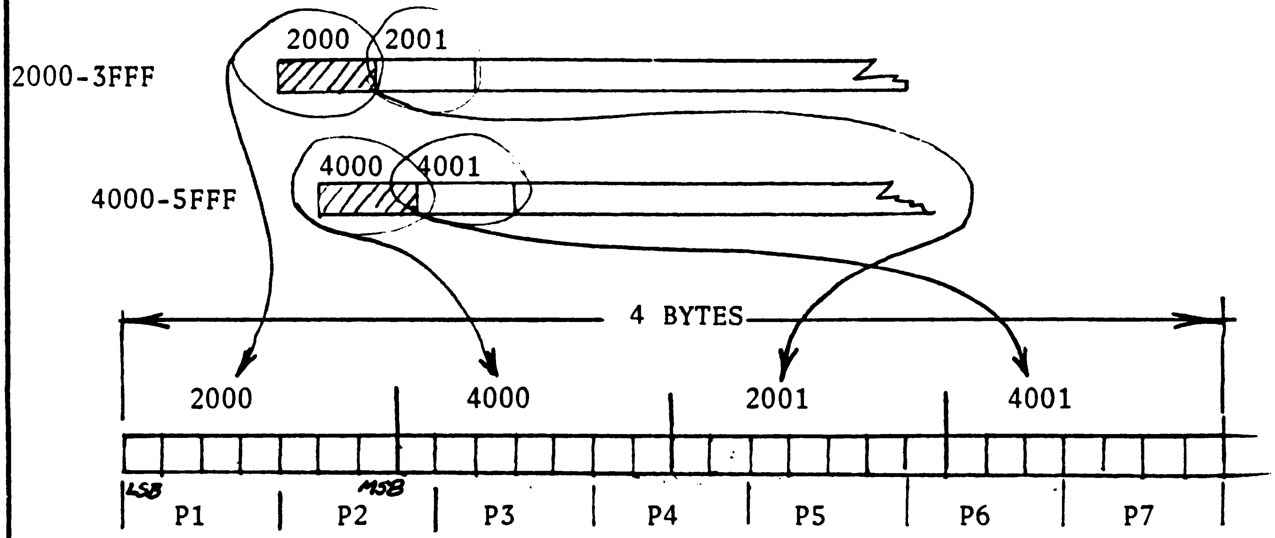
This is the third new graphics mode. It has 140 by 192 pixel resolution, and 1 of 16 color selection per pixel. In this mode the pixel is formed by a group of four dots of the same color.

There are two distinct screen pages in this mode but the mapping of the individual pages is, at first encounter, a bit difficult to master. Good luck!

- o The display dot represents a sequence of 4 data bits in the RAM display area.
- o Two rams are used starting at 2000 and 4000 respectively and alternate bytes are fetched from each ram area.

- In any video mode only 7 of the 8 bits of each byte are displayed.

With this information in mind...and remembering that each pixel in this mode is made from 4 bits...you can see that you need 4 bytes of information to get 7 pixels. The way in which these bytes map into picture elements is shown below.



4000-5FFF each byte represents 7 pixels.

Super Hires Apple ///

This is the Apple /// Hires equivalent of 80 character mode. It is a Black and White mode which has the dot resolution of 560 Horizontal by 192 vertical spaces.

There are two distinct screen pages, each with a primary and secondary page. Because it is like the 80 character modes, this mode draws its information from alternating ram. Each memory byte contributes 7 pixels. In Page 1 mode, the primary contains the odd dot groups and the secondary contains the even dot groups. The primary (first 7 pixels) is located at 2000-3FFF, and the secondary (second 7 pixels) is found at 4000-5FFF. In Page 2 the primary is at 6000-7FFF, and the secondary is 8000-9FFF.

In each byte the Most Significant Bit (MSB) is ignored and the data is displayed with the Least Significant Bit (LSB) first from left to right.

Apple /// Hires

This is the third new graphics mode. It has 140 by 192 pixel resolution, and 1 of 16 color selection per pixel. In this mode the pixel is formed by a group of four dots of the same color.

There are two distinct screen pages in this mode but the mapping of the individual pages is, at first encounter, a bit difficult to master. Good luck!

- The display dot represents a sequence of 4 data bits in the ram display area.
- Two rams are used starting at 2000 and 4000 respectively and alternate bytes are fetched from each ram area.
- In any video mode only 7 of the 8 bits of each byte are displayed.

With this information in mind...and remembering that each pixel in this mode is made from 4 bits...you can see that you need 4 bytes of information to get 7 pixels. The way in which these bytes map into picture elements is shown below.

It is apparent, from the diagram, that picture elements overlap the byte boundaries for 7 picture elements and 4 bytes. The basic pattern then repeats.

The four bytes are shifted out in a fashion similar to the other Apple /// modes:

- o The first byte comes from the primary and the second byte comes from the secondary.
- o The first byte contains the first pixel and the second byte comes from the secondary.
- o The first byte contains the first pixel and 3 bits of the second pixel.
- o The second byte contains the fourth bit of the second pixel, the third pixel, and the first two bits of the fourth pixel.
- o The third byte contains the last two bits of the fourth pixel, the fifth pixel, and the first bit of the sixth pixel.
- o The fourth byte contains the last three bits of the sixth pixel and the entire seventh pixel.

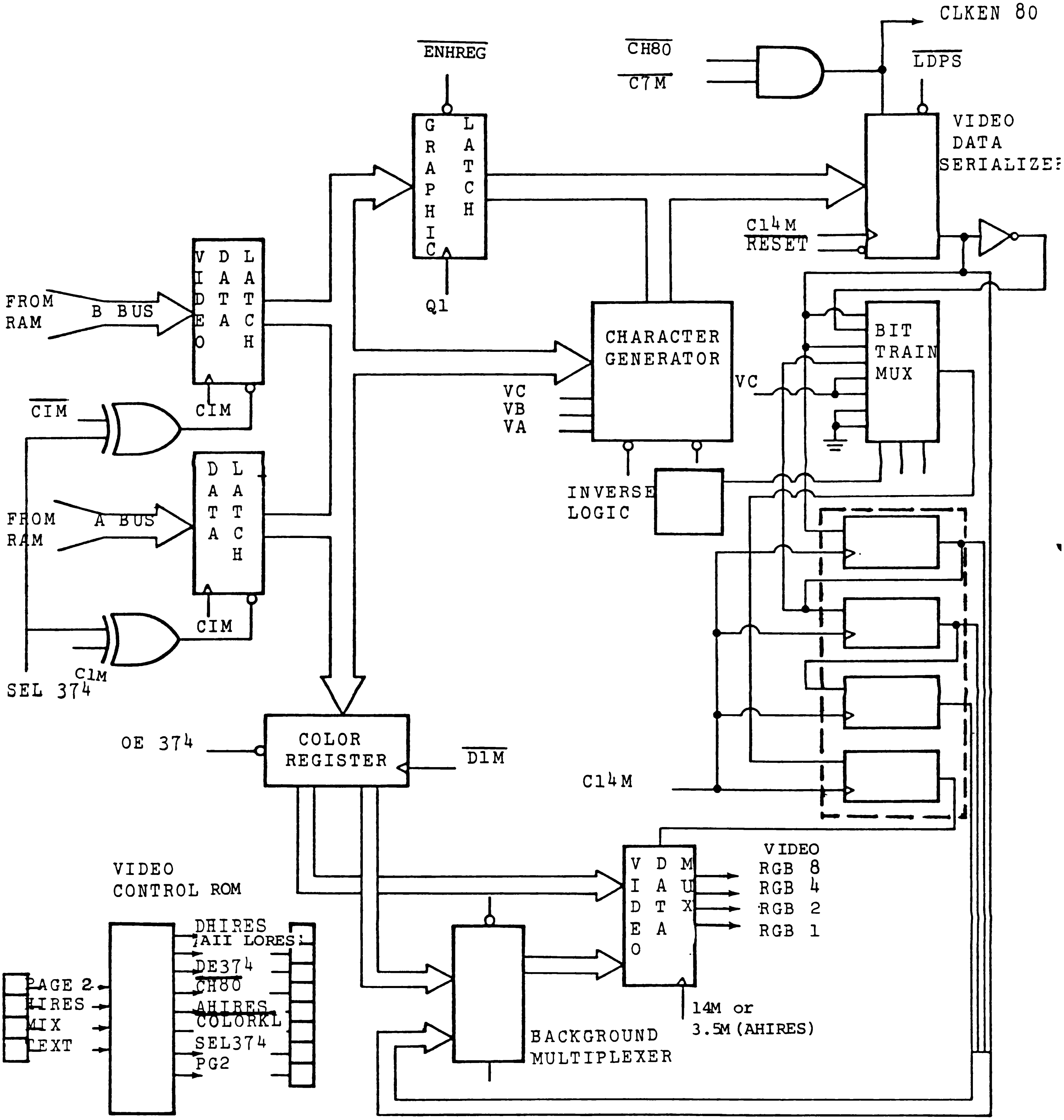
We hope the preceding diagram will help you picture what has already been described.

For this mode, Page 1 is mapped with the primary fetch in 2000-3FFF, and the secondary in 4000-5FFF. In Page 2 the primary is in 6000-7FFF, and the secondary is in 8000-7FFF.

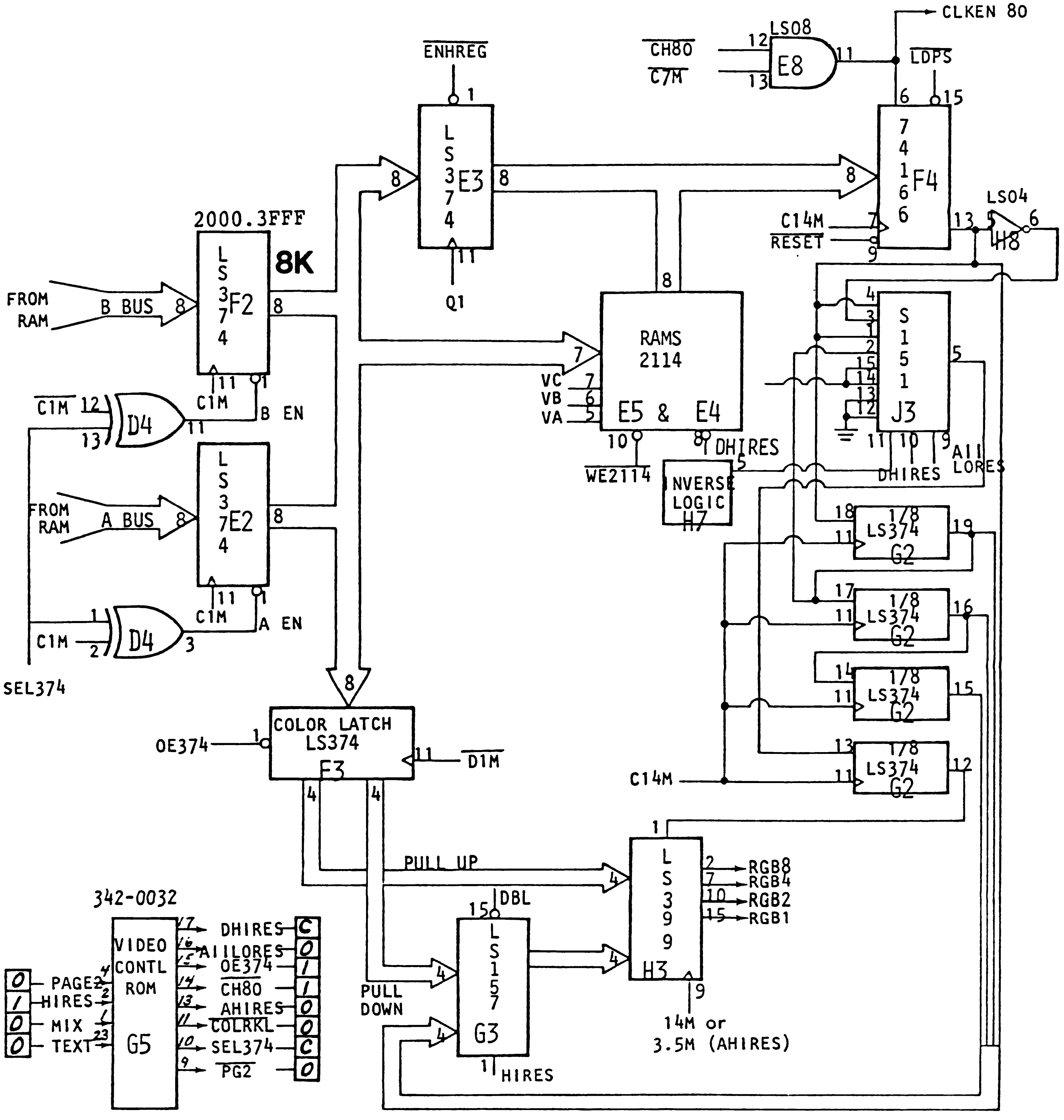
APPENDIX (VIDEO)

- o Apple /// Video Logic Block Diagram
- o Video Logic Diagrams for:
    1. Hires Mode Page 1, B/W 280 X 192
    2. Hires Mode Page 2, B/W 280 X 192
    3. Color Hires Mode Page 1, 280 X 192
    4. Color Hires Mode Page 2, 280 X 192
    5. Super Hires Mode Page 1, 560 X 192
    6. Super Hires Mode Page 2, 560 X 192
    7. Ahires Test Page 1, 140 X 192
    8. Ahires Test Page 2, 140 X 192
    9. Color Bar & Grey Scale Test
    10. Apple II Text Mode Page 1, B & W, 40 Column
    11. Apple II Test Mode Page 2, B & W, 40 Column
    12. Sara 40 Column Text Mode Test, 16 Colors
    13. Sara 80 Column Text Mode Test, B & W
- o Apple /// Video Modes Truth Tables
- o Video Prom Listing
- o Video Prom Equivalent Logic

APPLE III VIDEO LOGIC BLOCK DIAGRAM

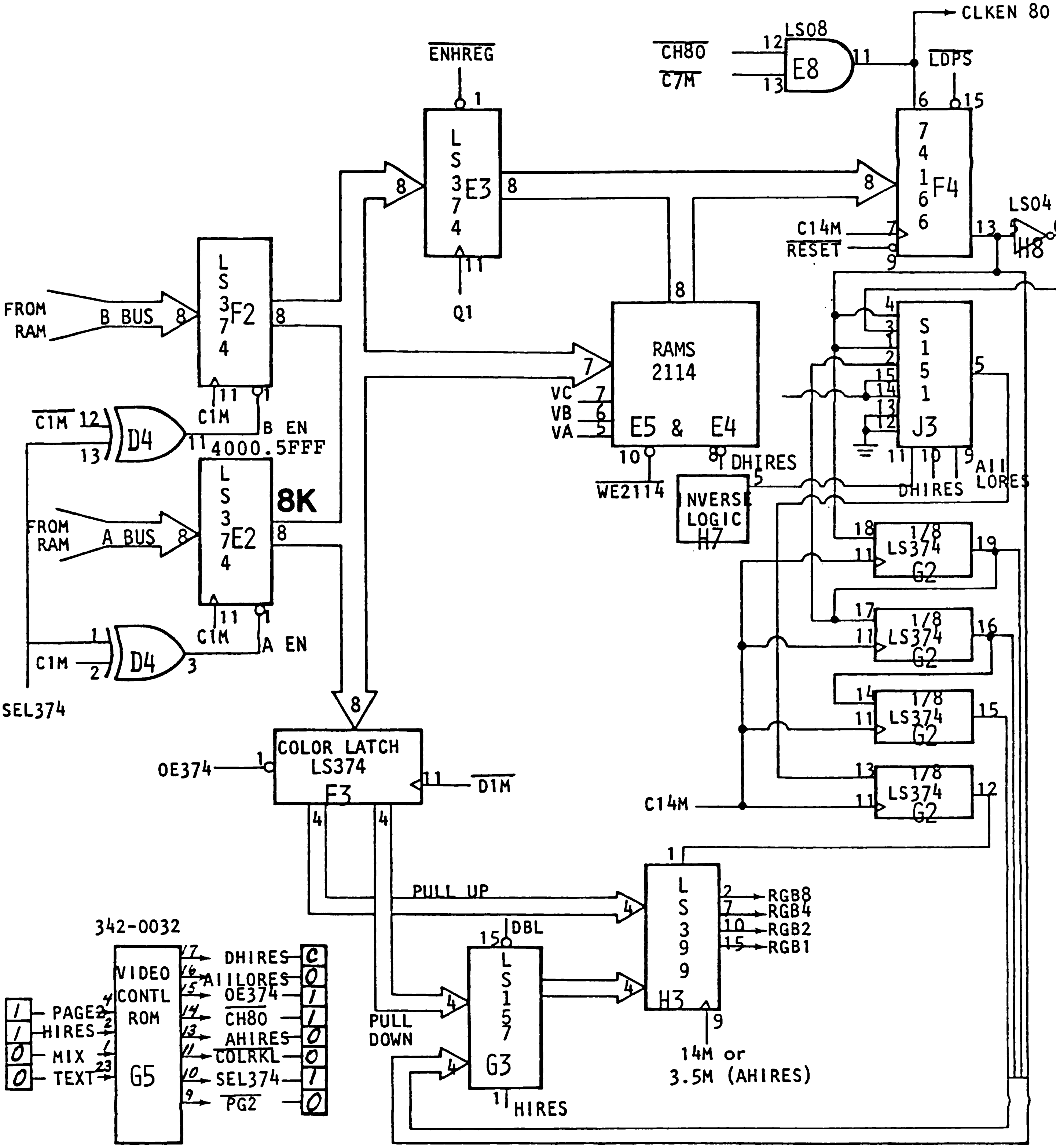


A/// VIDEO LOGIC DIAGRAM



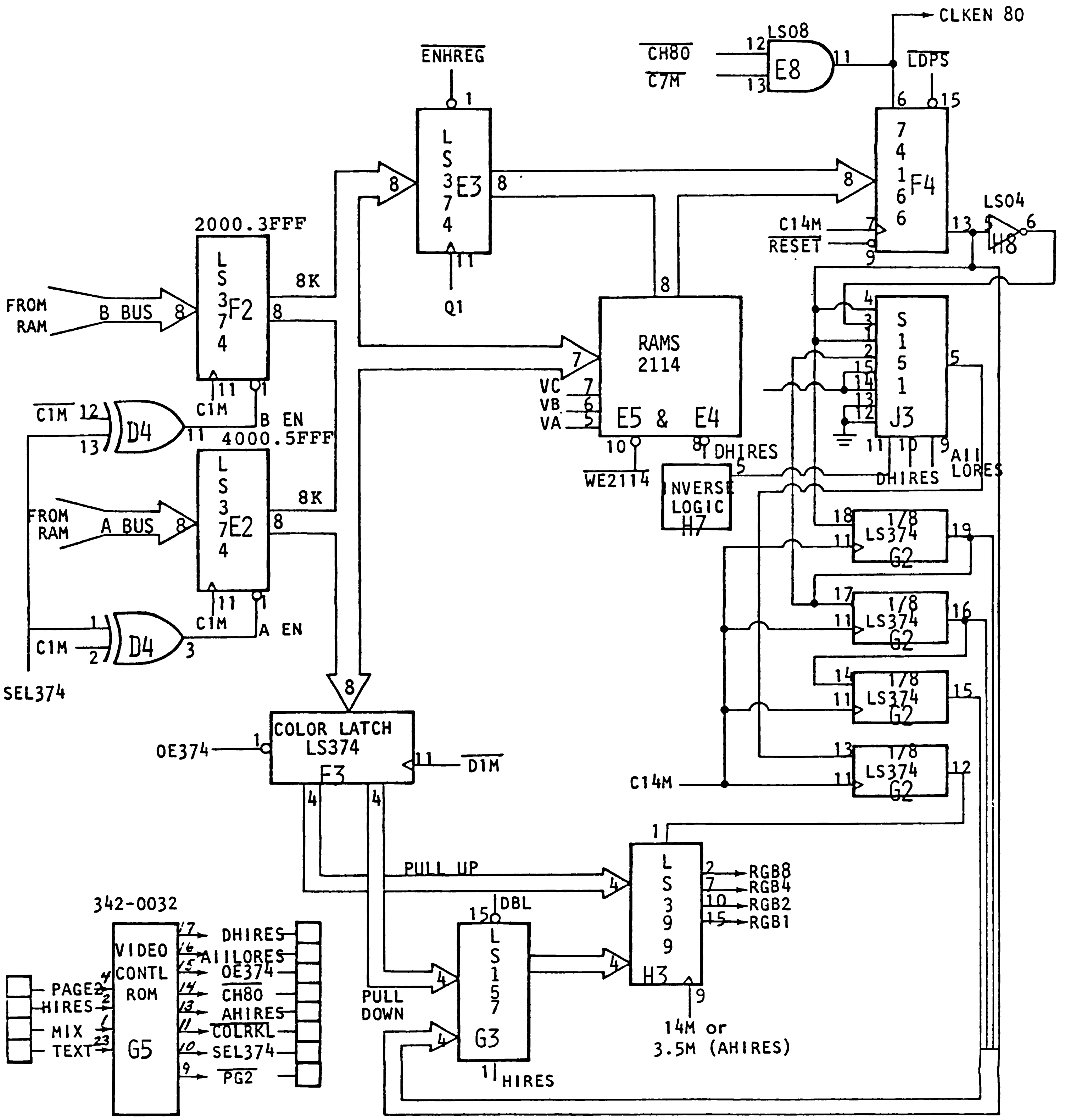
1. HIRES MODE PAGE 1 - B & W - 280 X 192
2000.3FFF (8K)

A/// VIDEO LOGIC DIAGRAM



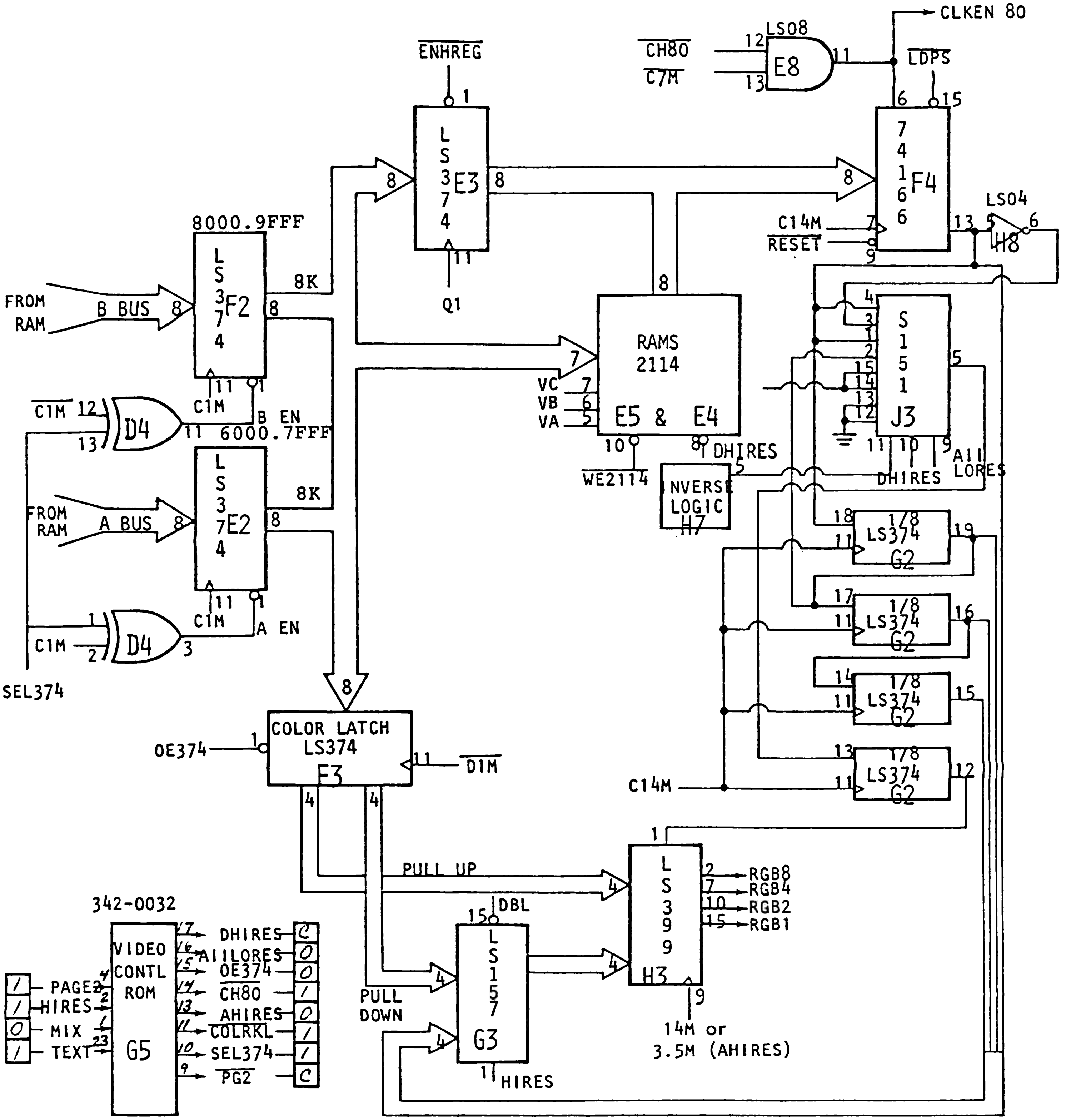
2. HIRES MODE PAGE 2 - B & W - 280 X 192
4000.5FFF (8K)

A/// VIDEO LOGIC DIAGRAM



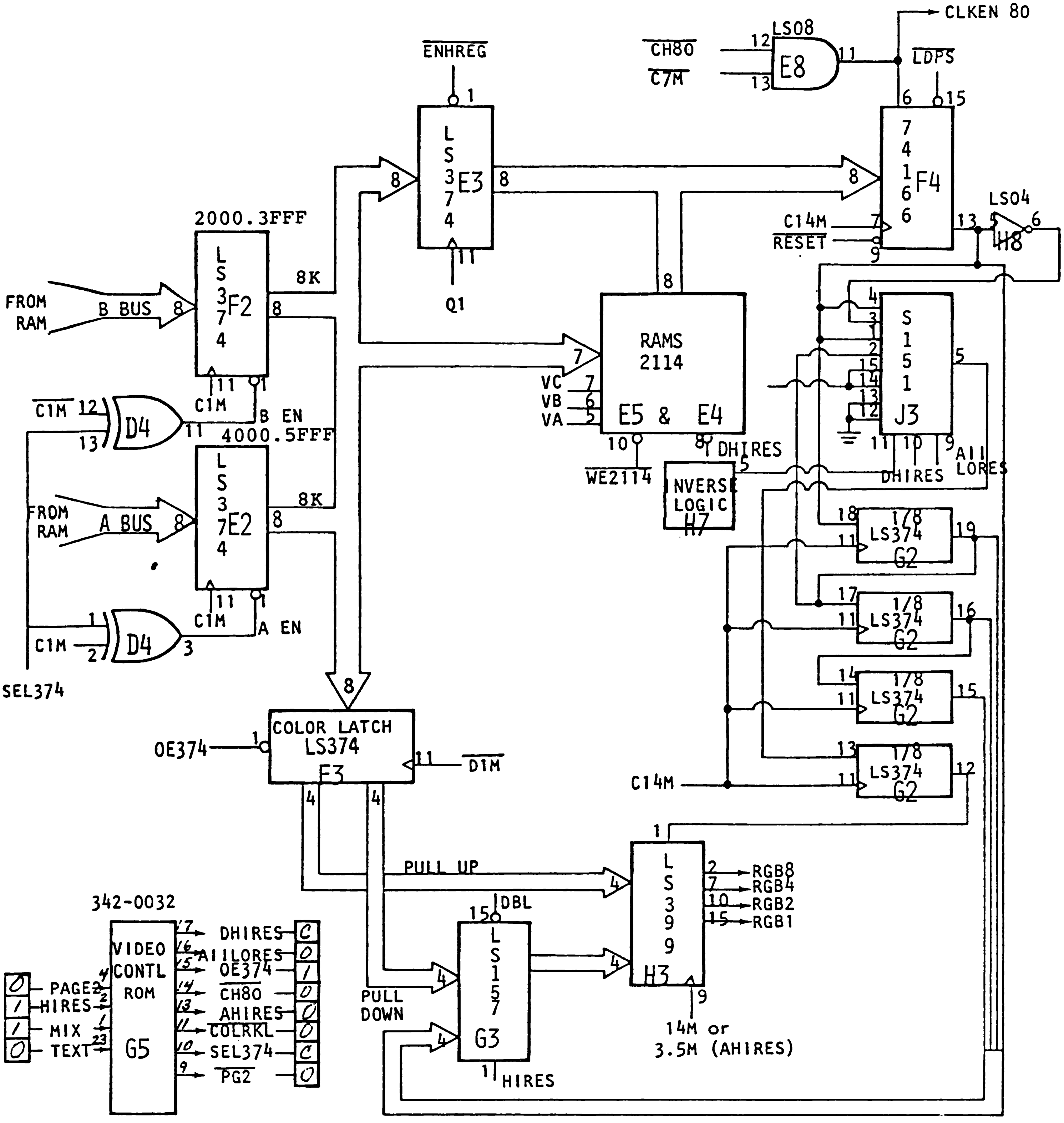
3. 280 X 192 COLOR HIRES MODE PAGE 1 (FGD/BKGD HIRES)
2000.5FFF (16K)

A/// VIDEO LOGIC DIAGRAM



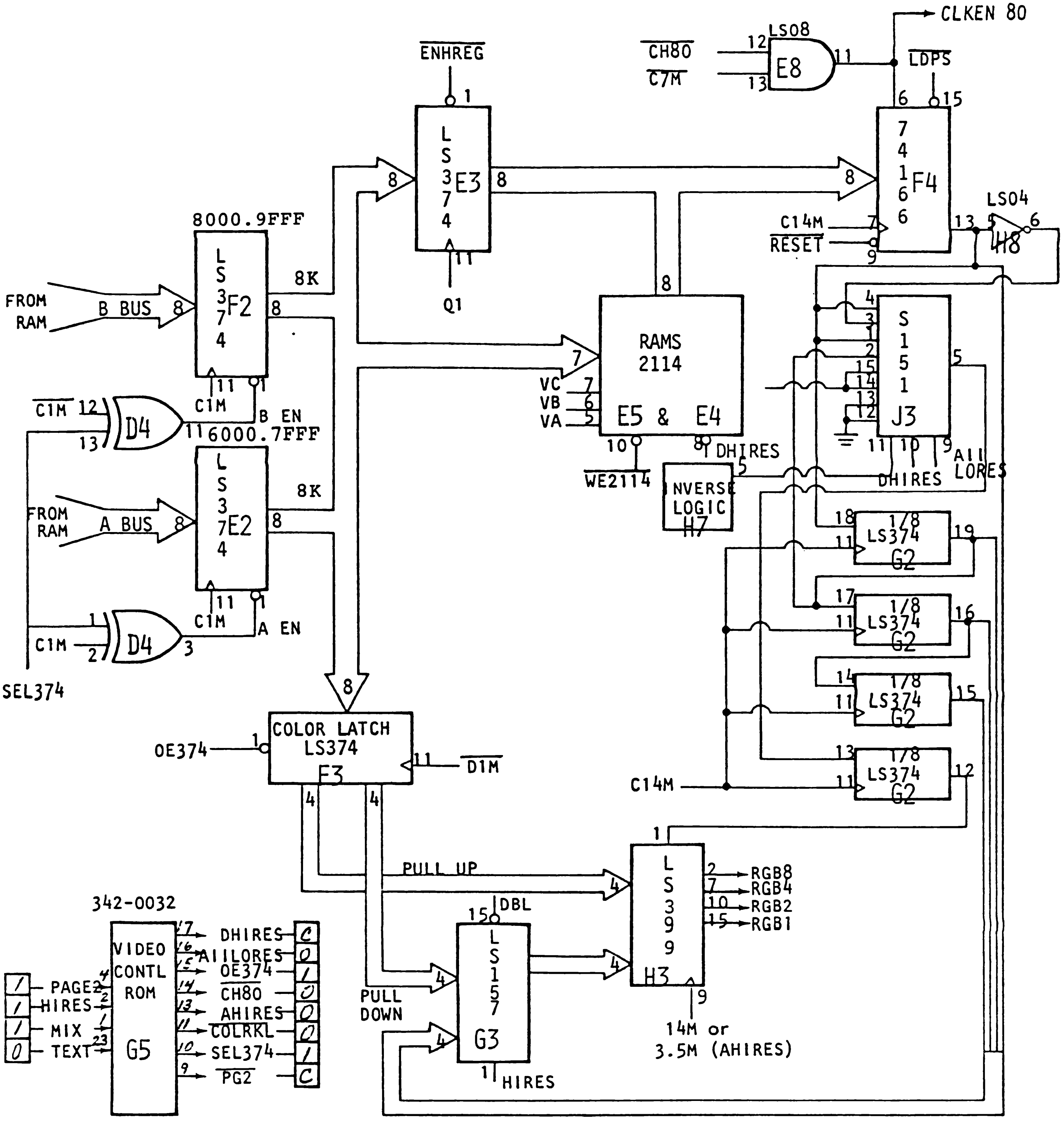
4. 280 X 192 COLOR HIRES MODE PAGE 2 (FGB/BKGD HIRES)
6000.9FFF (16K)

A/// VIDEO LOGIC DIAGRAM



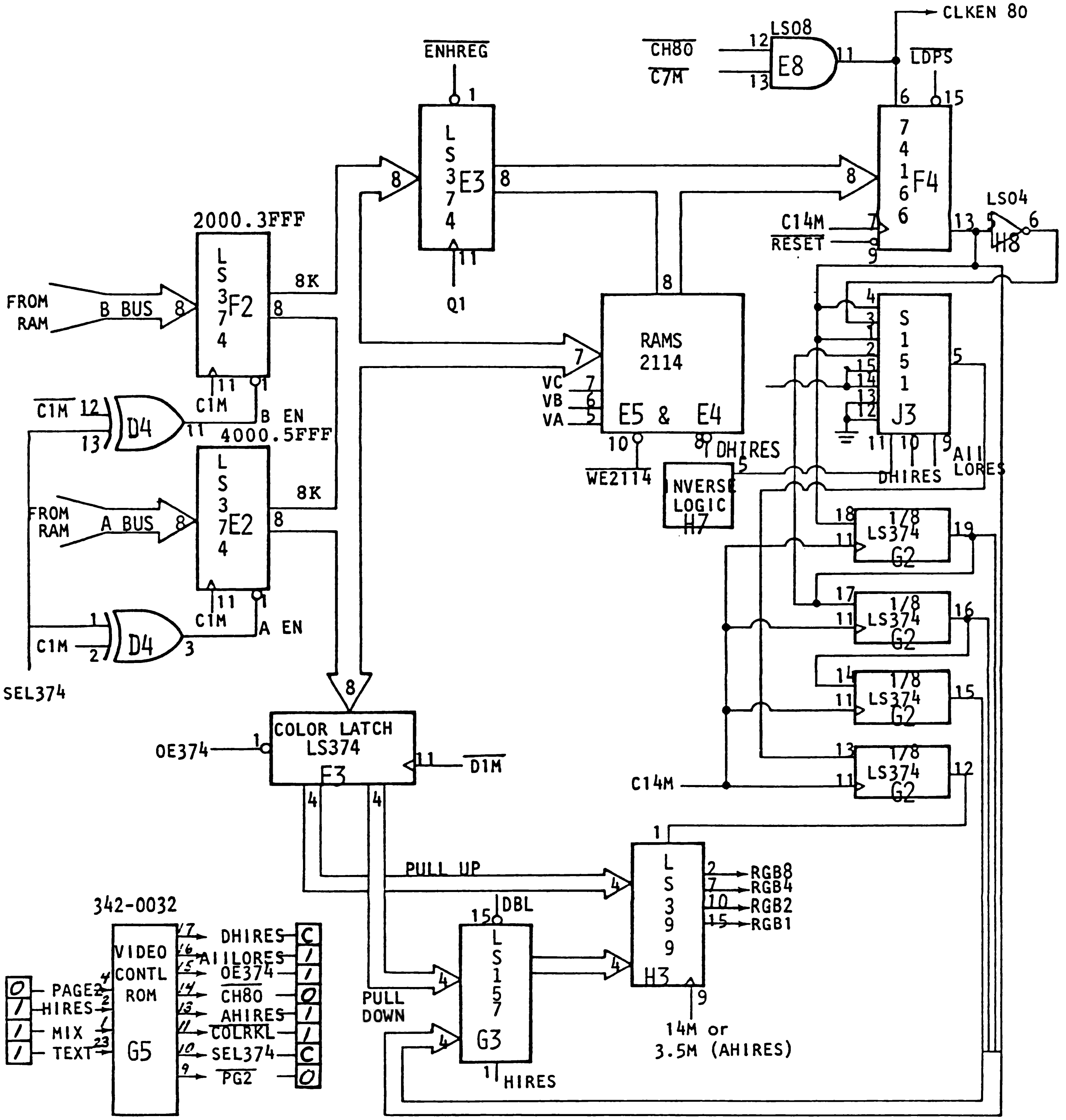
5. SUPER HIRES MODE PAGE 1 - B & W - 560X192
2000.5FFF (16K)

A/// VIDEO LOGIC DIAGRAM



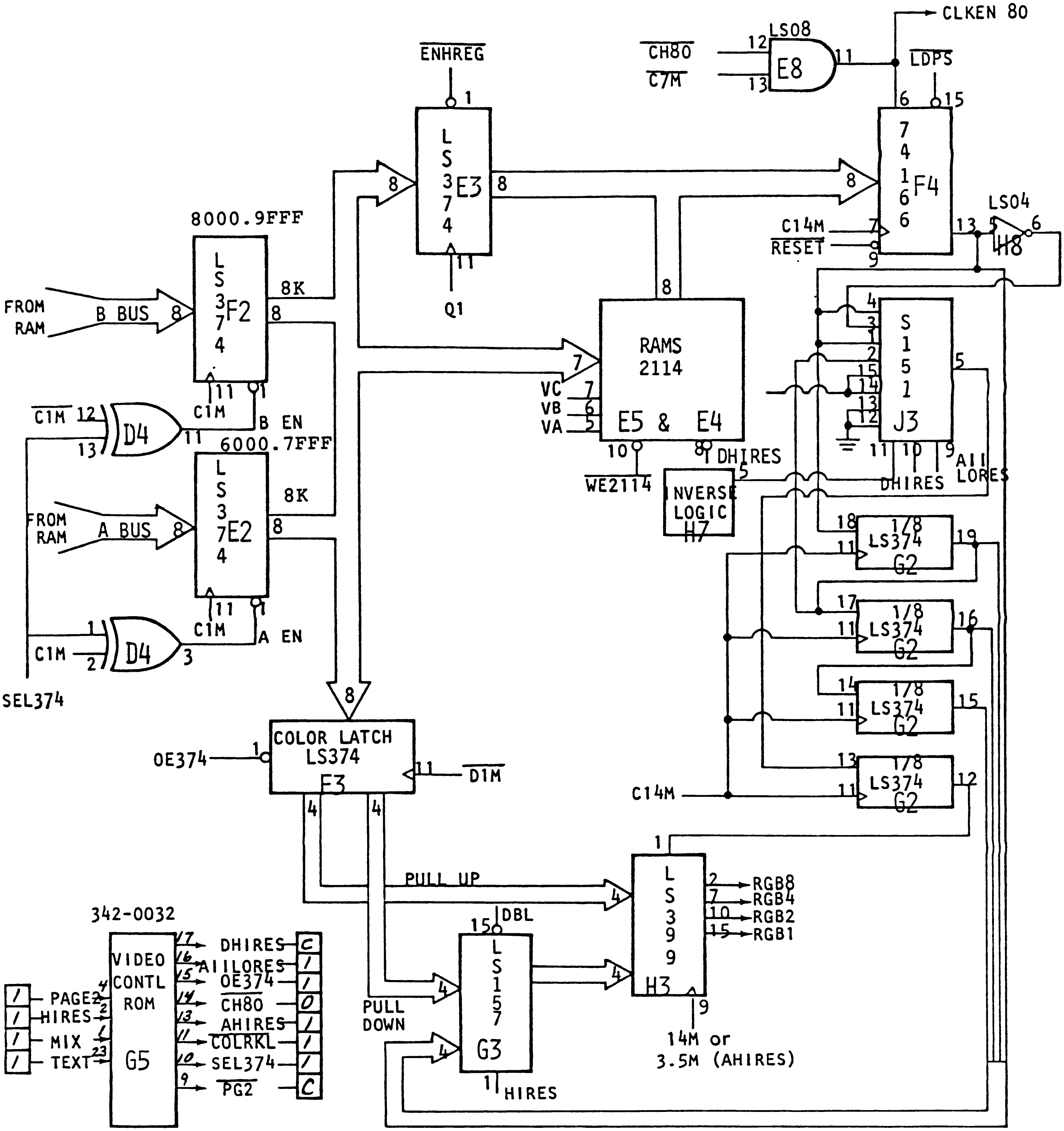
6. SUPER HIRES MODE PAGE 2 - B & W - 560 X 192
6000.9FFF (16K)

A/// VIDEO LOGIC DIAGRAM



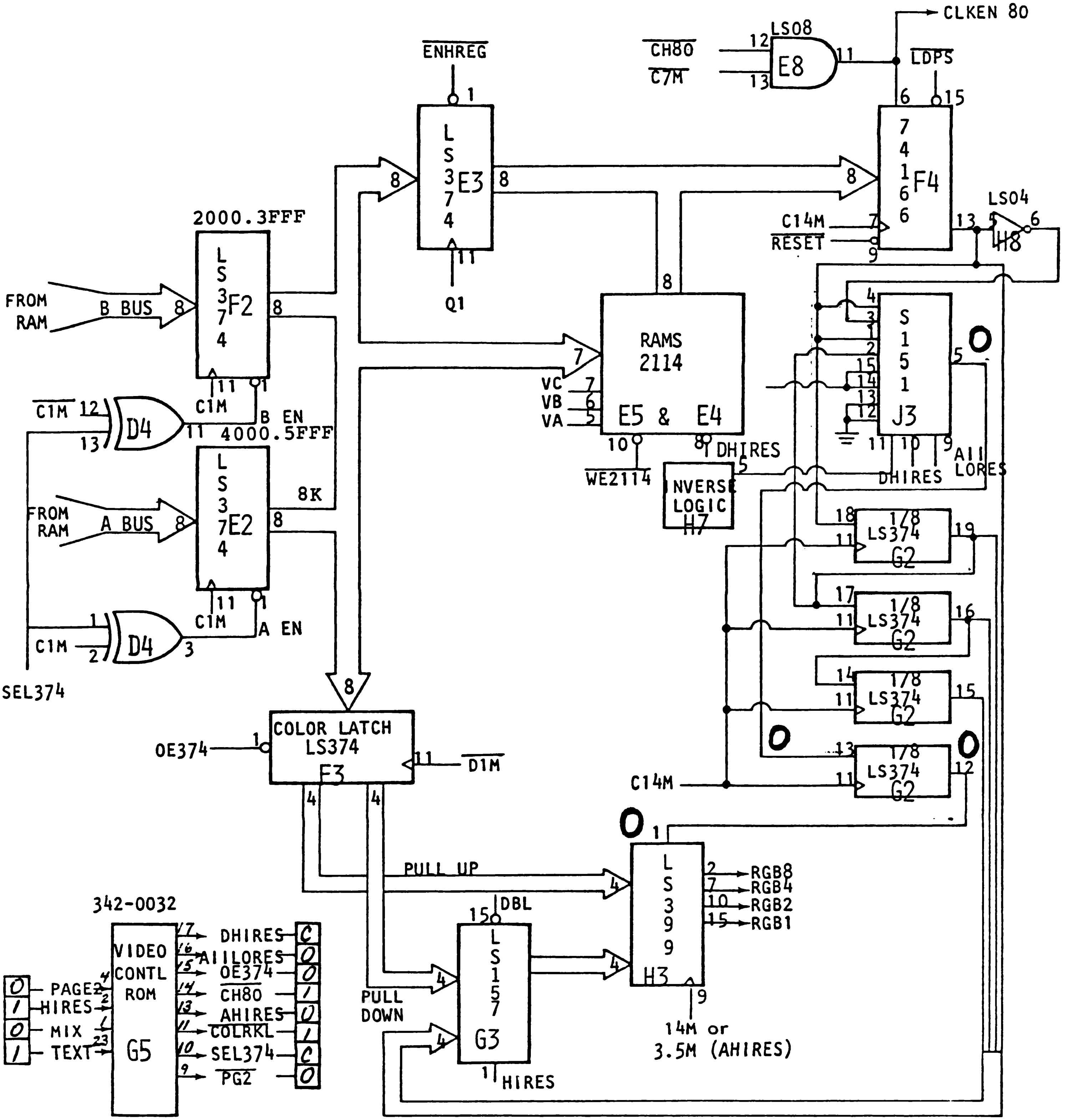
7. AHIRES TEST PAGE 1 - 140X192
2000.5FFF (16K)

A/// VIDEO LOGIC DIAGRAM



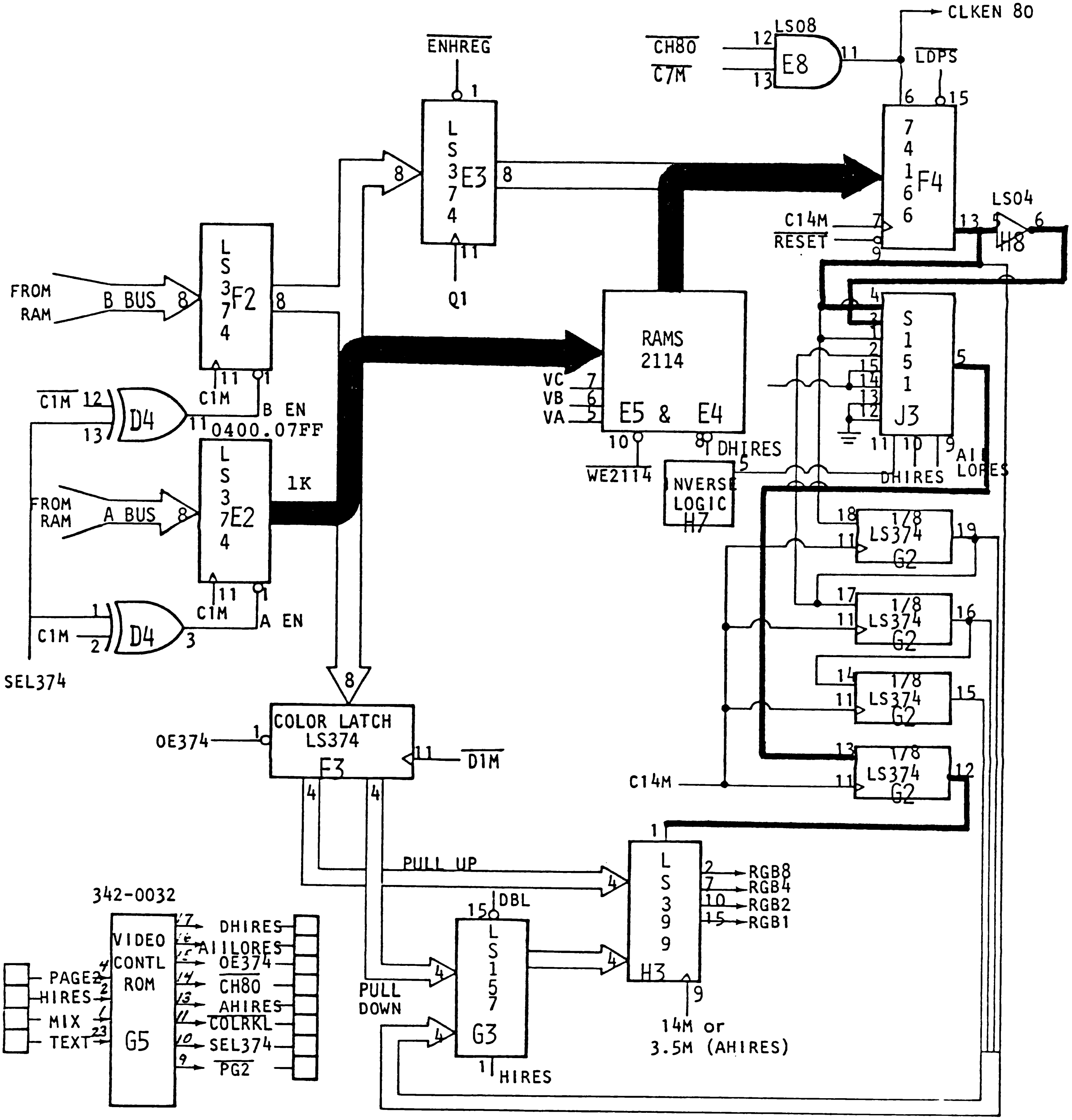
8. AHIRES TEST PAGE 2 - 140X192
6000.9FFF (16K)

A/// VIDEO LOGIC DIAGRAM



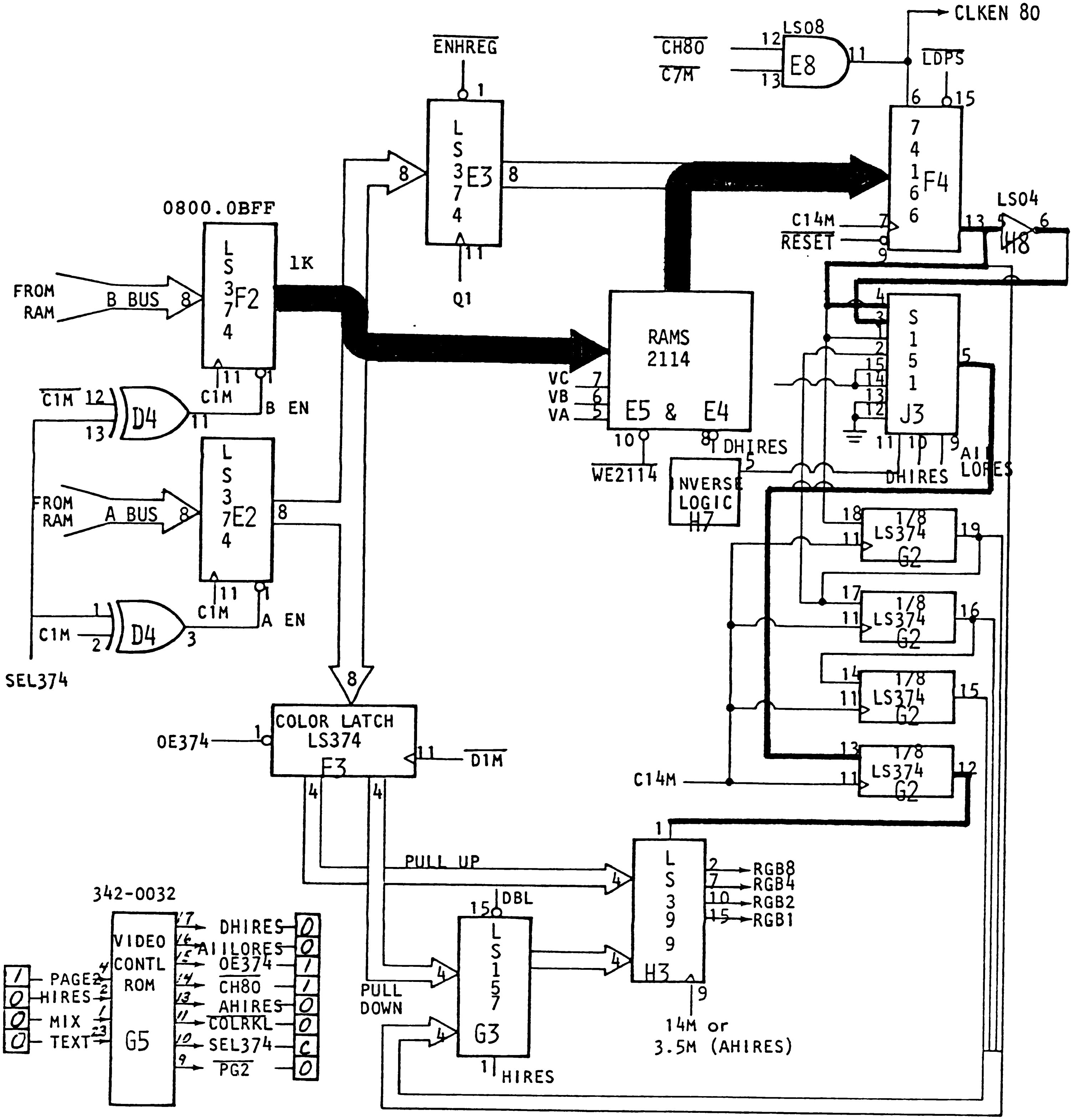
9. COLOR BAR & GRAY SCALE TEST
2000.5FFF (16K)

A/// VIDEO LOGIC DIAGRAM



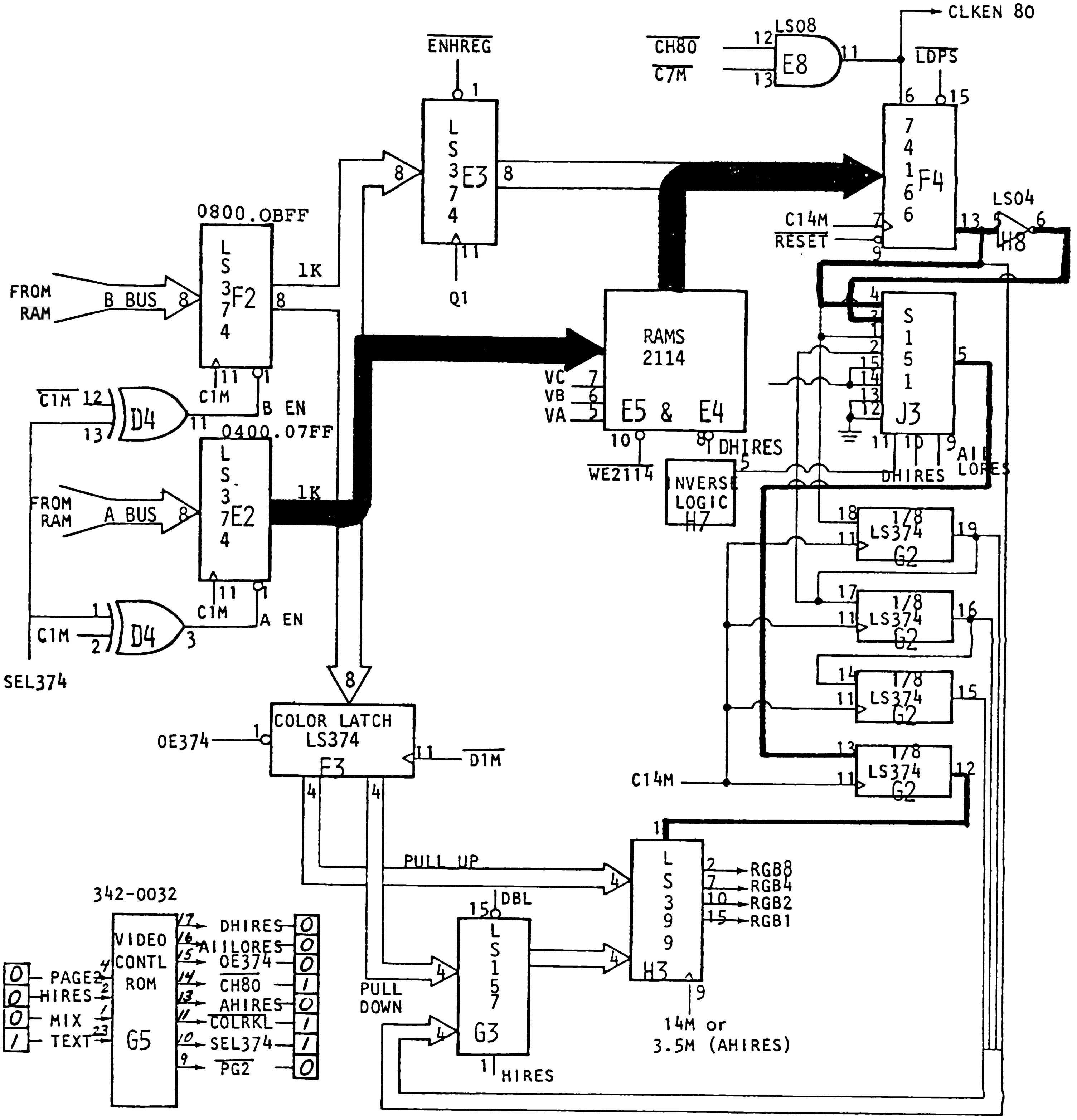
10. APPLE II TEXT MODE PAGE 1 - B & W - 40 COLUMN
0400.07FF (1K)

A/// VIDEO LOGIC DIAGRAM



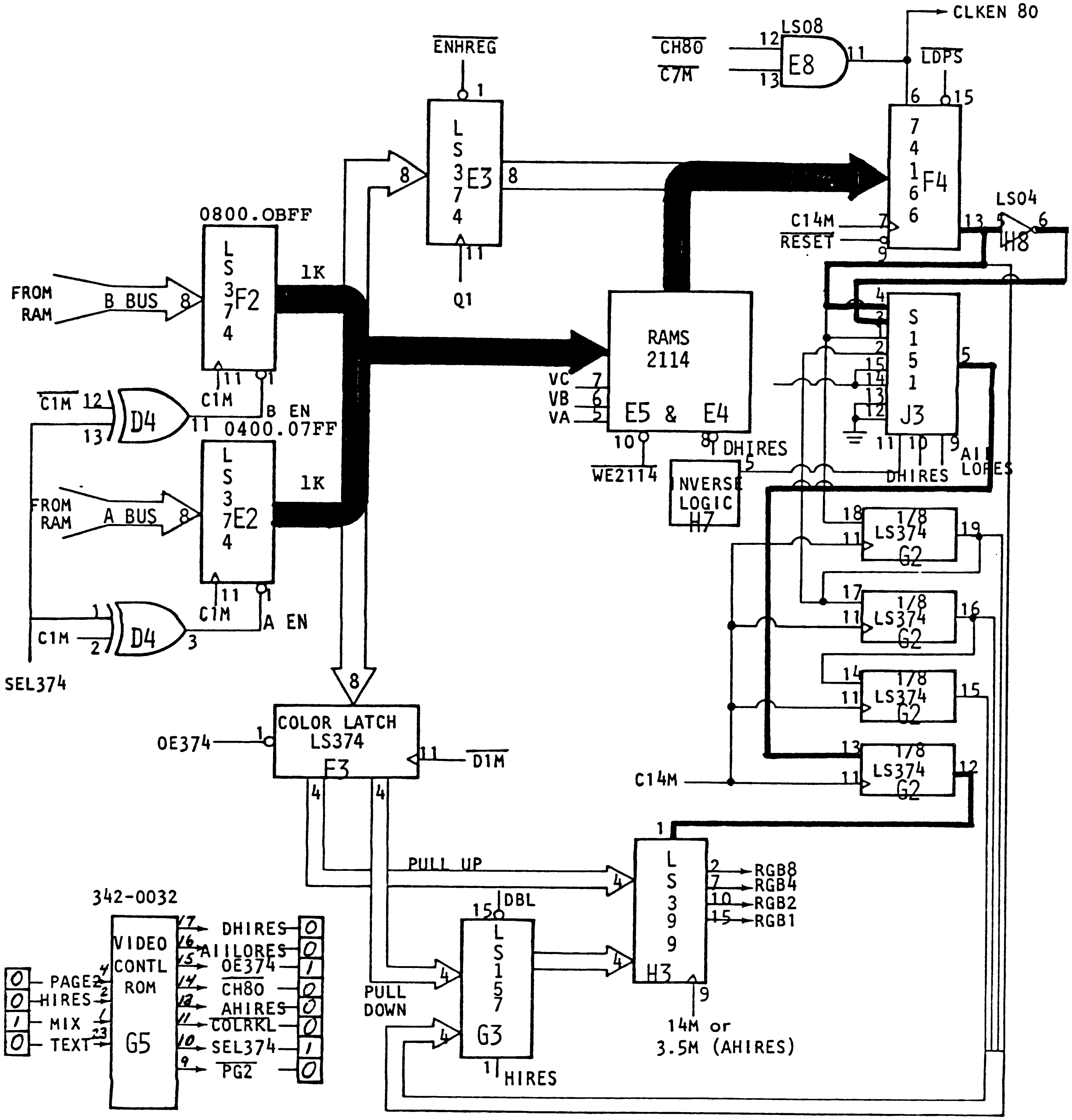
11. APPLE II TEST MODE PAGE 2 - B & W - 40 COLUMN
0800-0BFF (1K)

A/// VIDEO LOGIC DIAGRAM



12. SARA 40 COLUMN TEXT MODE TEST- 16 COLORS
0400.0BFF (2K)

A/// VIDEO LOGIC DIAGRAM



13. SARA 80 COLUMN TEXT MODE TEST - B & W
0400.0BFF (2K)

VIDEO MODES

APPLE III

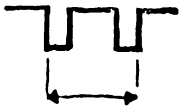
OUTPUTS

INPUTS TO ROM G5 (0032)

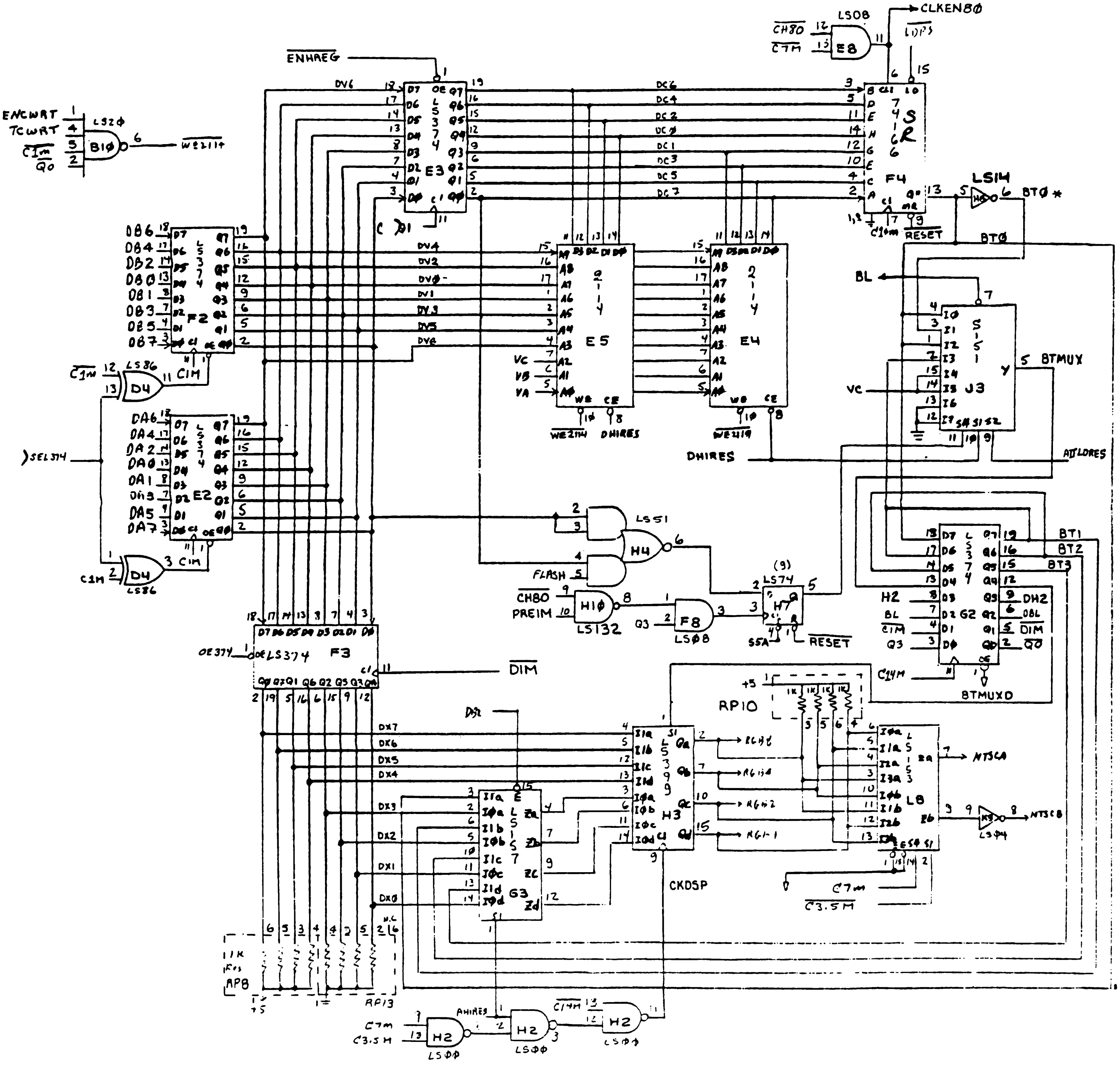
OUTPUTS FROM ROM G5 (0032)

	H6 (9334) pin 7	H6 (9334) pin 5	H6 (9334) pin 4	.6 (9334) pin 6	$\overline{\text{PG 2}}$	SEL 374	$\overline{\text{COLOR KL}}$	A HIRES	CH 80	$\overline{\text{OE}}$ 374	AII LORES	D HIRES	
	ROM G5 pin 2	ROM G5 pin 1	ROM G5 pin 23	ROM G5 pin 4	G5 pin 9	G5 pin 10	G5 pin 11	G5 pin 13	G5 pin 14	G5 pin 15	G5 pin 16	G5 pin 17	
	0 1 C056/C057	0 1 C052/C053	0 1 C050/C051	0 1 C054/C055									
PAGE 1	HIRES	MIX	GR/TEXT	GP1-2									
40 CHAR AII (B/W)	0	0	0	0	0	1	0	0	1	1	0	0	1
40 CHAR SARA (color)	0	0	1	0	0	1	1	0	1	0	0	0	2
80 CHAR (B/W)	0	1	0	0	0	1	0	0	0	1	0	0	3
80 CHAR (B/W)	0	1	1	0	0	1	0	0	0	1	0	0	4
AII HIRES (280x192, B/W)	1	0	0	0	0	clocking	0	0	1	1	0	clocking	5
FGD/BKGD HIRES (280x192, 16 colors)	1	0	1	0	0	clocking	1	0	1	0	0	clocking	6
SUPER HIRES (560x192, B/W)	1	1	0	0	0	clocking	0	0	0	1	0	clocking	7
140 x192 AHIRES (140x192, color)	1	1	1	0	0	clocking	1	1	0	1	1	clocking	8
PAGE 2													
40 CHAR AII (B/W)	0	0	0	1	0	clocking	0	0	1	1	0	0	1
40 CHAR SARA (color)	0	0	1	1	0	clocking	1	0	1	0	0	0	2
80 CHAR (B/W)	0	1	0	1	0	clocking	0	0	0	1	0	0	3
80 CHAR (B/W)	0	1	1	1	0	clocking	0	0	0	1	0	0	4
AII HIRES (280x192, B/W)	1	0	0	1	0	1	0	0	1	1	0	clocking	5
FGD/BKGD HIRES (280x192, 16 colors)	1	0	1	1	clocking	1	1	0	1	0	0	clocking	6
SUPER HIRES (560x192, B/W)	1	1	0	1	clocking	1	0	0	0	1	0	clocking	7
140 x 192 AHIRES (140x192, color)	1	1	1	1	clocking	1	1	1	0	1	1	clocking	8

clocking



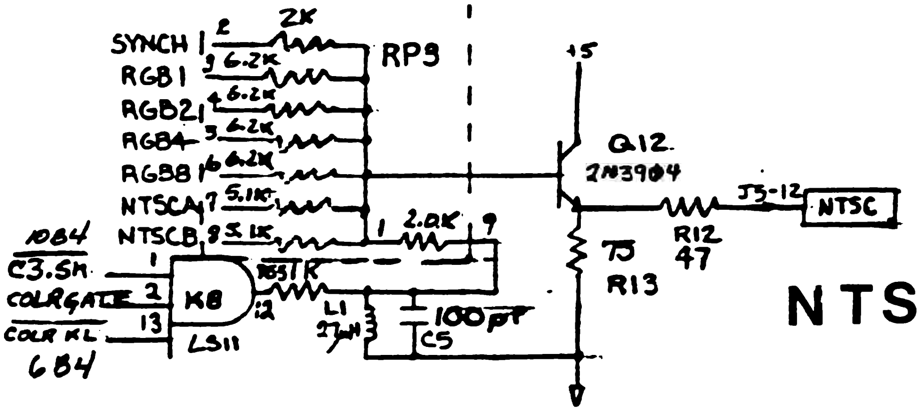
≈ 175 uSec ~ 5.7 KHz


CLKEN80
LS08
CH80
C7M
E8
ENHREG
DV6
E3
F4
LS14
BTØ *
BTØ
BL
ENCWRT
TCWRT
C1m
Q0
LS20
B10
WE2114
DB6
DB4
DB2
DB0
DB1
DB3
DB5
DB7
F2
C1M
LS86
D4
DV4
DV2
DVØ
DV1
DV3
DV5
DV8
E5
E4
VC
VB
VA
WE2114
DHIRES
WE2119
J3
BTMUX
VC
AIILORES
DHIRES
)SEL374
DA6
DA4
DA2
DA0
DA1
DA3
DA5
DA7
E2
LS51
H4
FLASH
CH80
PREIM
H10
LS132
Q3
F8
LS08
(9)
LS74
H7
55A
RESET
BT1
BT2
BT3
H2
BL
C1M
Q3
G2
DH2
DBL
DIM
Q0
C14M
BTMUXD
OE374
LS374
F3
DIM
+5
RP10
DX7
DX6
DX5
DX4
DX3
DX2
DX1
DX0
H3
RGH2
RGH4
RGH2
RGH1
CKDSP
L8
NTSCA
NTSCB
LS04
C7M
C3.5M
G3
1K
RP8
+5
RP13
AHIRES
C7M
C3.5M
H2
LS00
H2
LS00
C14M
H2
LS04

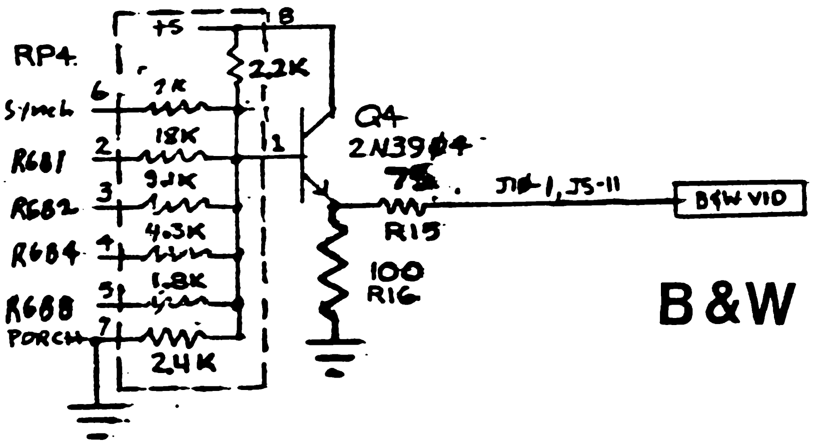
VIDEO OUTPUTS

- NTSC COLOR COMPOSITE VIDEO
- NTSC B/W COMPOSITE VIDEO
- SYNC
- FOUR PRIMARY INDEPENDENT VIDEO LINES
- MIX TO FORM RGB APPLE COLORS
  THREE LINES CAN DRIVE TTL RGB MONITOR

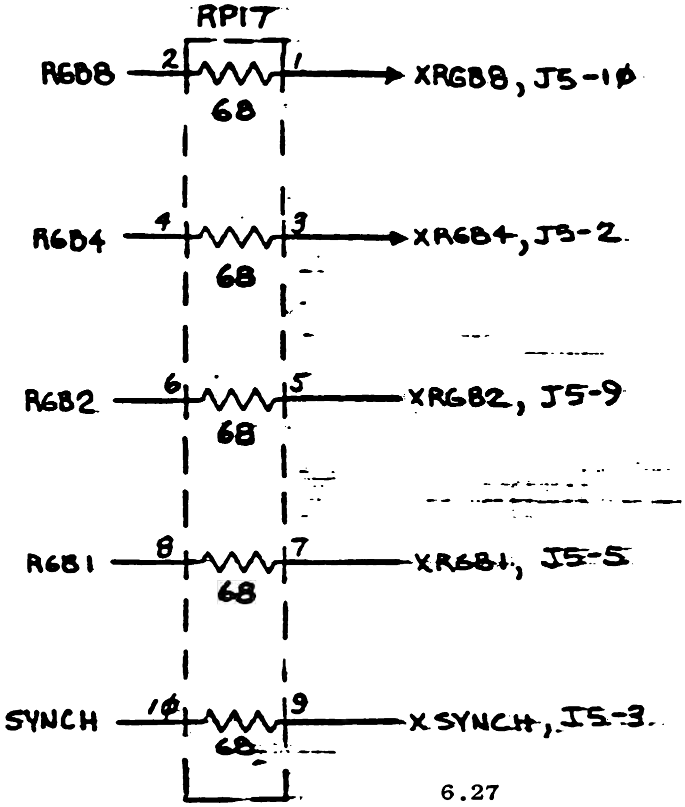
VIDEO OUTPUTS



NTSC

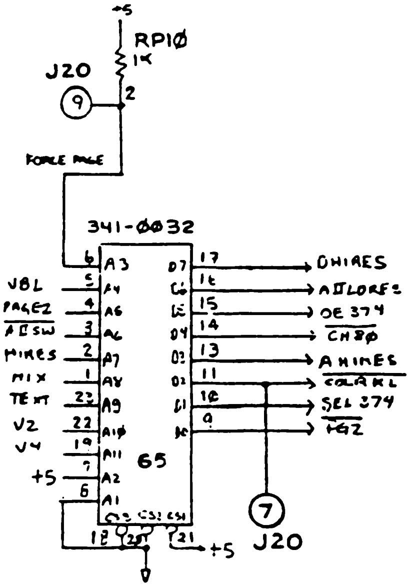


B&W VIDEO



RGB

ROM 341-0032



A=A
B=B
C=S4
D=VBL
E=PAGE2
F=AIISW'
G=HIRES
H=MIX
I=TEXT
J=V2
K=V4
D0=PG2
D1=SEL374
D2=COLRKL'
D3=AHIRES
D4=CH80'
D5=OE374
D6=AIILORES
D7=DHIRES

PG2=AIISW'*(HIRES*MIX'*TEXT ')'*HIRES*PAGE2*S4*VBL'

SEL374=(VBL'*(AIISW*(PAGE2'*(TEXT +MIX*V2*V4)'+PAGE2*(TEXT +MIX*V2*V4))+
AIISW'*(HIRES*(PAGE2*S4)'+HIRES'*(PAGE2*S4))))'

COLRKL'=(AIISW*TEXT +AIISW'*(HIRES'*(MIX+TEXT ')+HIRES*TEXT '))'

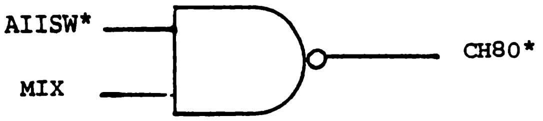
AHIRES=AIISW'*(HIRES*MIX*TEXT)

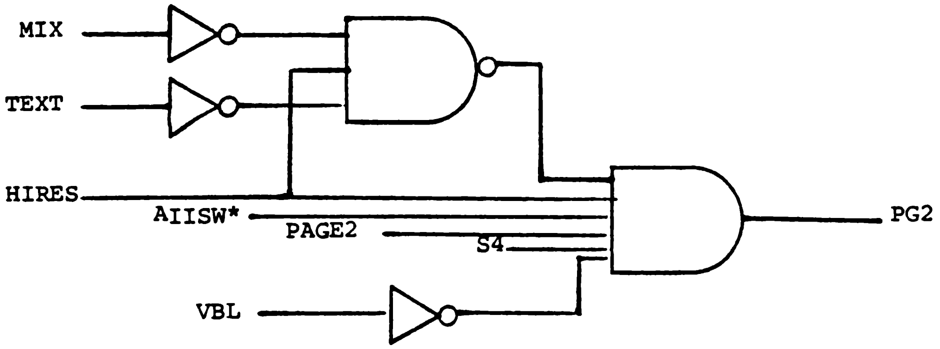
CH80'=(AIISW'*MIX)'

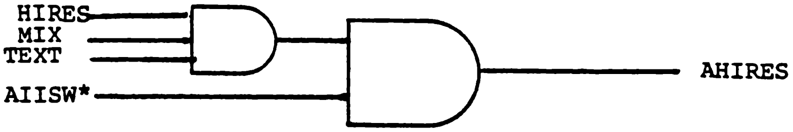
OE374=(AIISW*HIRES'*(TEXT +MIX*V2*V4)'+AIISW'*MIX'*TEXT)'

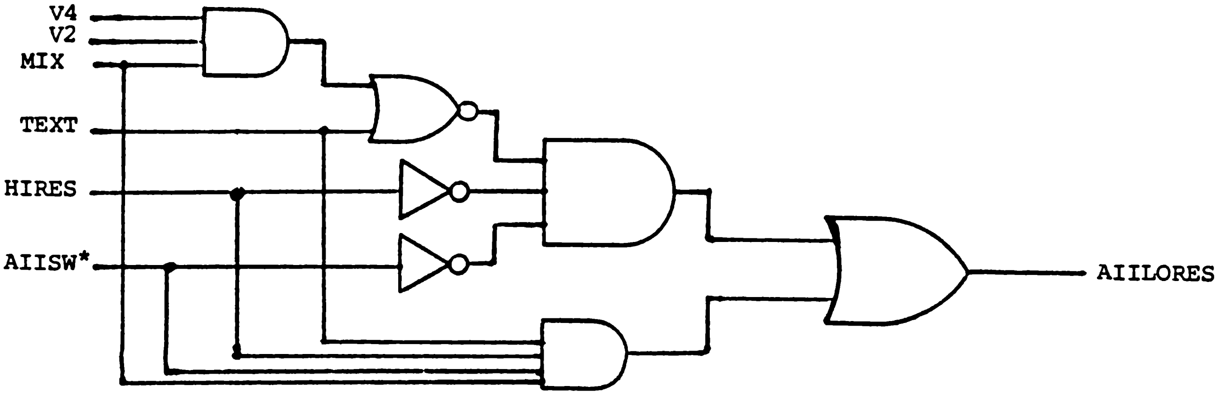
AIILORES=AIISW*HIRES'*(TEXT +MIX*V2*V4)'+AIISW'*HIRES*MIX*TEXT

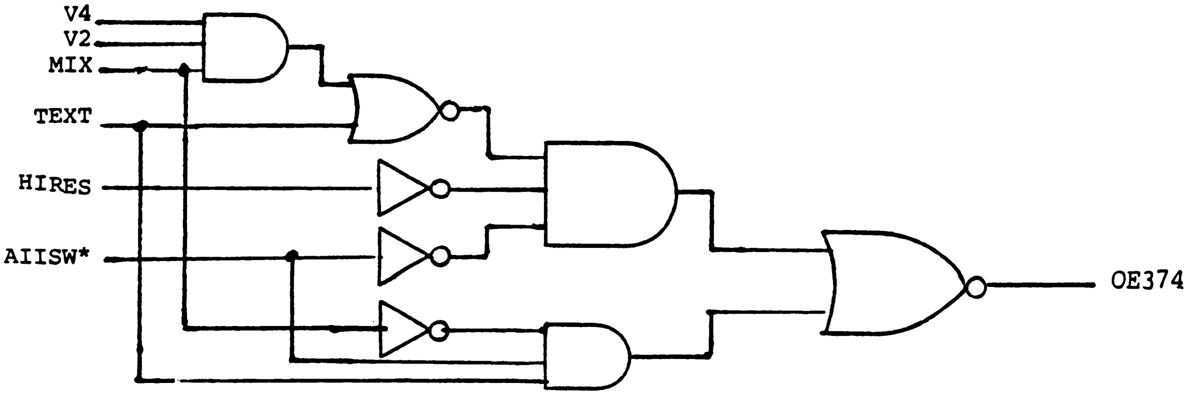
DHIRES=(AIISW*HIRES*(TEXT +MIX*V2*V4)'+AIISW'*HIRES)*VBL'


AIISW*
MIX
CH80*


MIX
TEXT
HIRES
AIISW*
PAGE2
S4
VBL
PG2


HIRES
MIX
TEXT
AIISW*
AHIRES


V4
V2
MIX
TEXT
HIRES
AIISW*
AIILORES


V4
V2
MIX
TEXT
HIRES
AIISW*
OE374

THE COLOR VIDEO CONNECTOR

Pin	Name	Description
1	SG	Shield Ground.
2	XRGB4	One of four GRB outputs. This (and pins 5, 9, and 10) is a TTL output with instantaneous color information. A linear weighted sum of these four signals will form a true 16-color RGB video signal
3	SYNCH	Composite synchronization signal with negative-going tips.
4	PDI	Not used.
5	XRGB1	See pin 2.
6	GND	Power and signal ground.
7	-5V	-5 volt power supply. A device may draw up to 200 ma through this pin.
8	+12V	+12 volt power supply. A device may draw up to 500 ma through this pin.
9	XRGB2	See pin 2.
10	XRGB8	See pin 2.
11	BWVID	Black and white composite video. This is an NTSC composite video signal with negative-going synch tips, 1 volt peak-to peak into a 75 ohm load. Color information is encoded as a linear grey scale.
12	NTSC	Color composite video. This is an NTSC-compatible video signal with negative-going sych tips, 1 volt peak-to-peak into a 75 ohm load.
13	GND	Power and signal ground.
14	-12V	-12 volt power supply. A device may draw up to 200 ma through this pin.
15	+5V	+5 volt supply. A device may draw up to 1 amp through this pin.

This connector supplies 7 different video signals and 4 power supply voltages. Through this connector you can hook up the Apple to any NTSC color or black and white video monitor. With an additional circuit you can hook up the Apple to a studio-quality RGB color monitor.

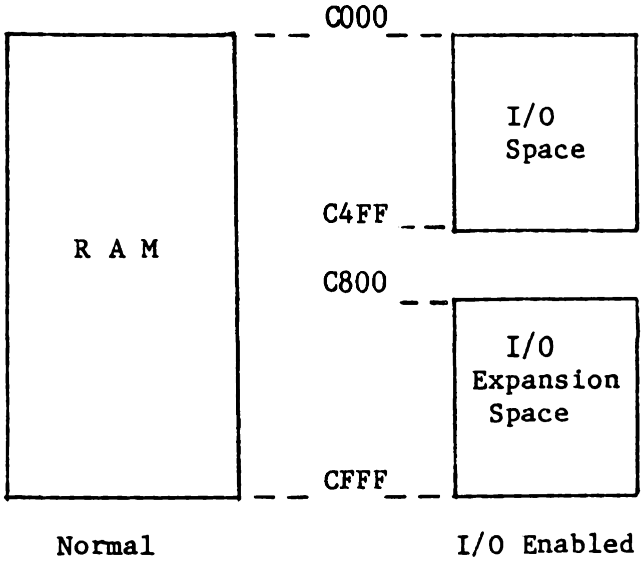
All power supply current ratings assume that no peripheral cards are installed in the system. If there are cards in the system, be sure to account for the current drawn by those cards.

INPUT/OUTPUT (I/O)

DESCRIPTION

In Apple computers I/O devices are treated very much like memory locations. Most of the system's I/O functions are mapped into the address range C000 to CFFF. The I/O space is enabled by a bit in the Environmental Register. Addresses C0XX control the on-board I/O. Addresses C1XX, C2XX, C3XX, and C4XX are reserved for the exclusive use of the four I/O slots. The I/O expansion space from C800 to CFFF is switched between the I/O slots. Addresses C500 to C7FF are always Ram, regardless of the setting of the I/O enable bit.

I/O ADDRESS SPACE



INTERFACE CONTROL SIGNALS

For every I/O slot, the Apple /// provides 16 locations that set the Device Select* signal and 256 locations that set the I/O Select* signal.

The Device Select* signal is a signal specific to each slot. It is active for for a 16-address block. This signal is ususally used as an enable signal.

The I/O Select* signal can be used to control a page of memory (256 addresses) which could be placed in ROM, in the interface circuitry, for executing "driver routines". The I/O Select* signal could also be used in circumstances where a small amount of read/write memory for temporary storage is needed. Each I/O slot has its own I/O Select* signal, and each signal is active when a specific page of memory is addressed.

The I/O Strobe is common to all I/O slots. This signal will be low (true) when an address location within the range of C800 to CFFF (2K of memory).

INTERRUPTS

Interface cards that are capable of generating interrupts MUST latch the interrupt output until it is reset by the software. In addition, they MUST include the ability to mask and unmask their interrupt through software, and MUST default to the masked state when the system is reset.

C09X	Slot 1 Device Select
C1XX	Slot 1 I/O Select
C0AX	Slot 2 Device Select
C2XX	Slot 2 I/O Select
C0BX	Slot 3 Device Select
C3XX	Slot 3 I/O Select
C0CX	Slot 4 Device Select
C4XX	Slot 4 I/O Select

The method of accomplishing this transmission between the interface and the computer is called handshaking. In the Apple ///, the handshaking is normally accomplished through the exchange of Device Select*, I/O Select*, IRQ*, and R/W*. The R/W* control signal is used to synchronize the flow of data to and from I/O devices. When the Read/Write* signal is a logic one, the processor is reading information from the data bus. Conversely, when R/W* is low, we are performing a write to the data bus.

As you can see, the handshaking between the Apple /// and the interface is dependent upon the software. Let us again emphasize the role of addressing plays in the I/O process.

ADDRESSING THE I/O

There are certain addresses that you can write to or read from to control the operation of the interface card. Where "n" is the number of the slot where the interface is installed, these hardware addresses are in the range:

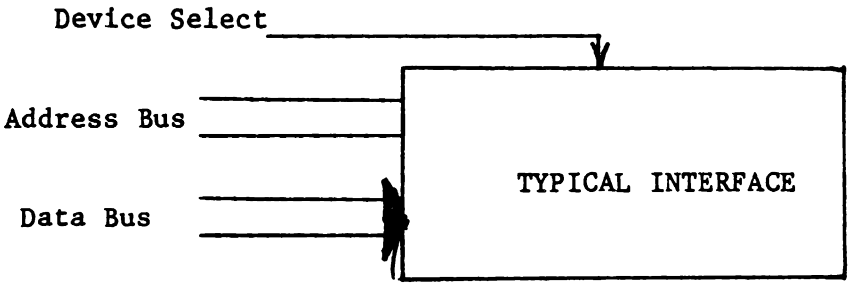
C080 + n0 to C087 + n0

For example, if you install an interface in slot 2, you should write to the addresses from C0A0 through C0A7.

The operations that the interface card performs are initiated by the read or write operations presented on these hardware addresses.

THE INPUT OPERATION

In the input operation, whenever the correct address is presented to the interface card, the data is present on the data lines D7-D0. For example, if the location C083 + n0 corresponds in the software to an input, the data presented on D7-D0 is accepted by the computer. If the interface card contains a control ROM, the code in ROM is being addressed whenever the I/O Select line is low; that is when the address on the address lines is between Cn00 and CnFF). Recall that "n" is the slot number.

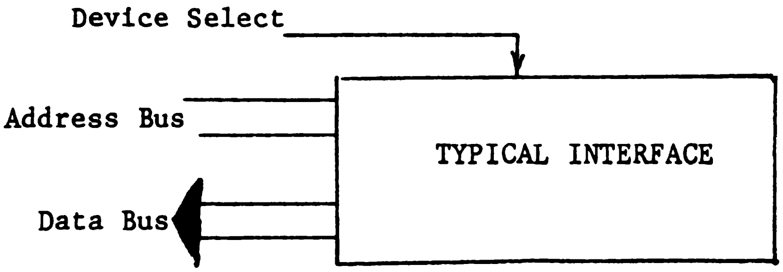


THE OUTPUT OPERATION

In the output operation,

IF the address Co81 + n0 represents an output operation
in the software
AND the Read/Write* signal is low,

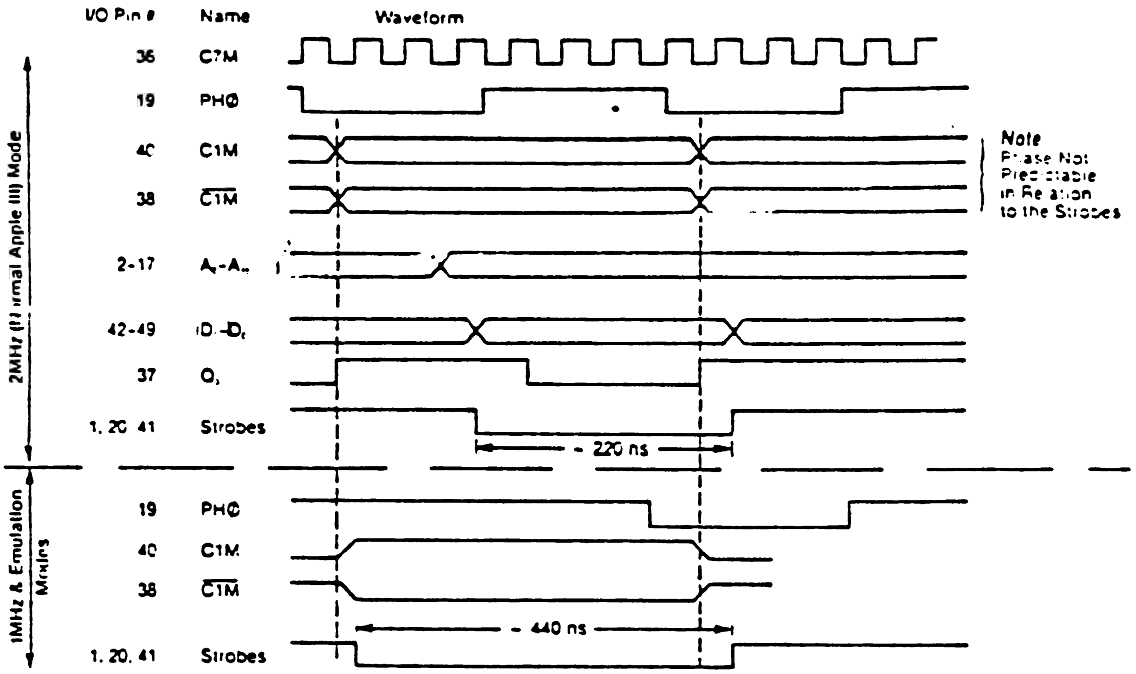
THEN the data is presented on the data bus and latched into
the interface whenever the address C081 + n0 is presented.



SYSTEM TIMING

A system timing diagram is provided. This diagram shows the timing of some signals at the I/O slots in the 1 MHz and 2 MHz frequency modes.

I/O TIMING DIAGRAMS



THE A/// JOYSTICK

The A/// has two ports designated for joystick (x and y axis paddles) each with two switches. However, unlike the Apple II the ports do not have "annunicator" outputs. One of the switches is a momentary contact and the other is a toggle.

The Analog X and Y inputs are read through a ramp type Analog to Digital converter (A/D). These values derived must be interpreted by the program. The switches are read to the data bus directly through a mulitplexor.

The 9708 has multiplexed inputs. To select which input channel is to be read the proper address must be set in an addressable latch and must be held during the PDLEN (ramp start) low cycle.

The I/O address for the setting and clearing of the A/D addresses and the ramp start is as shown in the following table:

I/O Address	A/D Function	Signal Name
C058	A0 Clear	PDL0
C059	A0 Set	
C05A	A2 Clear	PDL2
C05B	A2 Set	
C05C	Ramp Start Clear	PDLEN
C05D	" " Set	
C05E	A1 Clear	AXCO
C05F	A1 Set	

To read the various signals associated with the joysticks the following addresses should be read:

I/O Address	Function
C060,8	Switch 0
C061,9	Switch 1/Margin Switch
C062,A	Switch 2
C063,B	Switch 3/Serial Clock
C066,E	A/D ramp stop (PDLOT)

Note: The joystick port at J3 (Port A) can be configured to be a serial port to support a device like the Silentype. Care must be taken to insure that the port has been configured for the proper device or signal contention will occur and give erroneous results.

The sequence of operation for the A/D would be as follows:

1) set the desired channel address nto A/D 0 through A/D 2.

2) start the A/D by cycling the PDLEN signal low for 40 micro seconds then back high

3) set up one of the timers to count.

4) test for ramp stop

5) read the counter

6) compute the value of the channel input.

Peripheral Connector Pinout

GND	26	25	+5V
DMAOK	27	24	NOT USED
$\overline{\text{DMAI}}$	28	23	NOT USED
$\overline{\text{IONMI}}$	29	22	$\overline{\text{TSADE}}$ (Open collector)
$\overline{\text{IRQ}}$	30	21	RDY (Open collector)
$\overline{\text{IORES}}$	31	20	$\overline{\text{I/O STROBE}}$
$\overline{\text{INH}}$	32	19	PHO
-12V	33	18	R/$\overline{\text{W}}$
-5V	34	17	A15
SYNC	35	16	A14
C7M	36	15	A13
Q3	37	14	A12
$\overline{\text{C1M}}$	38	13	A11
$\overline{\text{IOCLR}}$	39	12	A10
C1M	40	11	A9
$\overline{\text{DEV SEL}}$	41	10	A8
D7	42	9	A7
D6	43	8	A6
D5	44	7	A5
D4	45	6	A4
D3	46	5	A3
D2	47	4	A2
D1	48	3	A1
D0	49	2	A0
+12V	50	1	$\overline{\text{I/O SELECT}}$

A/// Peripheral Connector Slot

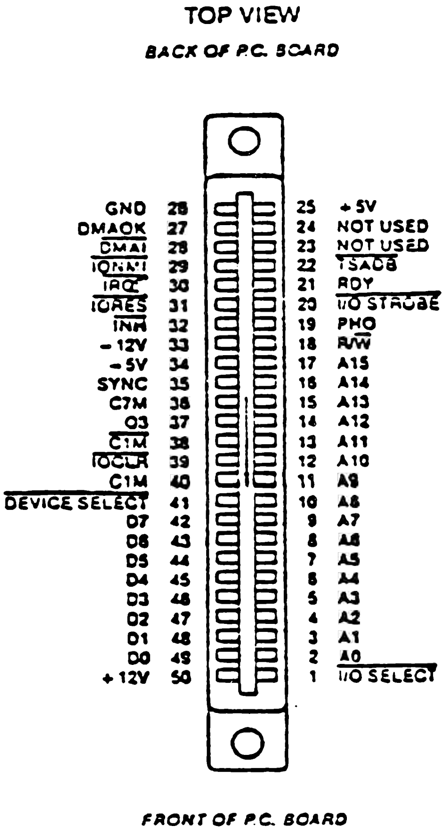


Table 33: Peripheral Connector Signal Description

Pin:	Name:	I/O	Description:
1	$\overline{\text{I/O SELECT}}$	O	This line, normally high, will become low when the microprocessor references page $Cn, where n is the individual slot number. This signal become active during PHO (nominally 500ns) and will drive 12 LSTTL loads.
2-17	AO-A15	I, O	The buffered address bus. The address on these lines becomes valid within 300ns after the beginning of $\overline{\text{C1M}}$ and remains vaild through PHO. These lines will each drive 8 LSTTL loads.
18	R/$\overline{\text{W}}$	I, O	Buffered Read/$\overline{\text{Write}}$ signal. This becomes valid at the same time the address bus does, and goes high during a read cycle and low during a write. This line can drive up to 10 LSTTL loads.
19	PHO	O	A 1 MHz signal which is identical to C1M. This line will drive 5 LSTTL inputs.
20	$\overline{\text{I/O STROBE}}$	O	This line will go low during C1M when the address bus contains an address between $C000 and $CFFF. This line will drive 12 LSTTL loads.
21	RDY	I	The 6502's RDY input. This line should change only during C1M, and when low will halt the microprocessor on the next read cycle. This line has a 1K ohm pullup to +5V. This line should be driven from an open collector output.
22	$\overline{\text{TSADB}}$	I	A low on this line from the peripheral will cause the address bus to tri-state for Direct Memory Access (DMA) applications. This has a 1 K ohm resistor pullup to +5V. This should be driven from an open collector output.
23		NA	Not used in an Apple ///(NO DAISY CHAINING OF PERIPHERALS)
24		NA	Not used in an Apple ///.
25	+5V	O	Positive 5-volt supply, 2.0 amps total for all peripheral boards together (but note a limit of 1.5 Watts per board).
26	GND	NA	System circuit ground. 0 volt line from power supply. Do not use for shield ground.
27	DMAOK	O	Acknowledge signal to the peripheral following

			its request for the special Direct Memory Access (DMA) mode. Informs the peripheral that the DMA can now proceed.
28	$\overline{\text{DMAI}}$	I	Direct Memory Access (DMA) interrupt. Requests the A Apple /// DMA mode. Has a 1 K ohm pullup to +5. This should be driven from an open collector output.
29	$\overline{\text{IONMI}}$	I	Input/Output Non-Maskable Interrupt. This is equivalent to the IORES (pin 31) line as it will execute the same code in the Autostart ROM. This line should be driven by an open collector output. THE NMI DOES NOT GO DIRECTLY T THE PROCESSOR, SO IT CAN BE MASKED BY THE SYSTEM RESET FUNCTIO
30	$\overline{\text{IRQ}}$	I	This line is ignored in Apple][emulation mode. It should be driven by a TTL output.
31	$\overline{\text{IORES}}$	O	Input/Output Reset signal used to reset the peripheral devices. Pulled low by a power on or RESET key. This line will drive 12 LSTTL loads.
32	$\overline{\text{INH}}$	I	Inhibit line. When a device pulls this line low, all system memory is disabled. This line has a 1 K ohm pullup resistor to +5V and should be driven form an open collector output.
33	-12V	O	Negative 12 volt supply, 200mA total for all peripheral boards together.
34	-5V	O	Negative 5 volt supply, 200mA total for all periperal boards together.
35	SYNC	O	The 6502 opcode synchronization signal. Can be used for external bus control signals. Will drive 10 LSTTL loads.
36	C7M	O	Seven MHz high frequency clock. Will drive 10 LSTTL loads.
37	Q3	O	A 2MHz (nonsymetrical) general purpose timing signal. Will drive 10 LSTTL inputs.
38	$\overline{\text{C1M}}$	O	Complement of C1M clock. This will drive 12 LSTTL loads.
39	$\overline{\text{IOCLR}}$	O	Provides the $C800 space disable function directly without address decoding ($CFFF is used for Apple][peripherals. It is addressed from $C02x. This line will drive 12 LSTTL loads.
40	$\overline{\text{C1M}}$	O	Phase C1M clock. This is the same as the microprocessor's 1 MHz clock. This will drive 12 LSTTL loads.
41	$\overline{\text{DEVICE SELECT}}$		This line becomes acive (low) on each peripheral

			connector when the address bus is holding address between $C0n0 and $C0nF where n is the slot number plus $8. This line will drive 12 LSTTL loads.
42-49	D7-D0	I,O	The 8-bit system data bus. During a write cycle, data is set up by the 6502 less than 300ns after the beginning of $\overline{\text{C1M}}$. During a read cycle the 6502 expects data to be ready no less than 100ns before the end of $\overline{\text{C1M}}$. These lines will drive 8 LSTTL inputs.
50	+12V	O	Positive 12 volt supply*, 300mA total for all peripheral boards together.

* NOTE: TOTAL POWER DRAWN BY ANY ONE PERIPHERAL BOARD IS NOT TO EXCEED 1.5 WATTS

The Real Time Clock/Calendar

A real time clock has been incorporated into the A /// using 58167 CMOS Clock/Calendar chip. This chip has the resolution to count to thousandths of a second. The clock circuitry can be set to cause an interrupt at intervals from a tenth of a second to interrupts every month.

Since the clock is a CMOS circuit it consumes about 10ua in the standby (power off in the Apple ///) mode. This is about the same as a normal LCD watch. Three "AA" alkaline batteries are mounted in a battery pack that clips to the casting near the internal speaker. Wires attached to the battery holder connect to a 2 pin molex connector at location G13.

This clock chip is not a member of the 6500 family and is not directly compatible. Special considerations have been incorporated into the logic design to allow the Apple III to access and control of the clock chip.

The timing requirements for the clock chip require that the address lines be latched for much longer than the processor can accomplish in normal operations, so the clock is addressed with the "Zero Page Register" (the B port of VIA B6). The operating system will temporarily store the current zero page address at another location then write the desired clock address into the zpage register. The processor clock, PH0, is extended to --usec by the action of the prom 180 and associated circuit. The clock chip also requires a separate read and write strobe so appropriate logic was designed to split the R/W signal into a read and write strobe.

When the processor has completed its access to the clock it will return the proper zero page address to the VIA and PH0 will return to its normal operation.

Please refer to the specification sheet in the Appendices for complete details of the clock.

The transistor array performs two functions. One it supplies Vcc from the power supply when the Apple /// is "on", and develops a power down strobe to the clock chip to set its standby mode just before the supply fully decays.

The clock may be programmed that while it is in the standby mode to provide a PDINT to an external device which may restore power to the Apple to service a particular device. This feature would be very useful in communications networks that poll at specific times in off-hours. However, at the time of this printing no such remote device has been specified.

The clock runs on a 32KHZ crystal may be adjusted to an operating tolerance of 5 minutes a month. There are two methods used, on is a vertifications of operation using software, this however has the accuracy of approximately 5 minutes a month, which for many applications and users is close enough, but for those users who demand a closer setting a method of setting the clock using an accoustic probe and frequently meter is available. The only problem with this is the cost of the calibration equipment (nearly $1000 per station). Level II centers will most likely be equipped with these devices.

It should be noted that there is a slight shift if frequently between power on and standy modes. Depending on the actual usage of power on and off the clock may vary perceptibly over the course of a month. So it is best to describe the entire function as a clock, not a chronograph.

•

THE KEYBOARD

The Apple /// has a built-in 74 key typewriter-like keyboard which includes full alpha/numerics, four cursor control keys, two special function keys, and a numeric keypad. It has full upper and lower case ASCII code generation capability as well as full incorporation of Apple][functions.

The drawing on the previous page shows the standard keyboard legend and details the keystation number. Note that in addition to the 74 keys there is a recessed Reset key. Every key on the keyboard can be observed individually by the soft- ware. The Control and Shift keys modify the key codes when presented to the system.

The keyboard is electrically connected to the main circuit board by a 26 conductor ribbon cable. The cable plugs into a socket on the keyboard and the main circuit board. The signal assignment is shown on the Pin Signal Assignment table.

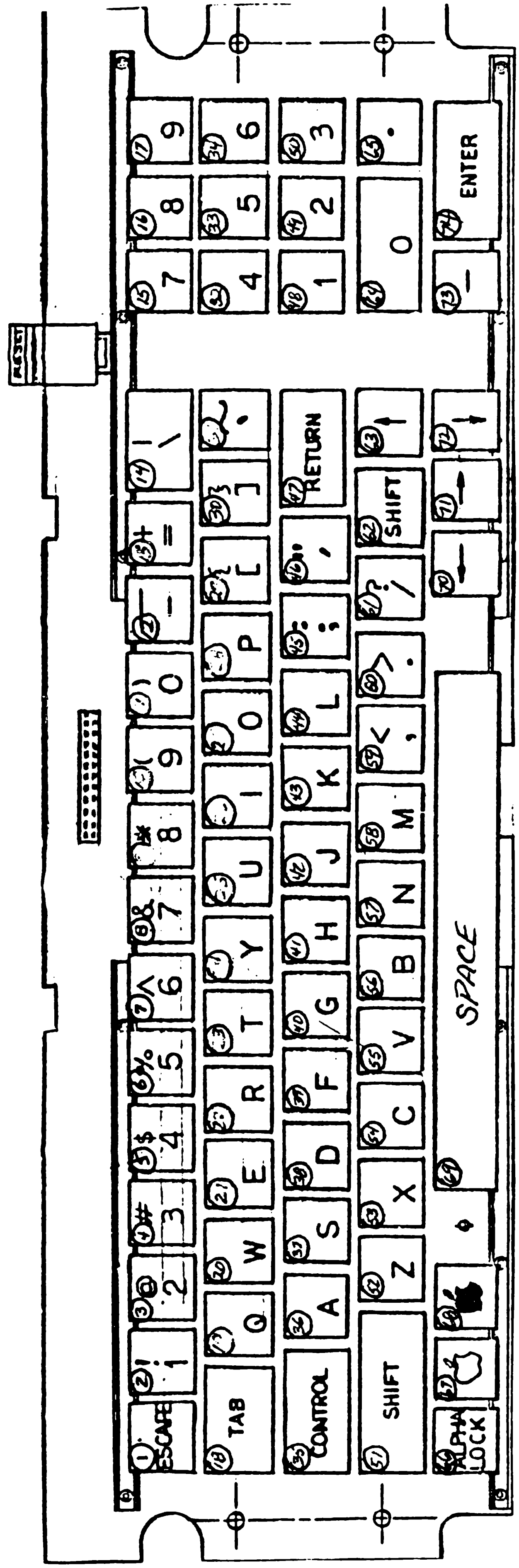
Repeat Functions

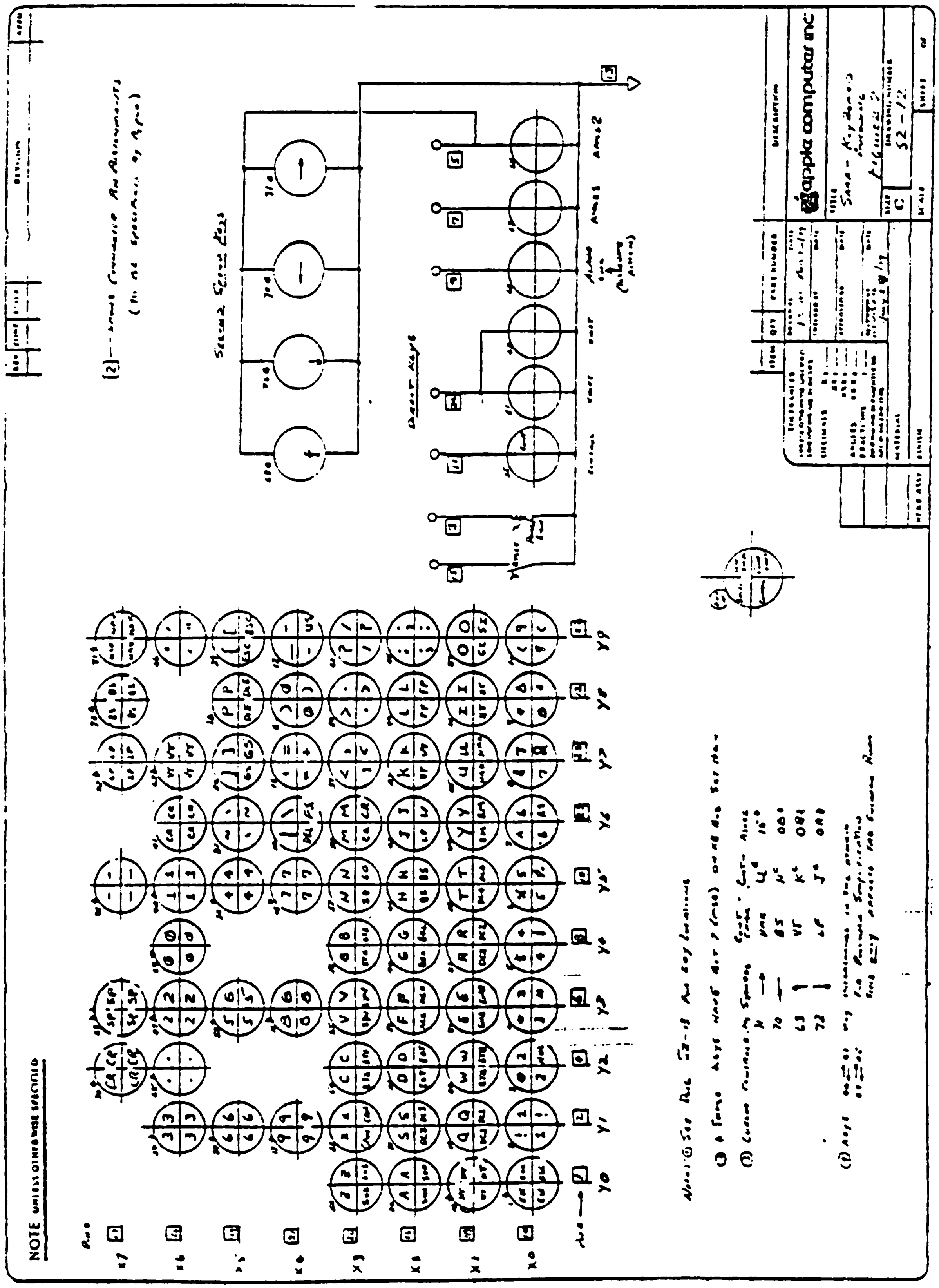
Any key held down for more thn 1/2 second is automatically activated to repeat at a 10 CPS rate. A high speed (30 CPS) repeat function is activated by holding down the closed Apple key (Key #68) after depressing and holding the key to be repeated. An idiosyncracy of the Apple /// is that if the closed Apple key is depressed before another key, it is displayed as only one character. If it is depressed after another key, the high speed repeat is activated.

The four cursor control keys (63, 70, 71, 72) are two-contact keys. This means that as the key is partially depressed, it makes its first contact generating a signal code. When it is fully depressed, it will make a second contact, automatically activating a high speed repeat of that key.

READING THE KEYBOARD

The keyboard can be thought of as two hardware ports (busses) that can provide two distinct types of data. The first type is ASCII, which is addressed by Memory Address C000; we will call this the KA port. The KA port always contains the lower 7 bits of the ASCII code and, like the Apple][, uses the MSB as a "keyboard data ready" flag. The second type of data is addressed by Memory Address C008; we call this the KB port. The KB port looks at the "direct connect" keys and at the eighth bit of the key code. A summary of the bit meanings for these two types of data is shown in the table at the top of the following page.


ESCAPE
TAB
CONTROL
SHIFT
ALPHA LOCK
SPACE
RETURN
SHIFT
ENTER
RESET


NOTE UNLESS OTHERWISE SPECIFIED
X7
X6
X5
X4
X3
X2
X1
X0
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
apple computer inc
C
S2-72

KEYBOARD ENCODER MATRIX

	KEYBOARD VERTICAL Y							KEY PAD
Y0	A	Z	ESC	TAB				NONE
Y1	1	Q	S	X				9 6 3
Y2	2	W	D	C				. ENTER
Y3	3	E	F	V	SPACE			8 5 2
Y4	4	R	H	B				0
Y5	5	T	G	N				7 4 1 -
Y6	6	|\	Y	~\	J	M	RETURN	NONE
Y7	7	+=	U	}·]	K	<,	↑ ↓	NONE
Y8	8	0	I	P	;:	←	> .	NONE
Y9		9	§[	O	" '	L	?/	NONE

	KEYBOARD HORIZONTAL X										KEY PAD
X0	ESC	1	2	3	4	5	6	7	8	9	NONE
X1	TAB	Q	W	E	R	T	Y	U	I	O	NONE
X2	A S	D	F	G	H	J	K	L		;	NONE
X3	Z X	C	V	B	N	M	<,	>.	? /		NONE
X4	0	_ -	+	=	|\						7 8 9
X5	P	{ [	}]	~\							4 5 6
X6	" '	RETURN	↑								1 2 3 . 0
X7	SPACE	←	→	↓							- ENTER

****

MEMORY ADDRESS REFERENCE

****

	KA PORT (C000)			KA PORT (C008)
Bit 0	ASCII Bit 0	*	Bit 0	"1"="any key down"
Bit 1	ASCII Bit 1	*	Bit 1	"0"="shift depressed"
Bit 2	ASCII Bit 2	*	Bit 2	"0"="control depressed"
Bit 3	ASCII Bit 3	*	Bit 3	"0"="alpha lock set"
Bit 4	ASCII Bit 4	*	Bit 4	"0"="Apple 1 switch depressed"
Bit 5	ASCII Bit 5	*	Bit 5	"0"="Apple 2 switch depressed"
Bit 6	ASCII Bit 6	*	Bit 6	"1"="start up uncommitted mode"
Bit 7	"1"="data ready flag"	*	Bit 7	ASCII Bit 7

****

The KA data is used exactly like that in the Apple][keyboard. The KB data is provided for function expansion. The KB ports 1 to 5 are direct mechanical connections to defined function switches. Bit 0 is an output from the encoder circuity and bit 7 is the eighth bit of the key code. Bit 6 is a special bit, a flag used during turn-on to show that the operational mode (Apple /// or Apple][) has not yet been determined..

It should be noted that the Reset key cannot act on its own but has to be depressed with another key. This is a safety feature to prevent blowing away a good night's programming effort. Now isn't that nifty!? A CONTROL- RESET will give a true system reset. However, it cannot be used for recovery from Apple][mode. The CONTROL-RESET will also give the system an NMI (Non-Maskable Interrupt). This provides Apple /// with two levels of "reset."

KEYBOARD CODES

A complete list of the codes generated by the encoder circuitry is presented is the following table:

Table: Apple /// KEYBOARD CODES (HEX)

Key #	Key Name	US	SH	CT	SU-CT
1*	ESCAPE	9B	9B	9B	9B
2	1	31	21	31	31
3	2	32	40	32	00
4	3	33	23	33	23
5	4	34	24	34	24
6	5	35	25	35	25
7	6	36	5E	36	53
8	7	37	26	37	26
9	8	38	2A	38	2A
10	9	39	28	39	28
11	0	30	29	30	29
12	-	2D	5F	2D	1F
13	=	3D	2B	3D	2B
14	BACKLASH	5C	7C	7F	1C
15*	7	B7	B7	B7	B7
16*	8	B8	B8	B8	B8
17*	9	B9	B9	B9	B9
18*	TAB	89	89	89	89
19	Q	51	51	11	11
20	W	57	57	17	17
21	E	45	45	05	05
22	R	52	52	12	12
23	T	54	54	14	14
24	Y	59	59	19	19
25	U	55	55	15	15
26	I	49	49	09	09
27	O	4F	4F	0F	0F
28	P	50	50	10	10
29	RT-BRACK	5B	7B	1B	1B
30	LT-BRACK	5D	7D	1D	1D
31	LT-BRACK	60	7E	60	7E
32*	4	B4	B4	B4	B4
33*	5	B5	B5	B5	B5
34*	6	B6	B6	B6	B6
35	CONTROL	-----KB-2------			
36	A	41	41	01	01
37	S	53	53	13	13
38	D	44	44	04	04
39	F	46	46	04	04
40	G	47	47	07	07
41	H	48	48	08	08
42	J	4A	4A	0A	0A
43	K	4B	4B	0B	0B
44	L	4C	4C	0C	0C
45	;	3B	3A	3B	3A
46	'	27	22	27	22
47	RETURN	0D	0D	0D	0D
48*	1	B1	B1	B1	B1
49*	2	B2	B2	B2	B2
50*	3	B3	B3	B3	B3
51	SHIFT	-----KB-1------			
52	Z	5A	5A	1A	1A
53	X	58	58	18	18
54	C	43	43	03	03
55	V	56	56	16	16
56	B	42	42	02	02
57	N	4E	4E	0E	0E
58	M	4D	4D	0D	0D
59	,	2C	3C	2C	3C
60	.	2E	3E	2E	3E
61	/	2F	3F	2F	3F
62	SHIFT	-----KB-1-------			
63*	UP-CURSOR	8B	8B	8B	8B
64*	0	B0	B0	B0	B0
65*	.	AE	AE	AE	AE
66	ALPHA-LK	-----KB-3------			
67	APPLE 1	-----KB-4------			
68	APPLE 2	-----KB-5------			
69*	SPACE	A0	A0	A0	A0
70*	LT-CURSOR	8B	8B	8B	8B
71*	RT-CURSOR	95	95	95	95
72*	DN-CURSOR	8A	8A	8A	8A
73*	-	AD	AD	AD	AD
74*	ENTER	8D	8D	8D	8D

* Bit 7 (MSB) on these keys appears on bit 7 of KB port, on the KA port.

Note: the keys on the numeric keypad have only one code. *Shift and Control* have no effect on these keys.

THE APPLE II EMULATION MODE

In this mode the Apple /// special functions are locked out, making the keyboard look exactly like the Apple][. Thus, the Apple][software does not look at the KB port and must get all the Apple][codes for the KA port. This is the reason for coding and bit arrangements. However, the Apple /// functions are not really locked out and could be read by an enterprising programmer, if desired.

Some of the keyboard codings which should be noted because of the Apple II emulation mode are:

1. "NUL" is a control-@ (Control-Shift-2). With the Apple][, the "NUL" is a Control-Shift-p.
2. "RS", record separator, is a control-Shift-6, which corresponds to control-Shift-n in the Apple][.
3. The Shift-m, for a left square bracket in the japple][, is not available in the emulation mode since the character is represented on the keyboard. The "GS", group separator, is a Control-left bracket rather than the Control-Shift-m.
4. "BS", backspace, has been retained for the left arrow and "NAK", negative acknowledgment, for the right arrow for both the Apple][and Apple /// modes.
5. "VT", vertical tab, and "LF, line feed, were chosen for the up and down cursor keys. In the Apple][mode these will not give a cursor movement (unless the operating system is changed) but will give the Control-k and Control-j codes. This could cause some slight confusion for those Apple][programs that use those codes (...now he tells me!).
6. The autorepeat and high speed repeat functions will work for the Apple][just like they do in the Apple /// mode. Nice!

ELECTRONIC CIRCUIT DESCRIPTION

Please refer to sheet 9 of 10 of the Schematic (Drawing Number 050-0039) for the following Keyboard Logic circuit description.

The Apple /// keyboard is simply an 8 by 10 X,Y matrix which is scanned by the encoder circuit [keyboard encoder rom H14] on the main logic board. All keys are scanned with the exception of five keys [shift, control, capslock, Apple1, Apple2] that are direct connected. The second contacts of the cursor keys (*high speed* repeat function are OR'd wired into the Apple2 switch line on KB-5.

On the main board the encoder scans the keyboard matrix and provides the correct code outputs plus a strobe and an "any key down" signal. A diagram for the key matrix shows the key locations, and their ASCII character representations are shown on the following page. The special function keys can be detected separately from the standard control keys by observing that the MSB of the KB port is set high.

The A3 signal to the Tri-state data selectors (LS257's) selects whether the output of the LS257 will be a KA or KB port. If A3 is high, selected by memory address C008, the KB port is selected. The KBD line enable the reading of data off the keyboard.

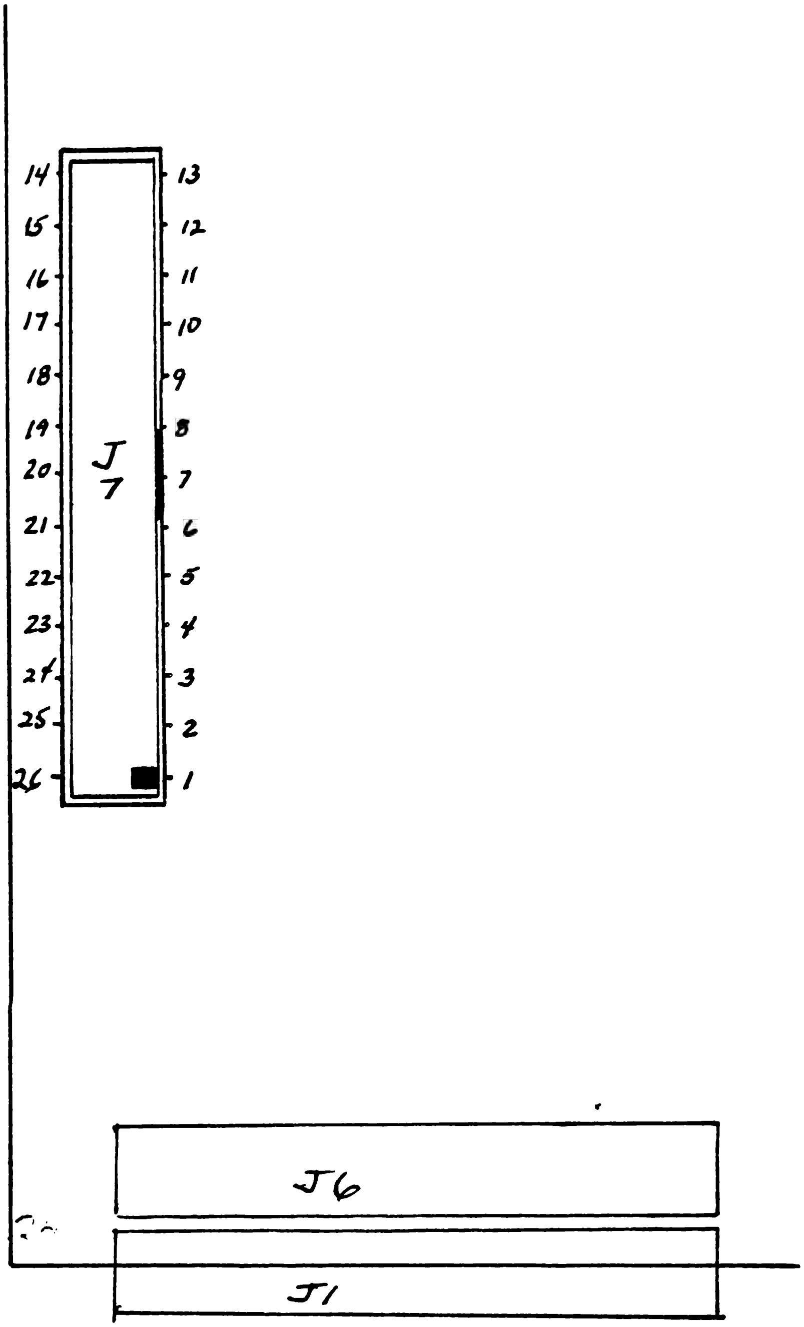
The Repeat Function: The normal repeat function (10 cps) that occurs when a key is held down is the result of clocking and resetting the flip-flop H11 (feeding into H12). This is accomplished by the AK (any key) and DTRDY (data ready) setting, H11 then having CLRSTB (clear strobe) resetting the flip-flop. The Apple2 key, when depressed after a character key, engages the high-speed repeat function. The combination of the Apple2 key signal clocking the edge triggered flip-flop (H11), and pulse change to the inputs of the 556 (L10) dual timers speeds up the timing.

The Reset Function: The power on reset is provided by the one shot (A5). Depressing the reset key results in a soft reset. This causes the KRESET line to go low and enable the LS139 (J11). If the Control key and the Reset key are both depressed, a hard reset results. This hard reset can be foiled through sophisticated programming. The RESETLK (reset lock signal) provided from the Environmental Register [6522 - B6], can disable the Reset and NMI. (Try it!)

Keyboard Light: The keyboard light indicates the VCC is provided to the keyboard. If no light is observed, check Q9 [MPV 51].

PIN SIGNAL ASSIGNMENT

Pin #	Description
1	Y0
2	Y1
3	Power Light
4	Y2
5	Apple 2 (high speed repeat)
6	Y3
7	Apple 1
8	Y4
9	Alpha Lock (alternate action)
10	Y5
11	Control
12	Y8
13	Signal Ground
14	X0
15	Reset
16	X2
17	X7
18	X2
19	X5
20	X3
21	X4
22	Y9
23	Y6
24	Shift (both keys)
25	Y7
26	X6

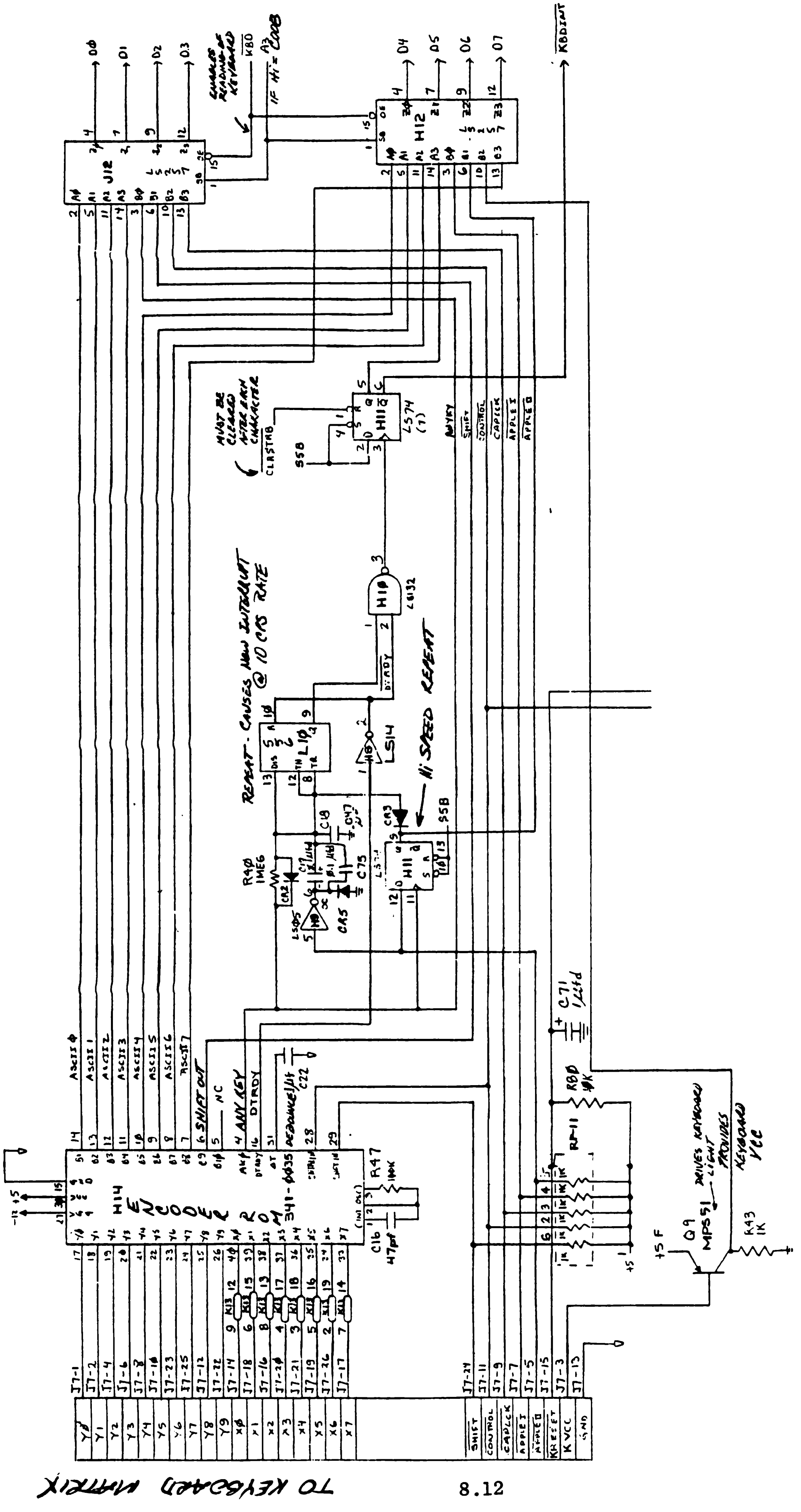


$ = REPRESENTS HEXADECIMAL

Table 2: Keys and their Associated ASCII Codes (Bit 7 always set)

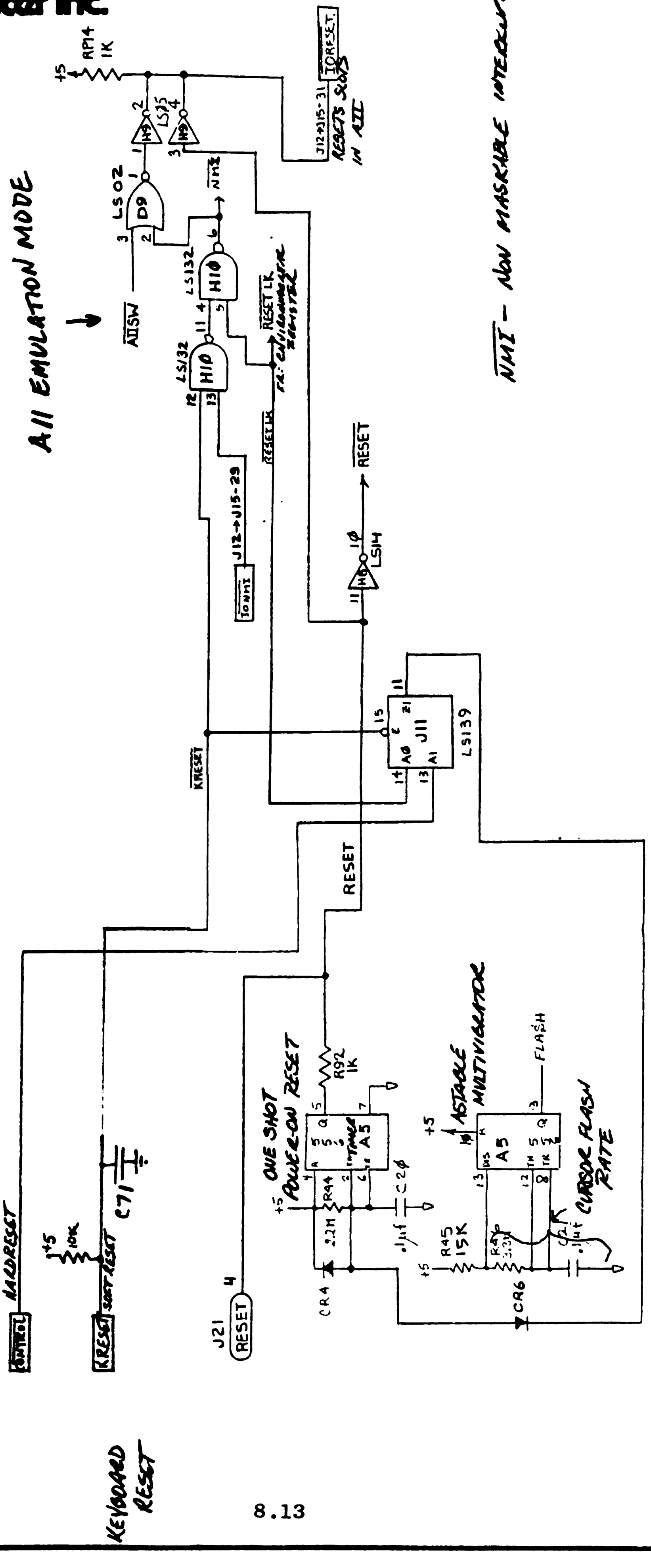
Key	Alone	CONTROL	SHIFT	Both
<space>	$A0	$A0	$A0	$A0
ESCAPE	$9B	$9B	$9B	$9B
1!	$B1	$B1	$A1	$A1
2@	$B2	$B2	$C0	$80
3#	$B3	$B3	$A3	$A3
4$	$B4	$B4	$A4	$A4
5%	$B5	$B5	$A5	$A5
6^	$B6	$B6	$DE	$9E
7&	$B7	$B7	$A6	$A6
8*	$B8	$B8	$AA	$AA
9(	$B9	$B9	$A8	$A8
0)	$B0	$B0	$A9	$A9
-_	$AD	$AD	$DF	$9F
=+	$BD	$BD	$AB	$AB
\\|	$DC	$9C	$FC	$FF
TAB	$89	$89	$89	$89
[{	$DB	$9B	$FB	$9B
]}	$DD	$9D	$FD	$9D
'"	$A7	$A7	$A2	$A2
RETURN	$8D	$8D	$8D	$8D
,<	$AC	$AC	$BC	$BC
.>	$AE	$AE	$BE	$BE
/?	$AF	$AF	$BF	$BF
<left arrow>	$88	$88	$88	$88
<right arrow>	$95	$95	$95	$95
<up arrow>	$8B	$8B	$8B	$8B
<down arrow>	$8A	$8A	$8A	$8A
.	$AE	$AE	$AE	$AE
-	$AD	$AD	$AD	$AD
ENTER	$8D	$8D	$8D	$8D
A	$C1	$81	$C1	$81
B	$C2	$82	$C2	$82
C	$C3	$83	$C3	$83
D	$C4	$84	$C4	$84
E	$C5	$85	$C5	$85
F	$C6	$86	$C6	$86
G	$C7	$87	$C7	$87
H	$C8	$88	$C8	$88
I	$C9	$89	$C9	$89
J	$CA	$8A	$CA	$8A
K	$CB	$8B	$CB	$8B
L	$CC	$8C	$CC	$8C
M	$CD	$8D	$CD	$8D
N	$CE	$8E	$CE	$8E
O	$CF	$8F	$CF	$8F
P	$D0	$90	$D0	$90
Q	$D1	$91	$D1	$91
R	$D2	$92	$D2	$92
S	$D3	$93	$D3	$93
T	$D4	$94	$D4	$94

U	$D5	$95	$D5	$95
V	$D6	$96	$D6	$96
W	$D7	$97	$D7	$97
X	$D8	$98	$D8	$98
Y	$D9	$99	$D9	$99
Z	$DA	$9A	$DA	$9A


TO KEYBOARD MATRIX
H14 ENCODER ROM 341-0035
J12
H12
H11 LS74
L10
H10 LS132
H8 LS14
H8 LS05
R40 1MEG
C17 .1 1ꟸ
C18 .047 µF
C75
CR2
CR3
CR5
C16 47pf
R47 100K
C22
C71 1µfd
R80 10K
RP-11
Q9 MPS51
R43 1K
+5F
ASCII 0
ASCII 1
ASCII 2
ASCII 3
ASCII 4
ASCII 5
ASCII 6
ASCII 7
SHIFT OUT
NC
ANY KEY
DTRDY
DEBOUNCE
D0
D1
D2
D3
D4
D5
D6
D7
KBD
CHARGE READING OF KEYBOARD
IF Hi = C00B
A3
KBDINT
MUST BE CLEARED AFTER EACH CHARACTER
CLRSTRB
SSB
ANYKEY
SHIFT
CONTROL
CAPLCK
APPLE I
APPLE O
REPEAT - CAUSES NEW INTERRUPT @ 10 CPS RATE
Hi SPEED REPEAT
DRIVES KEYBOARD LIGHT
PROVIDES KEYBOARD VCC
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
X0
X1
X2
X3
X4
X5
X6
X7
SHIFT
CONTROL
CAPLCK
APPLE I
APPLE O
KRESET
KVCC
GND
J7-1
J7-2
J7-4
J7-6
J7-8
J7-10
J7-23
J7-25
J7-12
J7-22
J7-14
J7-18
J7-16
J7-20
J7-21
J7-19
J7-26
J7-17
J7-24
J7-11
J7-9
J7-7
J7-5
J7-15
J7-3
J7-13
-12
+5

apple computer inc.

RESET



NMI - NON MASKABLE INTERRUPT.

THE APPLE /// POWER SUPPLY

The Apple /// power supply converts power from the AC line to DC. This is a constant voltage power supply. This means:

1. The output voltage is maintained constant regardless of changes in the load, line, or temperature.
2. The Apple /// power supply is a free running flyback type, off line switching power supply.
   - It can accept either 115VAC or 230VAC (jumper selectable) and delivers 4 regulated DC outputs at a total of 55 watts.
   - It supplies +5, -5, +11.8, and -12VDC.
   - It is called a flyback type power supply because energy is transferred from the primary of the transformer to the secondary when the switching transistor switches off (during flyback).

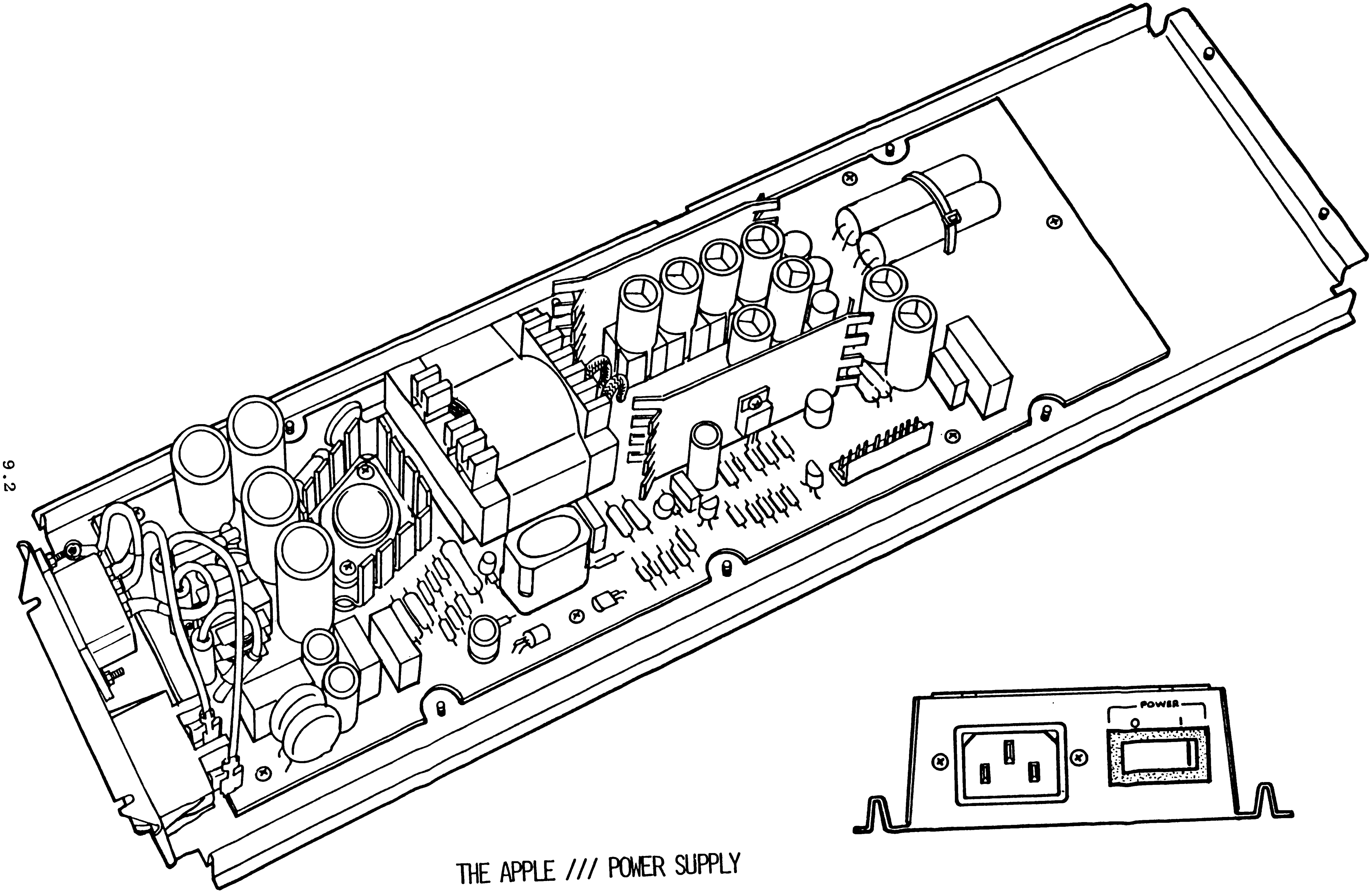
The following paragraphs will describe the switching power supply in more detail.

THE BASIC SWITCHING POWER SUPPLY

The regulating element of the switching power supply consists of a transistor that acts as a rapidly opened and closed switch. The AC input is rectified to unregulated DC, then "chopped" by the switching element components at a fast rate, approximately 25kHz. The resultant is transformer-coupled to an output network which provides the final rectification and filtering. Regulation is accomplished through control circuits that vary the on-off periods (duty cycles) of the switching components.

Advantages

1. Greater Efficiency
   - Lower power is dissipated because of the on/off role of the regulator. The switching transistors dissipate very little power when either saturated (on) or cutoff (off). With less wasted power, the switching power supply runs at cooler temperatures and costs less to operate.
2. Size and Weight
   - Because components such as capacitors, transformers, and inductors operate at high switching rates they can be smaller and weigh less than those that operate at power line frequencies.
3. Operating Conditions
   - The switching power supply can operate under low AC conditions and can sustain (holdup) its output if input power is momen-



THE APPLE /// POWER SUPPLY
PARTS LAYOUT

tarily lost. This is because the AC input is rectified and the filter capacitors charge to peak voltages on the AC line.

Disadvantages

1. Transient Recovery Time

   - The dynamic loading regulation is slower than that of the series regulated supply. The recovery is limited mostly by the inductance of the output filter network.

2. EMI (Electro-Magnetic Interference)

   - This is a natural byproduct of this type of power supply. This EMI can be conducted to the load (resulting in higher output ripple and noise), and it can be conducted back into the AC line. (Now you know where that stuff on TV came from).

   - Apple designed this power supply with filter networks and shielding to greatly reduce EMI.

HOW IT WORKS!

Regulation is accomplished by a switching transistor Q2 operating under control of a feedback network. The feedback network, consisting of a voltage comparitor and blocking oscillator, controls the duty cycle of the oscillator.

The energy is transferred from the primary to the secondary of the transformer and delivered to the output rectifier/filter. Here the waveform is rectified and averaged to provide a DC output level that is proportional to the duty cycle of the waveform.

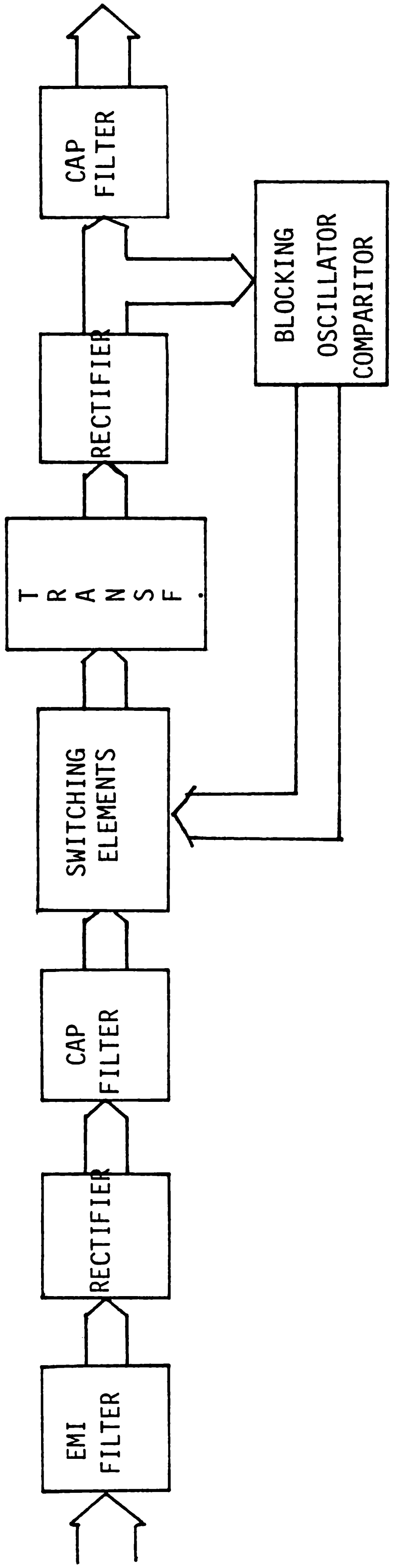
Referring to the block diagram, Figure x.x below, note that:

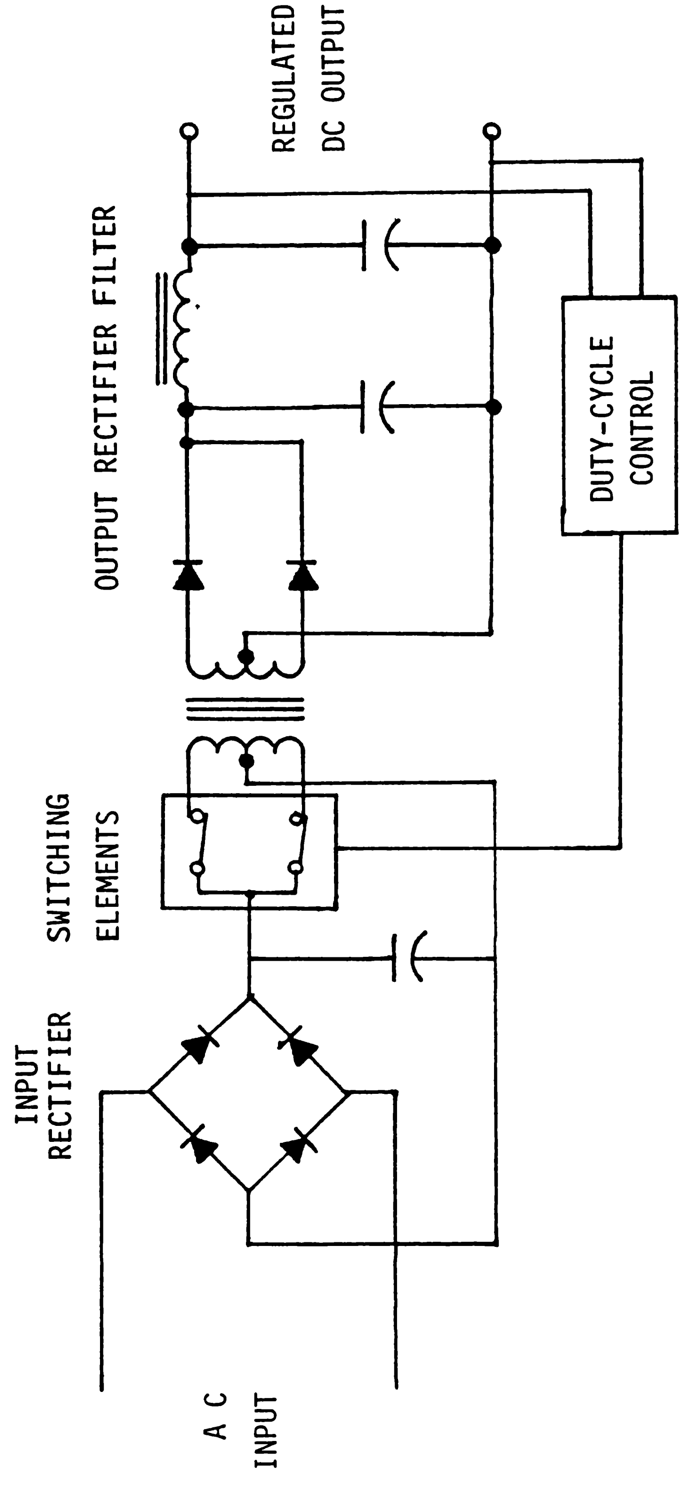
- The AC is passed through an EMI filter and then rectified to provide approximately 300 VDC across the capacitive input filters (C6, C7, C8, C9 of the schematic diagram). This voltage is applied to the primary of the transformer (T2) by the switching elements (turning on power transister Q2). A linear current ramp is developed by the primary inductance of the transformer.

- When the switching elements are turned off, the energy stored in the transformer is transferred to a second set of rectifiers through a capacitive filter network to provide filtering of the output.

- The +5 volt output of the final rectifier network is compared to a reference voltage, and the error is fed back to a blocking oscillator.

- The blocking oscillator basically changes the frequency depending on the output voltage. This in turn changes the repetition rate of the switching elements, which changes the energy transfer through the transformer and voltage output. This is how regulation is accom-


EMI FILTER
RECTIFIER
CAP FILTER
SWITCHING ELEMENTS
T R A N S F .
RECTIFIER
CAP FILTER
BLOCKING OSCILLATOR COMPARITOR


REGULATED
DC OUTPUT
OUTPUT RECTIFIER FILTER
DUTY-CYCLE
CONTROL
SWITCHING
ELEMENTS
INPUT
RECTIFIER
A C
INPUT

plished.

- o If the output voltage should change in such a way that the blocking oscillator goes into saturation, the output is essentially cut off.

DETAILED HARDWARE DESCRIPTION [Refer to Schematic]

A THERMISTOR, R1, is used to limit AC input surge current by its negative temperature coefficient of resistance. When cold, during turn on, R1 has a high resistance; after it heats up, R1 has a low resistance.

VDR1 is a varistor and is used as a transient suppressor. It keeps voltage spikes that result from power supply switching from affecting the performance of the power supply. It basically provides AC line surge current protection at turn on.

THE AC LINE SELECTABLE JUMPER, when connected to 220V position, causes the power supply to act as a conventional full wave rectifier. For 120V AC inputs the input circuitry becomes a voltage doubler.

THE EMI FILTER made up of T1, L1, L2, and C1, helps prevent high frequency RFI spikes from being conducted to the load or back into the AC line.

DB1 is a diode rectifier bridge.

THE SWITCHING ELEMENT consists of the circuitry associated with Q2 and Q1. You may recall that the linear current ramp, developed in the primary of the transformer when Q2 is turned on, is transferred to the secondary when Q2 is turned off.

The turn on of Q2 is accomplished by R2 for starting, and thereafter by the feedback winding in T2 driven by R4 and C10. This winding initiates turn on during the ringdown following the flyback.

If a sufficient voltage is developed across R9, Q1 will be forward bias. This would occur if by chance one of the output voltages were shorted. In that case, the oscillator would stop and shut off all the outputs, pause for 1/2 second, and attempt to restart.

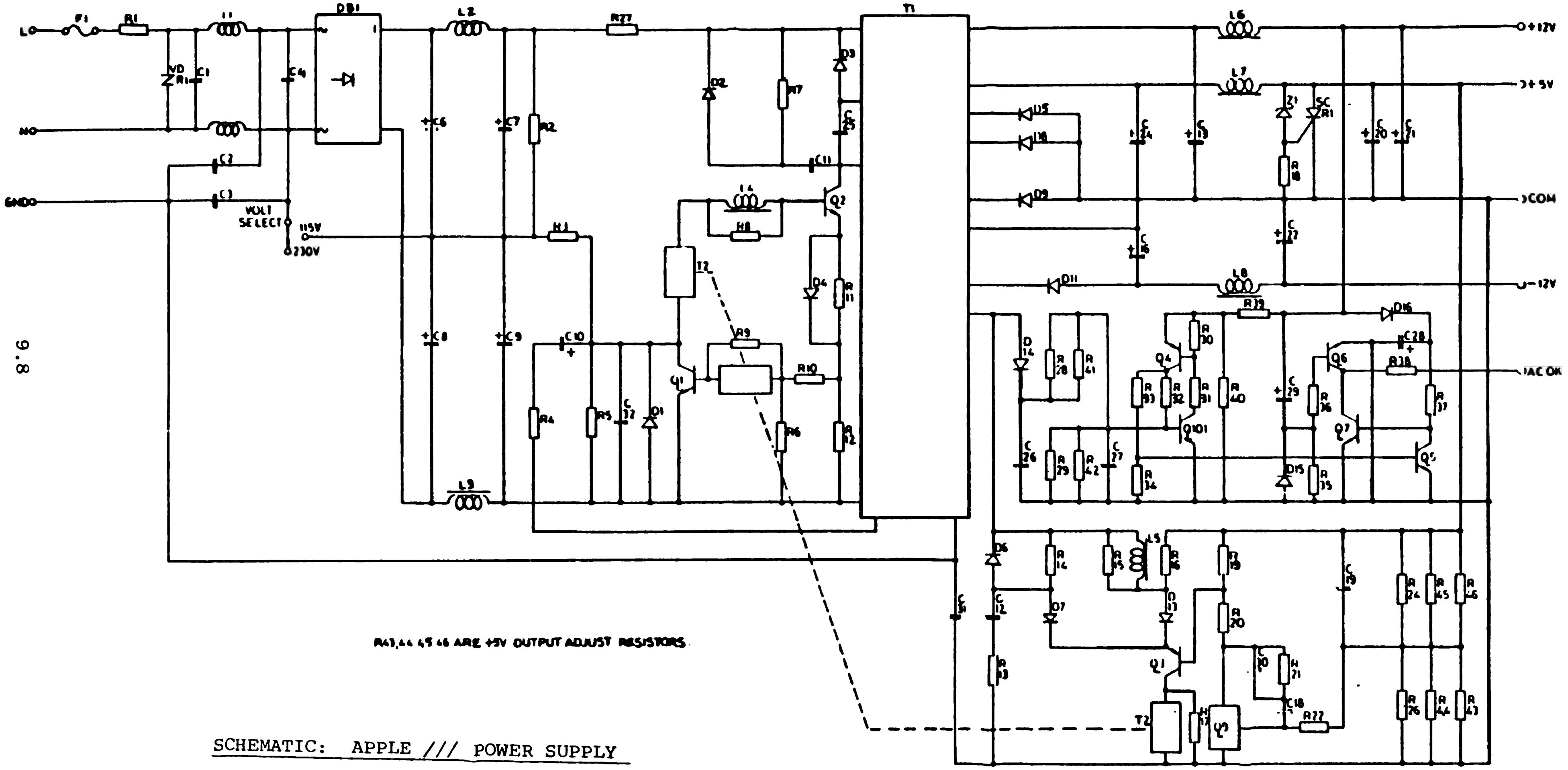
THE OUTPUT RECTIFIER DIODES, D7 through D12, provide rectification, but also protect internal components against reverse currents that could be injected into supply by an active load.

IC1 helps accomplish regulation by comparing the output voltage against its own internal reference and delivering a voltage level to the base of Q3.

The emitter of Q3 is driven by a positive going ramp created by the inductive resistance associated with R14 while Q2 is on. When this voltage is sufficient to forward bias the emitter-base junction of Q3, conduction of Q2 is terminated.

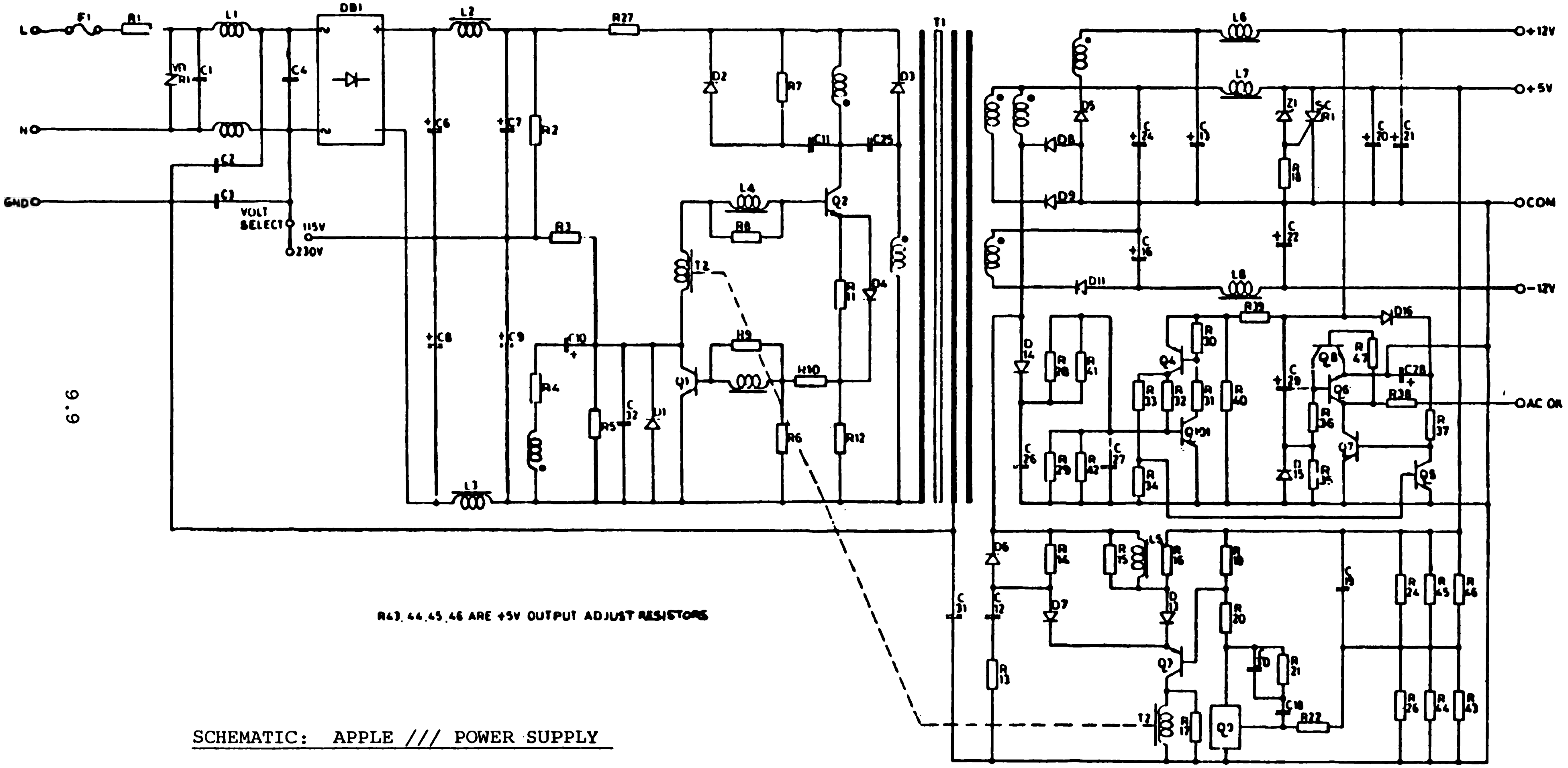
You can now see that the operating frequency varies with the line and load.

OVERVOLTAGE PROTECTION is accomplished by sensing the +12V level via the resistor voltage divider of R17 and R18, referenced to the zener voltage on Z1. When the +12V output rises above tolerance, Q4 is turned on, which in turn triggers SCR1. SCR1 then clamps the +12V to ground, causing the power supply to fold back.



R43,44 45 46 ARE +5V OUTPUT ADJUST RESISTORS

SCHEMATIC: APPLE /// POWER SUPPLY



R43,44,45,46 ARE +5V OUTPUT ADJUST RESISTORS

SCHEMATIC: APPLE /// POWER SUPPLY

APPLE III POWER SUPPLY

REF	DESCRIPTION	QTY	PART NUMBER
	AC Input Socket		149-00200020
	Connector Housing 1 CCT	1	138-00000170
	Crimp Terminal	1	403-02200510
	Double Side Tape Width=3x4mm	20	027-01400010
	Faston Tab	1	403-02200700
	Heatsink	1	398-00200060
	Insulator 298. 45X88.9MM	1	183-00101410
	Nut M3 P=0.5 MS/NP	2	394-00400011
	On/Off Switch	1	278-01100010
	Pan	1	403-01101810
	PHL Pan M.C Screw M#x12 P=0.5 BS/NP	2	391-20204141
	PHL Pan M.C Screw M3X8 P=0.5 BS/NP	3	391-20204061
	PHL Pan M/C Screw M3X8 P=0.5 BS/NP	1	391-20204021
	PVC Coating CU Wire 100MM UL1015	1	356-12200571
	PVC Coating CU Wire 80MM UL1015	1	357-11800545
	PVC Coating CU Wire 95MM UL1015	1	356-12200566
	Rectifier RG3B	3	226-10700011
	Resistor, 68K +-5% 1/4W, Carbon Film	2	240-68306022
	Resistor, 82K +-5% 1/4W, Carbon Film	2	240-82306022
	SCR C122u	1	227-13000010
	Solder Bar	1	366-00130010
	Solder Bar 60/40	0	366-00130010
	Spring Washer M3 BS/NP	10	392-00800031
	Standoff M3	8	393-00200100
BR1	Bridge Rectifier KBP10		226-30500010
C01	Cap, 0.22uf, 250VAC, Metallized Paper	1	068-22400010
C02	Cap 0.1uf, 250VAC, Metallized Paper	1	068-10400010
C03	Cap, 4700pf, 400 VAC, Ceramic	2	055-47220001
C04	Cap, 4700pf, 400 VAC, Ceramic	2	055-47220001
C05	Cap, 0.1uf, 400 V, Polyester	1	058-10400100
C06	Cap, 100uf, 250V, Electrolytic	4	057-101201170
C07	Cap, 100uf, 250 V, Electrolytic	4	057-101201170
C08	Cap, 100uf, 250v, Electrolytic		057-10120170
C09	Cap, 100uf, 250V, Electrolytic	4	057-101201170
C10	Cap, 100uf, 250V, Electrolytic	1	057-22120080
C11	Cap, 0.001uf, 3KV, Ceramic		055-10261328
C12	Cap, 22uf, 100V, Polyester	2	058-22400120
C13	Cap, 1000uf, 10V, Electrolytic	6	057-10220020
C14	Cap, 1000uf, 10V, Electrolytic	6	057-10220020
C15	Cap, 1000uf, 10V, Electrolytic	6	057-10220020
C16	Cap, 1000uf, 10V, Electrolytic	6	057-10220020
C17	Cap, 330uf, 16V, Electrolytic		057-33120080
C18	Cap, 22ouf, 10V, Electrolytic	1	057-22120060
C19	Cap, 0.22uf, 100V, Polyester	1	058-22300080
C20	Cap, 1000uf, 10V, Electrolytic		057-10220020
C21	Cap, 0.22uf, 100V, Polyester		058-22400120
C22	Cap, 1000uf, 10V, Electrolytic		057-10220020
C23	Cap, 330uf, 16V, Electrolytic	3	057-33120080
C24	Cap, 680uf, 16V, Electrolytic	1	057-68120010
C25	Cap, 330uf, 16V, Electrolytic	3	057-33120080
C26	Cap, 0.1/1KV, Ceramic	1	055-10360925
D01	Diode, Rectifier, RGP10A	1	226-10400050
D02	Diode, Rectifier, RGP10M	2	226-10400100
D03	Diode, Recitifier, RGP10M	2	226-10400100

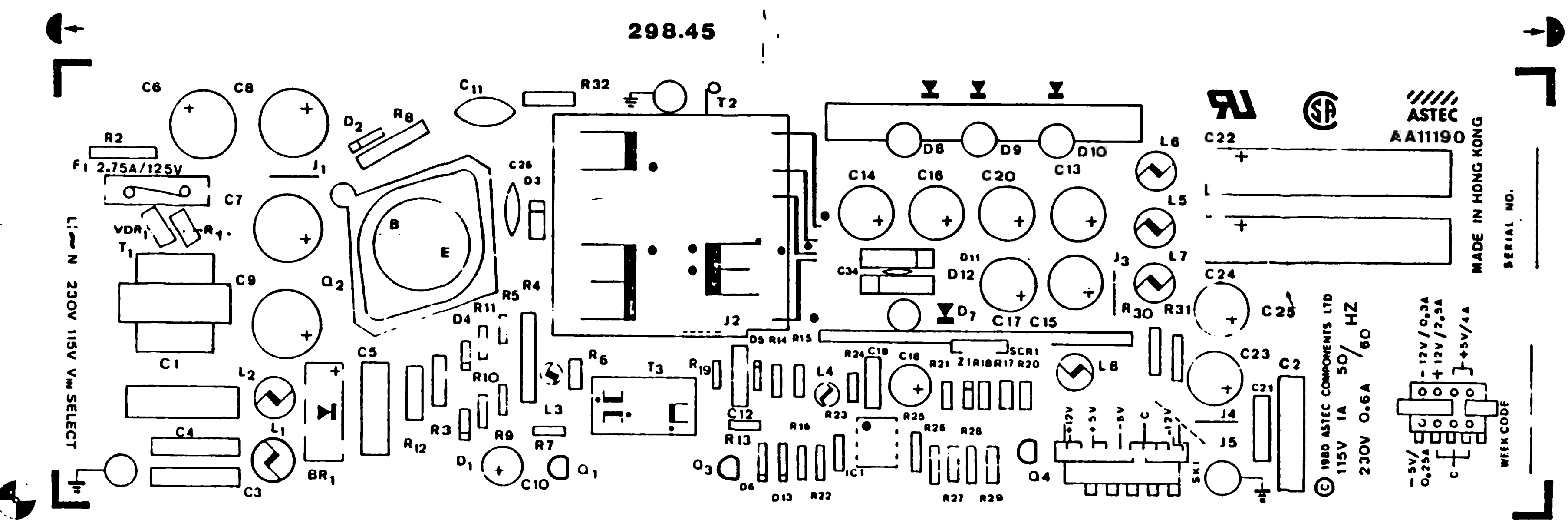
APPLE III POWER SUPPLY

REF	DESCRIPTION	QTY	PART NUMBER
D04	Diode, Rectifier, 1N4001GP	1	226-10400080
D05	Diode, Silicon, 1N5282	3	212-10700200
D06	Diode, Silicon, 1N5282	3	212-10700200
D07	Diode, Rectifier/Scr Assembly		853-00700010
D08	Diode, Rectifier assembly		853-00200140
D09	Diode, Rectifier Assembly		853-00200140
D10	Rectifier Assembly		853-00200140
D11	Schottky Diode S3SC3M		212-31100030
D12	Rectifier RG3B	1	226-10700010
D13	Diode, Silicon, 1N5282	3	212-10700200
F1	Fuse 2.75A 125V	1	084-00200040
IC1	Integrated Circuit, Regulator, TL431CP	1	211-10800070
J1	Jumper Wire	4	358-80810011
J2	Jumper Wire	4	358-80810011
J3	Jumper Wire	4	358-80810011
J4	Jumper Wire	40	358-80800001
L1	Choke	2	852-20100350
L2	Choke	2	852-20100350
L3	Base Choke	1	328-00100030
L4	Choke 1.5mH	1	328-00100010
L5	Choke Coil Assembly	1	852-20100010
L6	Choke Coil	1	852-10100370
L7	Choke Coil	1	328-00100060
L8	Choke Coil	1	328-00100060
Q1	Transistor SD467	1	209-11700463
Q2	Transistor 2SC1358	1	209-10200010
Q3	Transistor SB561	2	210-11700353
Q4	Transistor SB561	2	210-11700353
R01	Thermistor, 4R @25 C +-10% 6R @ 25 C +-20%	1	258-40970015
R02	Resistor, 150K +-5% 1/2W	2	240-15406033
R03	Resistor, 150K +-5% 1/2W		240-15406033
R04	Resistor, +-5% 47R 2W, Metal Oxide	1	248-47006063
R05	Resistor, +-5% 1/4W 1.2K	1	240-12206022
R06	Resistor, 5.6R +-5% 1/4W	1	240-56906022
R07	Resistor, +-5% 56R 1/4W, Carbon film		240-56006022
R08	Resistor, +5% 120R 2W	1	248-12106063
R09	Resistor, +-5% 1/4W 15R	2	240-15006022
R10	Resistor, +-5% 1/4W 10R, Carbon Film	1	240-10006022
R12	Resistor, 0.47R, Metal Film	1	247-04786054
R13	Resistor, -5% 1/4W 39R, Carbon Film	1	240-39006022
R14	Resistor, +-5% 270R 1/4W	2	240-27106033
R15	Resistor, +-5% 270R 1/4W, Carbon Film		240-27106033
R16	Resistor, 8.2 +-5% 1/4W, Carbon Film	1	240-82906022
R17	Resistor, +-5% 680R 1/4W	1	240-68106022
R18	Resistor, +-5% 1.8K, Carbon Film	1	240-18206022
	Resistor, +-5% 2.2K, Carbon Film	1	240-22206022
	Resistor, +-5% 2.7K 1/4W, Carbon Film	1	240-27206022
R19	Resistor, +-5% 560R 1/4W, Carbon Film	1	240-56106022
R20	Resistor, 22R 1/4W +-5%, Carbon film	1	240-22006022
R21	Resistor, 100R +-5% 1/4W, Carbon Film	1	240-10106022
R22	Resistor, 56R +-5% 1/4W, Carbon Film	3	240-56006022
R23	Resistor, 56R +-5% 1/4W, Carbon film		240-56006022
R243	Resistor, 12K +-5% 1/4W, Carbon Film	1	240-12306022
R25	Resistor, +-5% 1/4W 470R, Carbon Film		240-47106022

APPLE III POWER SUPPLY

REF	DESCRIPTION	QTY	PART NUMBER
R26	Resistor, +-2% 2.7K 1/4W, Metal Film	2	247-2701502
R27	Resistor, +-2% 2.7K 1/4W, Metal Film		247-27015022
R28	Resistor, 100K +-5% 1/4W, Carbon Film	2	240-10406022
R29	Resistor, 100K +-2% 1/4W, Carbon Film		240-10406022
R30	Resistor, -5% 56R 1W, Matal Oxide Filmm	1	248-56006052
R31	Resistor, +-5% 220R 1W, Metal Oxide Film	1	248-22106052
R32	Resistor, 1R !w, Metal film	1	247-10086054
T1	Common Mode Choke Assembly	1	852-20200010
T2	Power Transformer assembly	1	852-10200760
T3	Control Transformer Assembly	1	852-10200680
VDRL	Varistor 260VAC	1	256-26100014
Z1	Zener Diode 9.6 to 10.V @ 1mA	1	222-98085002

THE APPLE /// POWER SUPPLY COMPONENT LAYOUT



APPLE II EMULATION RESTRICTIONS

0 NO LANGUAGE CARD

0 NO ROM CARD

0 PADDLES ARE DIFFERENT

0 ENTER WITH SOFTWARE BUT ONLY
RESET WILL EXIT

THE COLOR VIDEO CONNECTOR

Pin	Name	Description
1	SG	Shield Ground.
2	XRGB4	One of four GRB outputs. This (and pins 5, 9, and 10) is a TTL output with instantaneous color information. A linear weighted sum of these four signals will form a true 16-color RGB video signal
3	SYNCH	Composite synchronization signal with negative-going tips.
4	PDI	Not used.
5	XRGB1	See pin 2.
6	GND	Power and signal ground.
7	-5V	-5 volt power supply. A device may draw up to 200 ma through this pin.
8	+12V	+12 volt power supply. A device may draw up to 500 ma through this pin.
9	XRGB2	See pin 2.
10	XRGB8	See pin 2.
11	BWVID	Black and white composite video. This is an NTSC composite video signal with negative-going synch tips, 1 volt peak-to peak into a 75 ohm load. Color information is encoded as a linear grey scale.
12	NTSC	Color composite video. This is an NTSC-compatible video signal with negative-going sych tips, 1 volt peak-to-peak into a 75 ohm load.
13	GND	Power and signal ground.
14	-12V	-12 volt power supply. A device may draw up to 200 ma through this pin.
15	+5V	+5 volt supply. A device may draw up to 1 amp through this pin.

This connector supplies 7 different video signals and 4 power supply voltages. Through this connector you can hook up the Apple to any NTSC color or black and white video monitor. With an additional circuit you can hook up the Apple to a studio-quality RGB color monitor.

All power supply current ratings assume that no peripheral cards are installed in the system. If there are cards in the system, be sure to account for the current drawn by those cards.

THE HIGH-RESOLUTION GRAPHICS (HI-RES) MODE

The Apple][emulation mode high resolution graphics are identical to the Apple][except some combinations of colors on the right edge of the screen will cause the left edge pixels to blink. This is normal though distracting.

THE SPEAKER

The speaker function is identical to the Apple][with the following additional features.

A reference to location 49216 (or the equivalent addresses -16336 or hexadecimal $C040) will cause a 0.1 second 1 KHz tone to be produced which is similar to the sound the AUTOSTART monitor makes when the BELL character is sent to the screen. The advantage to this is 0.1 seconds of cpu time is returned to the user since only 1 microsecond is required to start the BELL sound.

The AUDIO connector at the back of the Apple /// provides the same signal as the speaker. When you insert a miniature phone-tip plug into this jack, the Apple's internal speaker is silenced; if there is an amplifier or other device properly connected to the plug, then that device will receive all audio signals generated by the Apple. The signal is a 0.5 volt peak-to-peak audio signal on its tip and signal ground on its ring.

THE CASSETTE INTERFACE

The cassette interface is completely eliminated on the Apple ///. References to the cassette output port at 49184 (or the equivalent -16352 of hexadecimal $C020) will cause pin 39 of the I/O slots to go low for a microsecond. This is for use by Apple /// native mode peripherals to deselect to $C800 ROM address space.

Reading the cassette input port at 49248 or the equivalents -16288 or hexadecimal $C060 will read joystick switch 0 into bit 7.

Table 10: Input / Output Special Locations

Function	Address:			
	Decimal		Hex	Read/Write
Speaker	49200	-16336	$C030	R/W
Beep	49216	-16320	$C040	R/W
Deselect $C800 for Apple /// periperals (pin 39 in slots)	49184	-16352	$C020	R/W
Joystick switch 0	49248	-16288	$C060	R(bit 7)
Joystick switch 1	49249	-16287	$C061	R(bit 7)
Joystick switch 2	49250	-16286	$C062	R(bit 7)
Joystick switch 3	49251	-16285	$C063	R(bit 7)
$\overline{\text{A/D Select 0}}$	49240	-16296	$C058	R/W
A/D select 0	49241	-16295	$C059	R/W
$\overline{\text{A/D Select 1}}$	49246	-16290	$C05E	R/W
A/D Select 1	49247	-16289	$C05F	R/W
$\overline{\text{A/D Select 2}}$	49242	-16294	$C05A	R/W
A/D Select 2	49243	-16293	$C05B	R/W
A/D Ramp charge	49244	-16292	$C05C	R/W
A/D Start timeout	49245	-16291	$C05D	R/W
$\overline{\text{A/D Timeout}}$	49254	-16282	$C066	R(bit 7)
Clock millisecond counter ($NO)	49264	-16272	$C070	R(bits 7-4)

Table 9: A/D Selection

A/D 2	A/D 1	A/D 0	Input
0	0	0	Ground
0	0	1	Joystick, Port B, X axis
0	1	0	Joystick, Port B, Y axis
0	1	1	Joystick, Port A, X axis
1	0	0	Joystick, Port A, Y axis
1	0	1	Clock Battery
1	1	0	No connection
1	1	1	Reference Voltage

ANALOG INPUTS

The system has two joystick ports with provisions for two A/D inputs each. Joystick Port A reads A/D inputs 0 and 2 while Port B reads inputs 1 and 3 as defined in BASIC and the monitor subroutine PREAD.

To read the A/D inputs, the software must select the desired input and charge the ramp capacitor for at least 500 microseconds. Then the ramp is started and the time measured until the A/D timeout goes low. The discharge time is proportional to the input voltage.

STROBE OUTPUT

The strobe output ($C040) has been replaced by a 0.1 second 1 KHz tone from the speaker.

AUTOSTART ROM / MONITOR ROM

The Apple][emulation only comes with a modified version of the Autostart ROM. This is in write protected RAM which is loaded when the Apple][emulation disk is booted.

THE SYSTEM MONITOR

SAVING A RANGE OF MEMORY ON THE TAPE

Since there is no cassette port on the Apple /// the W (for WRITE) command has no effect. The code in the Emulation mode Autostart Monitor contains an RTS instruction followed by NOP instructions, followed by BRK instructions. This fills the space occupied by the WRITE subroutine (locations $FECD-$FEF4).

READING A RANGE FROM TAPE

Again, since there is no cassette port the R (READ) command has no effect. The READ subroutine contains an RTS followed by NOP instructions, followed by BRK instructions (locations $FEFD-$FF2C).

SOME USEFUL MONITOR SUBROUTINES

$FB1E PREAD READ A JOYSTICK AXIS

PREAD will return a number which represents the position of a joystick axis. You should pass the number of the joystick axis (0 to 3) in the X register. If this number is greater than 3, port A, Y axis is read. PREAD returns a number from $00 to $FF in the Y register. The accumulator is scrambled.

Joystick	Reference #
Port A, X axis	0
Port B, X axis	1
Port A, Y axis	2
Port B, Y axis	3

Page Three Monitor Locations

Address:		Use:
Decimal	Hex	
1008 1009	$3F0 $3F1	Holds the address of the subroutine which handles machine language "BRK" requests (normally $FA59).
1010 1011	$3F2 $3F3	Soft Entry Vector. These two locations contain the address of the reentry point for whatever language is in use. Normally contains $E003.
1012	$3F4	Power-up byte. Normally contains $45.
1013 1014 1015	$3F5 $3F6 $3F7	Holds a "JuMP" instruction to the subroutine which handles Applesoft]["&" commands. Normally $4C $58 $FF.
1016 1017 1018	$3F8 $3F9 $3FA	Holds a "JuMP" instruction to the subroutine which handles "USER" (CONTROL Y) commands.

Built-In I/O Locatons

	$0	$1	$2	$3	$4	$5	$6	$7
$C000	Keyboard Port A Input							
$C008	Keyboard Port B Input							
$C010	Clear Keyboard Strobe							
$C020	Deselect all expansion I/O space (pin 39) for Apple /// cards							
$C030	Speaker Toggle (1us) pulse							
$C040	Speaker Beep (1 KHz for 0.1 second)							
$C050	gr	tx	nomix	mix	pri	sec	lores	hires
$C058	$\overline{\text{A/D 0}}$	A/D 0	$\overline{\text{A/D 2}}$	A/D 2	A/D CHG	A/D ST	$\overline{\text{A/D 1}}$	A/D 1
$C060	SW0	SW 1	SW 2	SW 3	$\overline{\text{IRQ 2}}$	$\overline{\text{IRQ 1}}$	$\overline{\text{A/D TM}}$	MUX1
$C070	Clock millisecond output ($NO)							

$C090-$C09F	Slot 1 Device Select (pin 41) goes low during C1M
$C0A0-$C0AF	Slot 2 Device Select (pin 41) goes low during C1M
$C0B0-$C0BF	Slot 3 Device Select (pin 41) goes low during C1M
$C0C0-$C0CF	Slot 4 Device Select (pin 41) goes low during C1M
$C0E0	$\overline{\text{Disk Stepper Motor Phase A}}$
$C0E1	Disk Stepper Motor Phase A
$C0E2	$\overline{\text{Disk Stepper Motor Phase B}}$
$C0E3	Disk Stepper Motor Phase B
$C0E4	$\overline{\text{Disk Stepper Motor Phase C}}$
$C0E5	Disk Stepper Motor Phase C
$C0E6	$\overline{\text{Disk Stepper Motor Phase D}}$
$C0E7	Disk Stepper Motor Phase D

$C0E8	Disk motor off
$C0E9	Disk motor on
$C0EA	Select Drive 1 (Built-in)
$C0EB	Select Drive 2 (First external)
$C0EC	Q6L
$C0ED	Q6H
$C0EE	Q7L
$C0EF	Q7H
$C0F0	ACIA Receive/Transmit Data register
$C0F1	ACIA Status register
$C0F2	ACIA Command register
$C0F3	ACIA Control register
$C100-$C1FF	Slot 1 I/O Select (Pin 1) goes low during C1M low
$C200-$C2FF	Slot 2 I/O Select (Pin 1) goes low during C1M low
$C300-$C3FF	Slot 3 I/O Select (Pin 1) goes low during C1M low
$C400-$C4FF	Slot 4 I/O Select (Pin 1) goes low during C1M low

PERIPHERAL BOARD I/O

The Apple /// implements only slots 1 through 4. Slot 6 is always a disk interface card and slots 5 and 7 emulate either a SERIAL or COMMUNICATIONS card. Slot 0 scratchpad RAM exists but no provision is made to put a LANGUAGE card or FIRMWARE card into the system. Thus the RAM is limited to 48K with a 12K ROM chosen at Boot time.

PERIPHERAL CARD I/O SPACE

Slot 6 device I/O space $COEO-$COEF contains the hardware for the disk interface. Slot 7 device I/O space $COFO-$COF3 contains the addresses for the onboard ACIA.

PERIPHERAL CARD ROM SPACE

Slot 5 and slot 7 contain code which is functionally equivalent to the COMMUNICATIONS or SERIAL card for the Apple][. They differ in that they use the built-in ACIA. For a more complete explanation see "SERIAL AND COMMUNICATONS CARD EMULATION ".

Slot 6 contains a copy of the Apple][16 sector Boot PROM.

ROM MEMORY

The Applesoft, Integer Basic, and Autostart Monitor "ROMS" are actually write protected RAMs in the Apple ///. When the Emulation mode disk is booted it loads RAM memory with an image of each set of ROMs. Whichever language is selected when the Apple][disk is booted is loaded into the address space ($D000-$FFFF) and write protected.

RAM MEMORY

In Emulation mode there is always 48K of RAM. It is addressed $0000 to $BFFF. There is no provision for a slot 0 Language or Firmware card.

"USER 1" JUMPER

There is no "User 1" jumper in the Apple ///.

THE GAME I/O CONNECTOR

There is no 16 pin Game I/O connector in the Apple ///. However there are two 9 pin "D" - joystick connectors.

THE JOYSTICK PORTS

The Apple /// has to joystick ports (A and B). The A port will NOT operate a silentype printer in Emulation mode. The physical pinout is:

```
5   4   3   2   1
  9   8   7   6
```

PORT A PINOUT

Pin	Name	Description
1	SGND	Shield ground.
2	+5V	+5 volt power supply.
3	GND	Power and Signal Ground.
4	X0	Horizontal analog input, PDL (0) in BASIC.
5	SW1	Joystick switch 1, orange button.
6	+12V	+12 volt power supply.
7	GND	Power and signal Ground.
8	Y0	Vertical analog input, PDL (2) in BASIC.
9	SW3	Joystick switch 3.

PORT B PINOUT

Pin	Nmae	Description
1	SGND	Shield Ground.
2	+5V	+5 volt power supply.
3	GND	Power and Signal ground.
4	X1	Horizontal analog input, PDL (1) in BASIC.
5	SW2	Joystick switch 2, orange button.
6	+12V	+12 volt power supply.
7	GND	Power and signal ground.
8	Y1	Vertical analog input, PDL (3) in BASIC.
9	SW0	Joystick switch zero.

THE KEYBOARD

The keyboard is different in design but the locations of the Keyboard Data Input and the Clear Keyboard Strobe are the same. For more information see "THE KEYBOARD" in chapter 1.

CASSETTE INTERFACE JACKS

There are no cassette interface jacks in the Apple ///.

POWER CONNECTOR

The power connector is different but is not user accessible.

SPEAKER

The speaker is identical to the Apple][.

PERIPHERAL CONNECTORS

The Apple][emulation redefines a few of the pins on the connector and adds several new ones.

The most significant difference is that interrupts will not be sent to the 6502 from the slots. In fact the IRQ (pin 30) is an input to the cpu so the card can't even determine if an interrupt is occuring. Thus Emulation mode runs without interrupts, period.

The RES (pin 31) is an output to the card and goes low when the RESET key is pressed on the keyboard. However the microprocessor is actually performing an NMI not a RESET.

Peripheral Connector Pinout

GND	26	25	+5V
DMAOK	27	24	NOT USED
$\overline{\text{DMAI}}$	28	23	NOT USED
$\overline{\text{IONMI}}$	29	22	$\overline{\text{TSADE}}$ (Open collector)
$\overline{\text{IRQ}}$	30	21	RDY (Open collector)
$\overline{\text{IORES}}$	31	20	$\overline{\text{I/O STROBE}}$
$\overline{\text{INH}}$	32	19	PHO
-12V	33	18	R/$\overline{\text{W}}$
-5V	34	17	A15
SYNC	35	16	A14
C7M	36	15	A13
Q3	37	14	A12
$\overline{\text{C1M}}$	38	13	A11
$\overline{\text{IOCLR}}$	39	12	A10
C1M	40	11	A9
$\overline{\text{DEV SEL}}$	41	10	A8
D7	42	9	A7
D6	43	8	A6
D5	44	7	A5
D4	45	6	A4
D3	46	5	A3
D2	47	4	A2
D1	48	3	A1
D0	49	2	A0
+12V	50	1	$\overline{\text{I/O SELECT}}$

Peripheral Connector Signal Description

Pin:	Name:	Description:
1	$\overline{\text{I/O SELECT}}$	This line, normally high, will become low when the microprocessor references page $Cn, where n is the individual slot number. This signal become active during PHO (nominally 500ns) and will drive 12 LSTTL loads.
2-17	A0-A15	The buffered address bus. The address on these lines becomes valid within 300ns after the beginning of $\overline{\text{C1M}}$ and remains vaild through PHO. These lines will each drive 8 LSTTL loads.
18	$\text{R}/\overline{\text{W}}$	Buffered Read/$\overline{\text{Write}}$ signal. This becomes valid at the same time the address bus does, and goes high during a read cycle and low during a write. This line can drive up to 10 LSTTL loads.
19	PHO	A 1 MHz signal which is identical to C1M. This line will drive 5 LSTTL inputs.
20	$\overline{\text{I/O STROBE}}$	This line will go low during C1M when the address bus contains an address between $C000 and $CFFF. This line will drive 12 LSTTL loads.
21	RDY	The 6502's RDY input. This line should change only during C1M, and when low will halt the microprocessor on the next read cycle. This line has a 1K ohm pullup to +5V. This line should be driven from an open collector output.
22	$\overline{\text{TSADB}}$	A low on this line from the peripheral will cause the address bus to tri-state for Direct Memory Access (DMA) applications. This has a 1 K ohm resistor pullup to +5V. This should be driven from an open collector output.
23		Not used in an Apple ///.
24		Not used in an Apple ///.
25	+5V	Positive 5-volt supply, 2.0 amps total for all peripheral boards together (but note a limit of 1.5 Watts per board).
26	GND	System circuit ground. 0 volt line from power supply. Do not use for shield ground.
27	DMAOK	Acknowledge signal to the peripheral following

		its request for the special Direct Memory Access (DMA) mode. Informs the peripheral that the DMA can now proceed.
28	$\overline{\text{DMAI}}$	Direct Memory Access (DMA) interrupt. Requests the A Apple /// DMA mode. Has a 1 K ohm pullup to +5. This should be driven from an open collector output.
29	$\overline{\text{IONMI}}$	Input/Output Non-Maskable Interrupt. This is equivalent to the IORES (pin 31) line as it will execute the same code in the Autostart ROM. This line should be driven by an open collector output.
30	$\overline{\text{IRQ}}$	This line is ignored in Apple][emulation mode. It should be driven by a TTL output.
31	$\overline{\text{IORES}}$	Input/Output Reset signal used to reset the peripheral devices. Pulled low by a power on or RESET key. This line will drive 12 LSTTL loads.
32	$\overline{\text{INH}}$	Inhibit line. When a device pulls this line low, all system memory is disabled. This line has a 1 K ohm pullup resistor to +5V and should be driven form an open collector output.
33	-12V	Negative 12 volt supply, 200mA total for all peripheral boards together.
34	-5V	Negative 5 volt supply, 200mA total for all periperal boards together.
35	SYNC	The 6502 opcode synchronization signal. Can be used for external bus control signals. Will drive 10 LSTTL loads.
36	C7M	Seven MHz high frequency clock. Will drive 10 LSTTL loads.
37	Q3	A 2MHz (nonsymetrical) general purpose timing signal. Will drive 10 LSTTL inputs.
38	$\overline{\text{C1M}}$	Complement of C1M clock. This will drive 12 LSTTL loads.
39	$\overline{\text{IOCLR}}$	Provides the $C800 space disable function directly without address decoding ($CFFF is used for Apple][peripherals. It is addressed from $C02x. This line will drive 12 LSTTL loads.
40	$\overline{\text{C1M}}$	Phase C1M clock. This is the same as the microprocessor's 1 MHz clock. This will drive 12 LSTTL loads.
41	$\overline{\text{DEVICE SELECT}}$	This line becomes acive (low) on each peripheral

		connector when the address bus is holding address between $C0n0 and $C0nF where n is the slot number plus $8. This line will drive 12 LSTTL loads.
42-49	D7-D0	The 8-bit system data bus. During a write cycle, data is set up by the 6502 less than 300ns after the beginning of $\overline{\text{C1M}}$. During a read cycle the 6502 expects data to be ready no less than 100ns before the end of $\overline{\text{C1M}}$. These lines will drive 8 LSTTL inputs.
50	+12V	Positive 12 volt supply, 300mA total for all peripheral boards together.

ROM LISTINGS

APPLE][EMULATION MODE AUTOSTART ROM LISTING

The following is a listing of addresses which changed content in the Autostart ROM to eliminate cassette I/O, read joysticks, and redirect the NMI vector to the RESET code.

```
;       THE ACIA IS CAPABLE OF GENERATING INTERRUPTS IN EMULATION MODE.
;        IF IT DOES THE INTERRUPT RECEIVER SETS THE PROCESSOR INTERRUPT
;        INHIBIT BIT TO PREVENT THE SERVICING OF THIS INTERRUPT


FA49: 4C 10 FF            JMP IHBIRQS      ;JMP TO CODE TO INHIBIT INTERRUPTS

FF10: 68                  PLA              ;GET PROCESSOR STATUS BYTE
FF11: 09 04               ORA #$04         ;SET INTERRUPT INHIBIT BIT
FF13: 48                  PHA              ;PUT STATUS BYTE BACK ON STACK
FF14: A5 45               LDA $45          ;RESTORE ACCUMULATOR
FF16: 40                  RTI              ;RETURN WITH INTERRUPTS INHIBITTED


;       THE RESET KEY IN EMULATION MODE GENERATES AN NMI (NONMASKABLE
;        INTERRUPT). THEREFORE THE NMI VECTOR IS SET TO POINT AT THE
;        RESET CODE WHICH ALSO MAKES SURE THE DISK MOTOR STOPS


FFFA: 62 FA               DFB     RESET    ;POINT NMI VECTOR TO RESET CODE

FA62: D8         RESET    CLD              ;BINARY ARITHMATIC PLEASE
FA63: AD EE C0            LDA     $C0EE    ;SET DISK READ
FA66: AD EC C0            LDA     $C0EC
FA69: AD E8 C0            LDA     $C0E8    ;TURN OFF DISK
FA6C: 20 84 FE            JSR     SETNORM
FA6F: 20 2F FB            JSR     INIT
FA72: 20 93 FE            JSR     SETVID
FA75: 20 89 FE            JSR     SETKBD
FA78: EA                  NOP
FA79: EA                  NOP
FA7A  EA                  NOP


;       THE CASSETTE READ ROUTINE SIMPLY RETURNS TO USER CALLS
```

```
FEFD: 60          READ    RTS       ;NO CASSETTE PORT - RETURN TO USER

FEFE-FF0A: EA             NOP       ;FILL CODE WITH NOPS
FF0B: 22
FF0C-FF0F: 00             BRK       ;STOP USER FROM JUMPING INTO MIDDLE OF CODE
FF17-FF2C: 00             BRK


;       THE CASSETTE WRITE ROUTINE SIMPLY RETURNS TO USER CALLS


FECD: 60                  RTS       ;NO CASSETTE PORT - RETURN TO USER

FECE-FEF2: EA             NOP       ;FILL CODE WITH NOPS
FEF3-FEF5: 00             BRK       ;STOP USER JUMPING INTO CODE


;       READ JOYSTICK AXIS.  THIS IS THE SAME ENTRY ADDRESS OF PREAD
;        WHICH READS THE GAME PADDLES IN THE APPLE ][
;
;       X REGISTER CONTAINS JOYSTICK AXIS AND Y RETURNS $00-$FF OF JOYSTICK
;
;               X REGISTER      JOYSTICK AXIS
;
;                   0           PORT A, X AXIS
;                   1           PORT B, X AXIS
;                   2           PORT A, Y AXIS
;                   3           PORT B, Y AXIS


FB1E: 8A          PREAD   TXA                 ;SAVE X REGISTER
FB1F: 48                  PHA
FB20: 49 01               EOR #$01            ;REMAP JOYSTICK ADDRESS
FB22: AA                  TAX
FB23: AD 59 C0            LDA $C059           ;SET ANALOG MUX TO PORT B, X AXIS
FB26: AD 5E C0            LDA $C05E
FB29: AD 5A C0            LDA $C05A
FB2C: 4C C9 FC            JMP JOY2

FCC9: E8          JOY2    INX
FCCA: CA                  DEX                 ;SET FLAGS
FCCB: F0 12               BEQ JOY3            ;PORT B, X AXIS?
FCCD: AD 5F C0            LDA $C05F           ;NO
FCD0: CA                  DEX
FCD1: F0 0C               BEQ JOY3            ;PORT A, X AXIS?
FCD3: AD 58 C0            LDA $C058           ;NO
FCD6: CA                  DEX
FCD7: F0 06               BEQ JOY3            ;PORT B, Y AXIS?
FCD9: AD 5E C0            LDA $C05E           ;NO
```

```
FCDC: AD 5B C0          LDA $C05B       ;MUST BE PORT A, Y AXIS
FCDF: AD 5C C0   JOY3   LDA $C05C       ;CHARGE CAPACITOR
FCE2: A9 0F             LDA #$0F        ;WAIT 800US
FCE4: 20 A8 FC          JSR WAIT
FCE7: A0 80             LDY #$80
FCE9: AD 5D C0          LDA $C05D       ;START TIMEOUT
FCEC: A2 48             LDX #$48        ;WAIT 370US
FCEE: CA         JOY4   DEX
FCEF: 10 FD             BPL JOY4
FCF1: E8         JOY5   INX
FCF2: B9 E6 BF          LDA $BFE6,Y     ;FALSE READ
FCF5: 2A                ROL
FCF6: AD 66 C0          LDA $C066       ;BIT 7 IS VOLTAGE CROSSOVER
FCF9: 30 F6             BMI JOY5        ;HAS VOLTAGE CROSSED OVER?
FCFB: 8A                TXA             ;YES
FCFC: 10 04             BPL JOY6        ;WAS COUNT POSITIVE?
FCFE: A9 FF             LDA #$FF        ;NO
FD00: D0 01             BNE JOY7        ;USE $FF
FD02: 2A         JOY6   ROL             ;DOUBLE COUNT
FD03: A8                TAY             ;RETURN COUNT IN Y
FD04: 68                PLA             ;RESTORE X
FD05: AA                TAX
FD06: 60                RTS

FD07-FD0B: 00           BRK             ;FILL SPACE
```

REV	ZONE	ECO #	REVISION	APPD
C2			ENG. RELEASE	
C3			PRE-PRODUCTION RELEASE	
E			PRE-PRODUCTION CHANGES	
E		504	ECO RELEASE	
F		544	DELETED CAP ARRAY (CP1), AND N13, M13, K13, N3, N10 WAS RC NETWORK, C5 WAS 47pF, Q1 WAS QØ N.C. IS NOW IOSTOPD. J20, 7 WAS COLORKILL, J20, 9 WAS FORCPAGE. DELETED MICROPROCESSER (33).	
G		778	H3 WAS LS04; R15 WAS 47 OHM, R16 WAS 75 OHM. ADDED 1K OHM RESISTOR AT K10.	

NOTE: UNLESS OTHERWISE SPECIFIED

1. ⬭ = 75Ω

2. (UUT) = ALL UNITS UNDER TEST MOLEX PINS TO BE LOCATED TOGETHER.

3. ○ = ALL TIMING MOLEX PINS TO BE LOCATED TOGETHER.

4. THIS SCHEMATIC REPRESENTS ASSY 610-0105 AT REV LEVEL: F.

⚠5 FOR STANDARD SYSTEMS G9 IS 341-0030, FOR EURO SYSTEMS G9 IS 341-0060.

⚠6 FOR STANDARD SYSTEMS Y1 IS 14.318630 MHZ, FOR EURO SYSTEMS Y1 IS 14.250450 MHZ.

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5 B4

Page 5 of 10

ALPHA NUMERIC LOCATION

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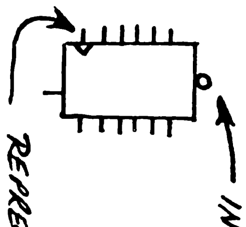

INVERSION PERFORMED INSIDE IC

REPRESENTS CLOCK INPUT

THIRD ANGLE PROJECTION
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ANGLES	±
FRACTIONS	±
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MATERIAL	N/A
NEXT ASSY	FINISH N/A

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TITLE SCHEMATIC APPLE /// MAIN LOGIC #2

SIZE C | DRAWING NUMBER 050-0039-G

SCALE NONE | SHEET 1 OF 10

DRAWING NUMBER 050-0039-G | SH 1 OF 10

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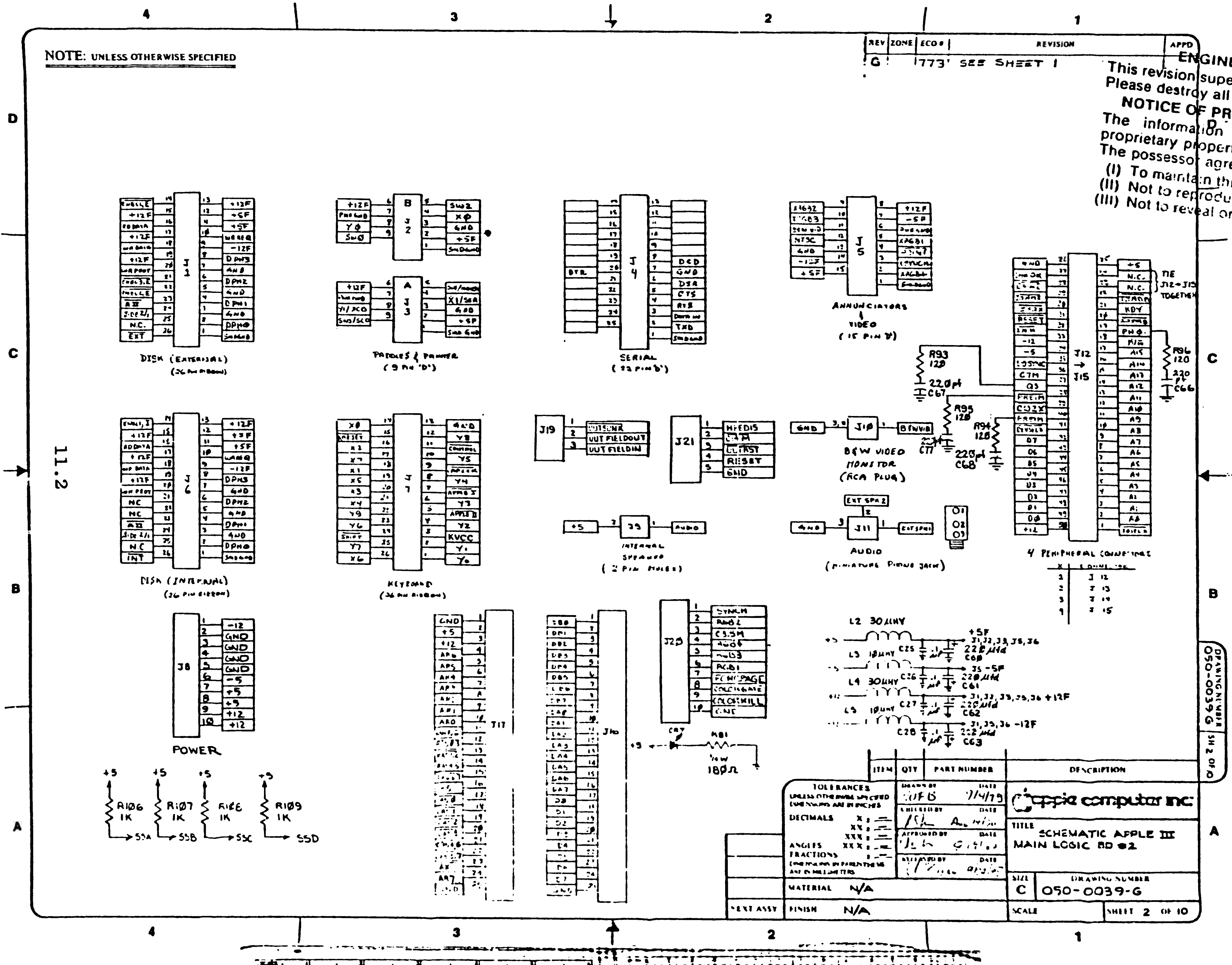
G		773	SEE SHEET 1	



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ANGLES XXX ±
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TITLE SCHEMATIC APPLE III MAIN LOGIC BD #2

MATERIAL N/A
FINISH N/A
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SIZE C
DRAWING NUMBER 050-0039-G
SCALE
SHEET 2 OF 10

DRAWING NUMBER 050-0039 G SH 2 OF 10

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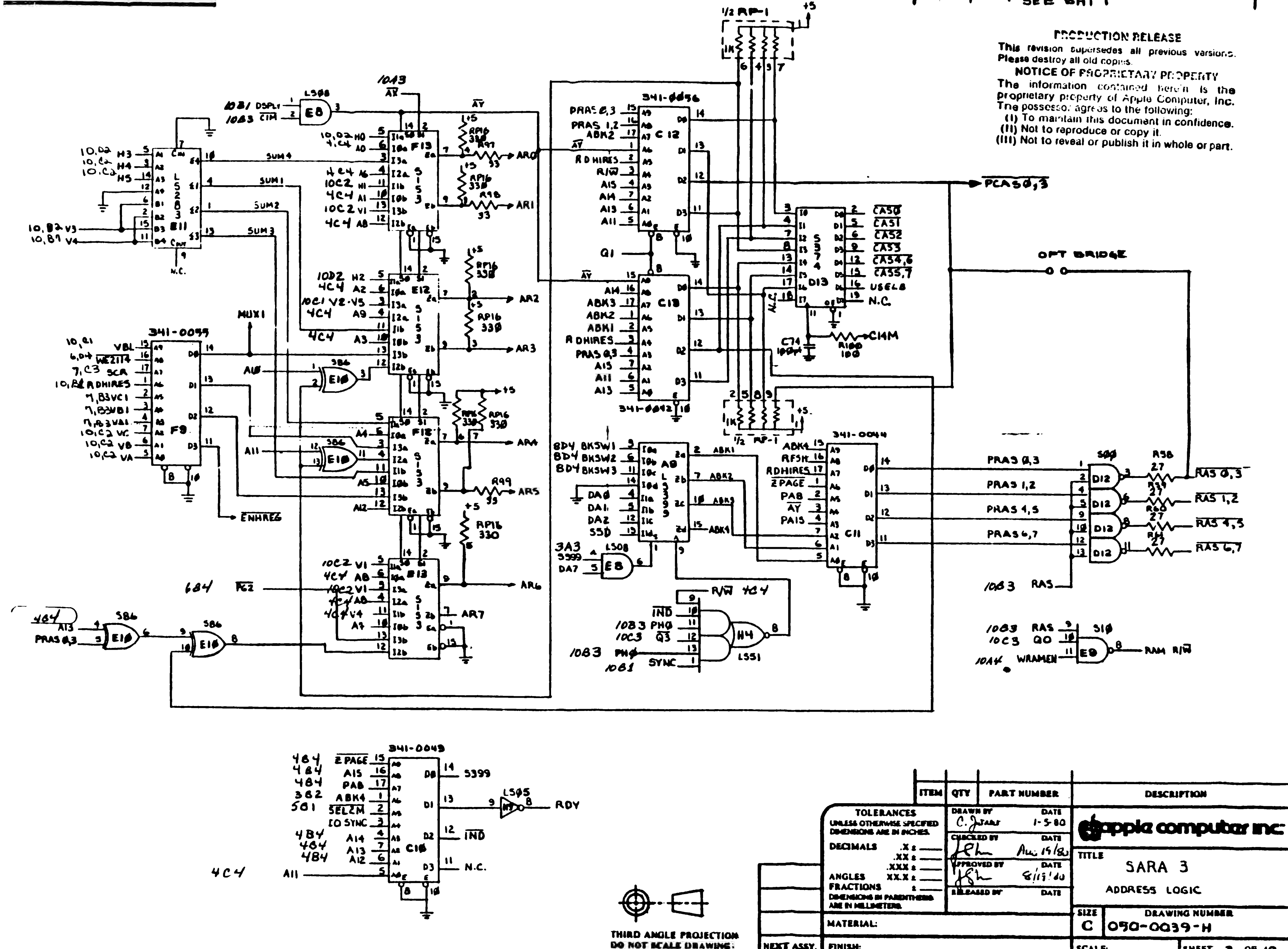

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± .XX ± .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.

		DATE
DRAWN BY	C. Jtaas	1-5-80
CHECKED BY		Aug 15/80
APPROVED BY		8/13/80
RELEASED BY		

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TITLE
SARA 3
ADDRESS LOGIC

MATERIAL:

FINISH:

NEXT ASSY.

SIZE C
DRAWING NUMBER 050-0039-H

SCALE:
SHEET 3 OF 10

THIRD ANGLE PROJECTION
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SH 3 OF 10

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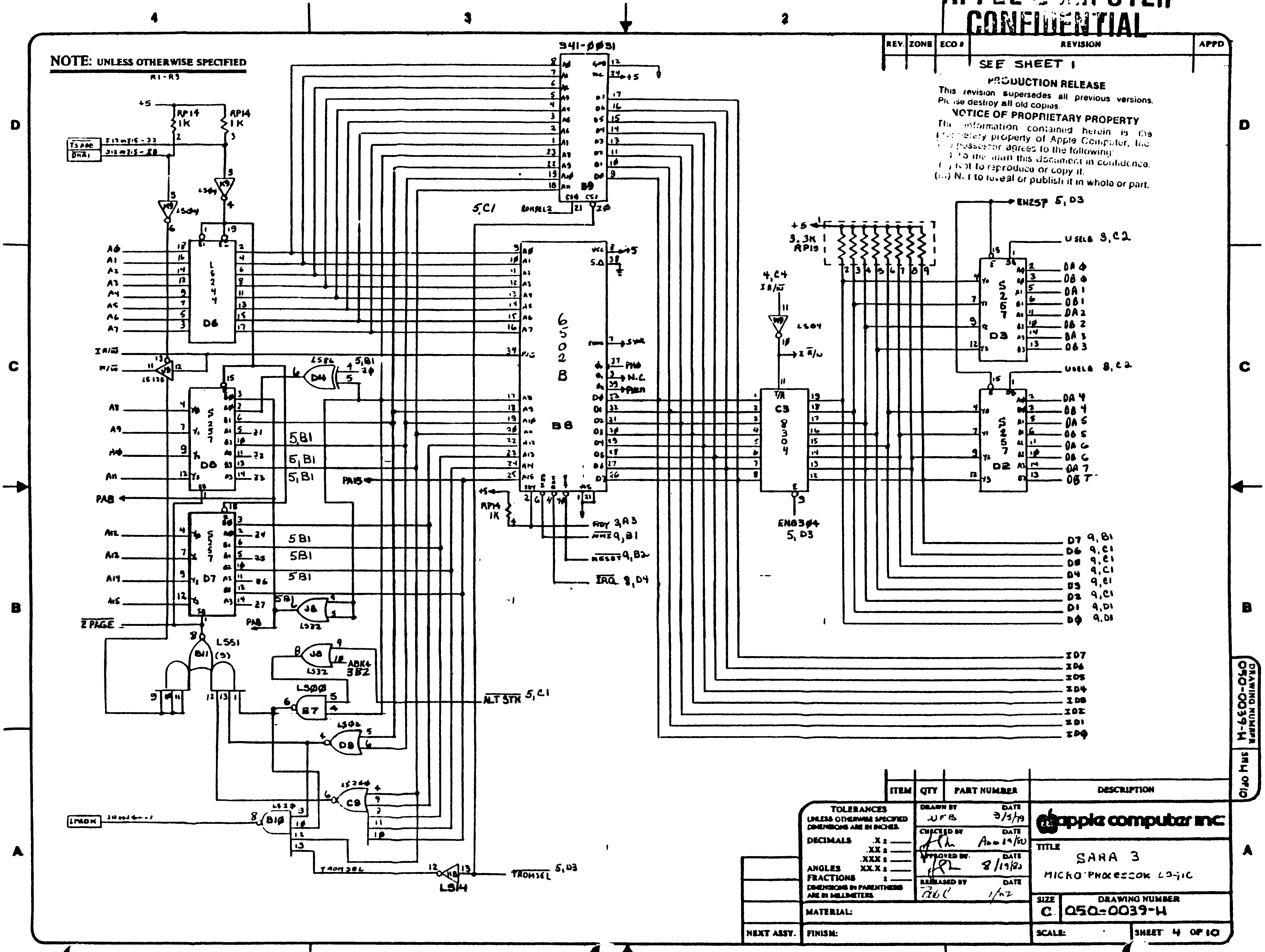

REV.	ZONE	ECO #	REVISION	APPD
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TOLERANCES
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DECIMALS .X ± ___
.XX ± ___
.XXX ± ___
ANGLES XX.X ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

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CHECKED BY DATE Aug 19/80
APPROVED BY DATE 8/19/80
RELEASED BY DATE 1/82

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TITLE SARA 3
MICRO PROCESSOR LOGIC

SIZE C
DRAWING NUMBER 050-0039-H

MATERIAL:

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FINISH:

SCALE:

SHEET 4 OF 10

DRAWING NUMBER 050-0039-H SH4 OF10

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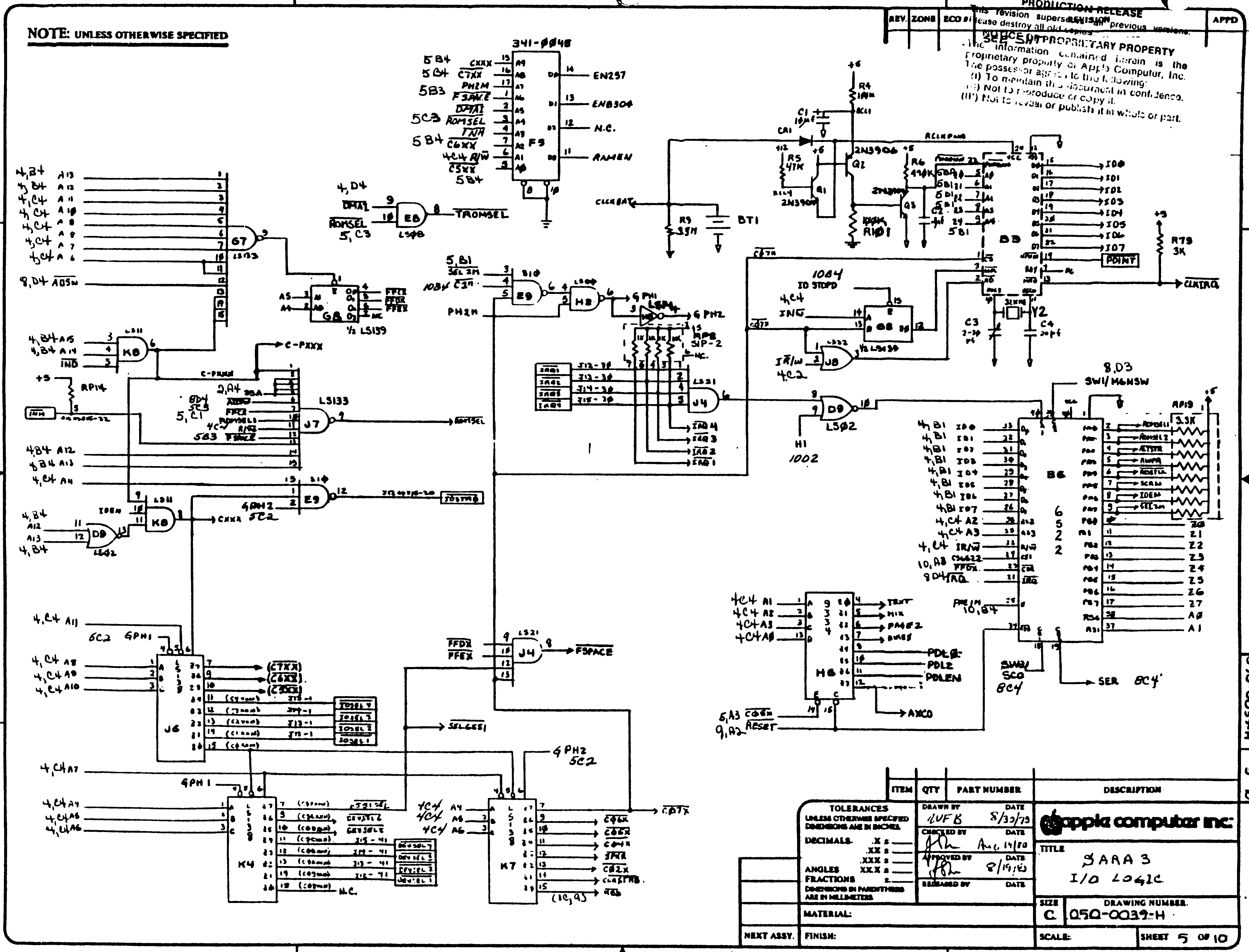

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DECIMALS	.X ± .XX ± .XXX ±	CHECKED BY	DATE Aug 14/80
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FRACTIONS	±	RELEASED BY	DATE
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ITEM	QTY	PART NUMBER	DESCRIPTION

MATERIAL:

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NEXT ASSY.

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TITLE SARA 3 I/O LOGIC

SIZE C

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SCALE:

SHEET 5 OF 10

DRAWING NUMBER 050-0039-H SH 5 OF 10

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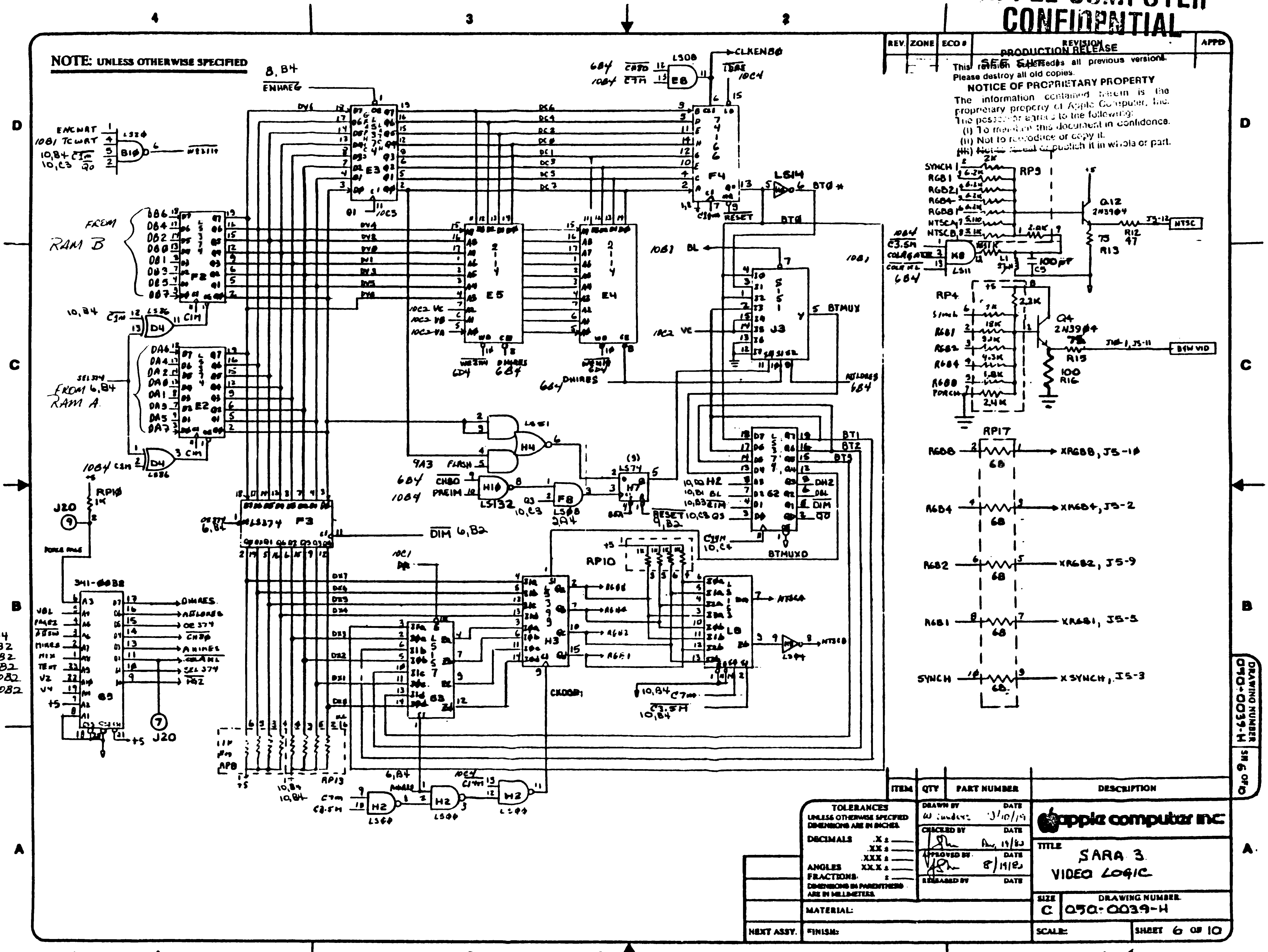

REV. | ZONE | ECO # | REVISION | APPD

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SEE SHEET 1

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ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS .X ± .XX ± .XXX ±
ANGLES .XXX ±
FRACTIONS ±
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.

MATERIAL:

NEXT ASSY. | FINISH:

DRAWN BY W. Sanders DATE 3/10/79
CHECKED BY DATE Au. 19/82
APPROVED BY DATE 8/19/82
RELEASED BY DATE

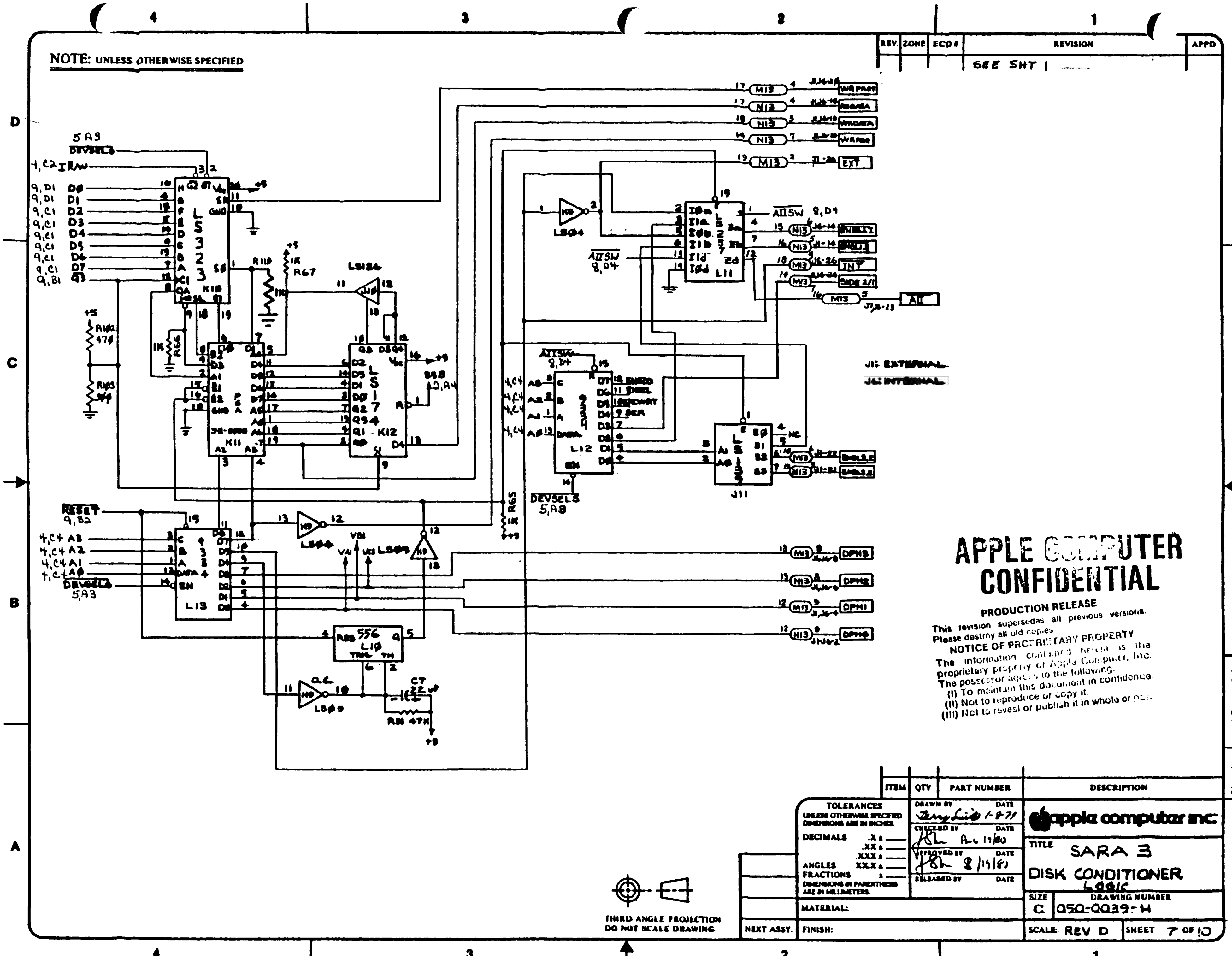
apple computer inc

TITLE SARA 3 VIDEO LOGIC

SIZE C DRAWING NUMBER 050-0039-H

SCALE: SHEET 6 OF 10

DRAWING NUMBER 050-0039-H SH 6 OF 10



REV.	ZONE	ECO #	REVISION	APPD
			SEE SHT 1	

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DECIMALS .X ± .XX ± .XXX ±
ANGLES .XXX ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY Terry Smith DATE 1-8-71
CHECKED BY JSh DATE Aug 19 80
APPROVED BY JSh DATE 8/14/81
RELEASED BY DATE

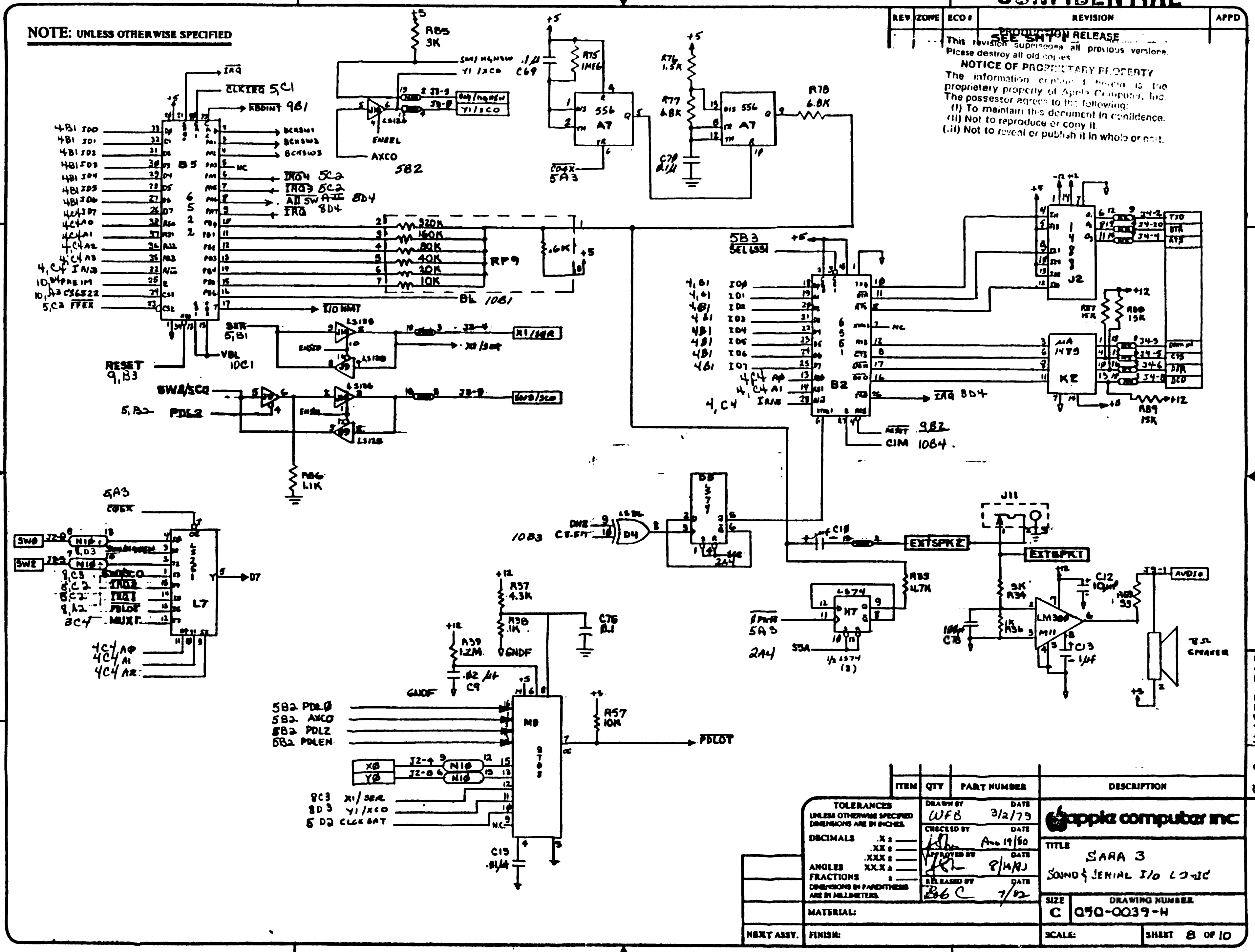
MATERIAL:
NEXT ASSY. FINISH:

apple computer inc
TITLE SARA 3
DISK CONDITIONER
Logic

SIZE C
DRAWING NUMBER 050-0039-H
SCALE REV D
SHEET 7 OF 10

DRAWING NUMBER 050-0039-H SH 7 OF 10

APPLE COMPUTER
CONFIDENTIAL



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TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ___ .XX ± ___ .XXX ± ___
ANGLES XX.X ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.

DRAWN BY WFB DATE 3/2/79
CHECKED BY DATE Aug 19/80
APPROVED BY DATE 8/14/82
RELEASED BY Bob C DATE 7/82

apple computer inc

TITLE SARA 3
SOUND & SERIAL I/O LOGIC

SIZE C
DRAWING NUMBER 050-0039-H

MATERIAL:
NEXT ASSY.
FINISH:
SCALE:
SHEET 8 OF 10

APPLE [illegible] CONFIDEN[illegible]L

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD
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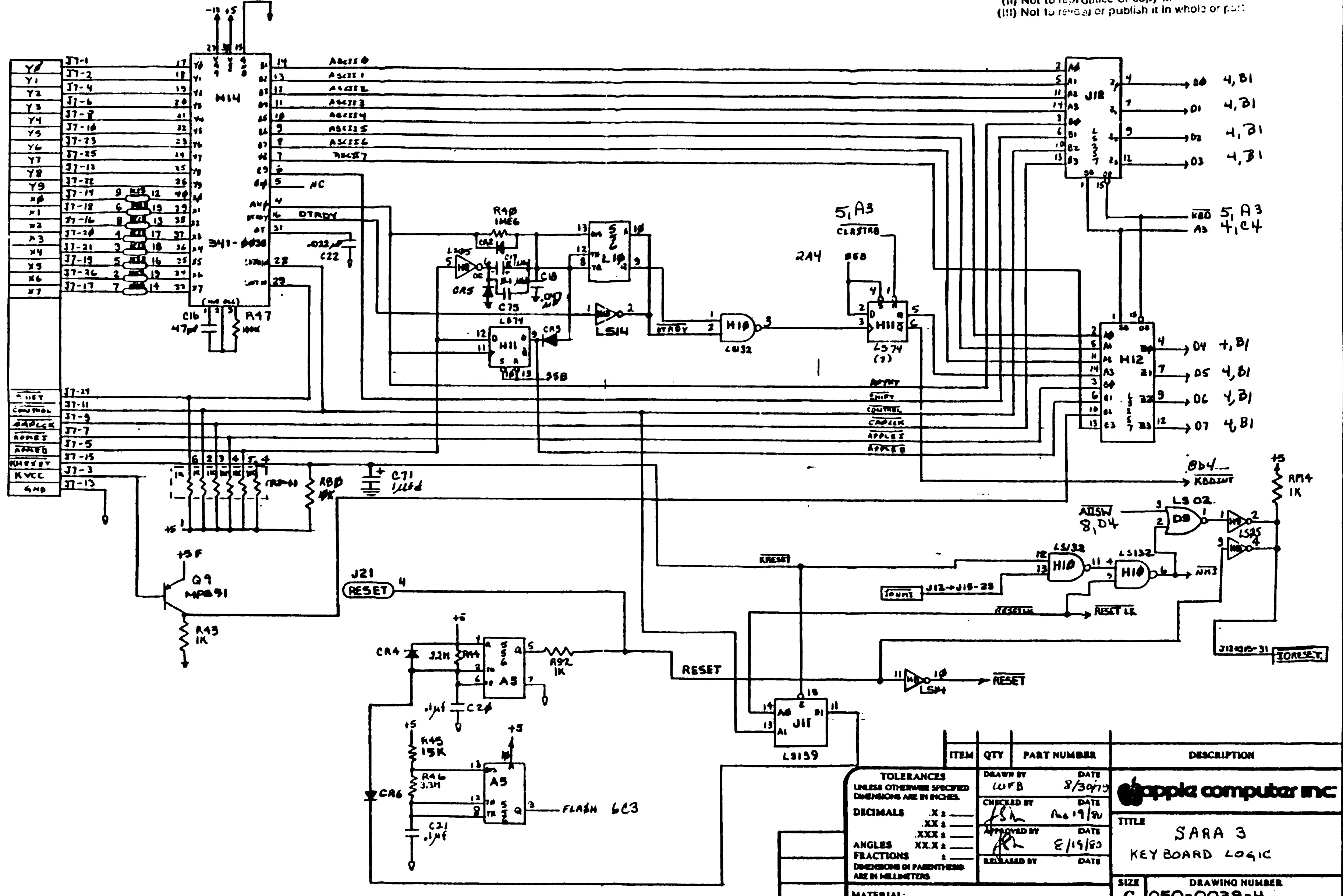


ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY WFB	DATE 8/30/79
CHECKED BY	DATE Aug 19/80
APPROVED BY	DATE 8/19/80
RELEASED BY	DATE

MATERIAL:

NEXT ASSY.

FINISH:

apple computer inc

TITLE SARA 3
KEY BOARD LOGIC

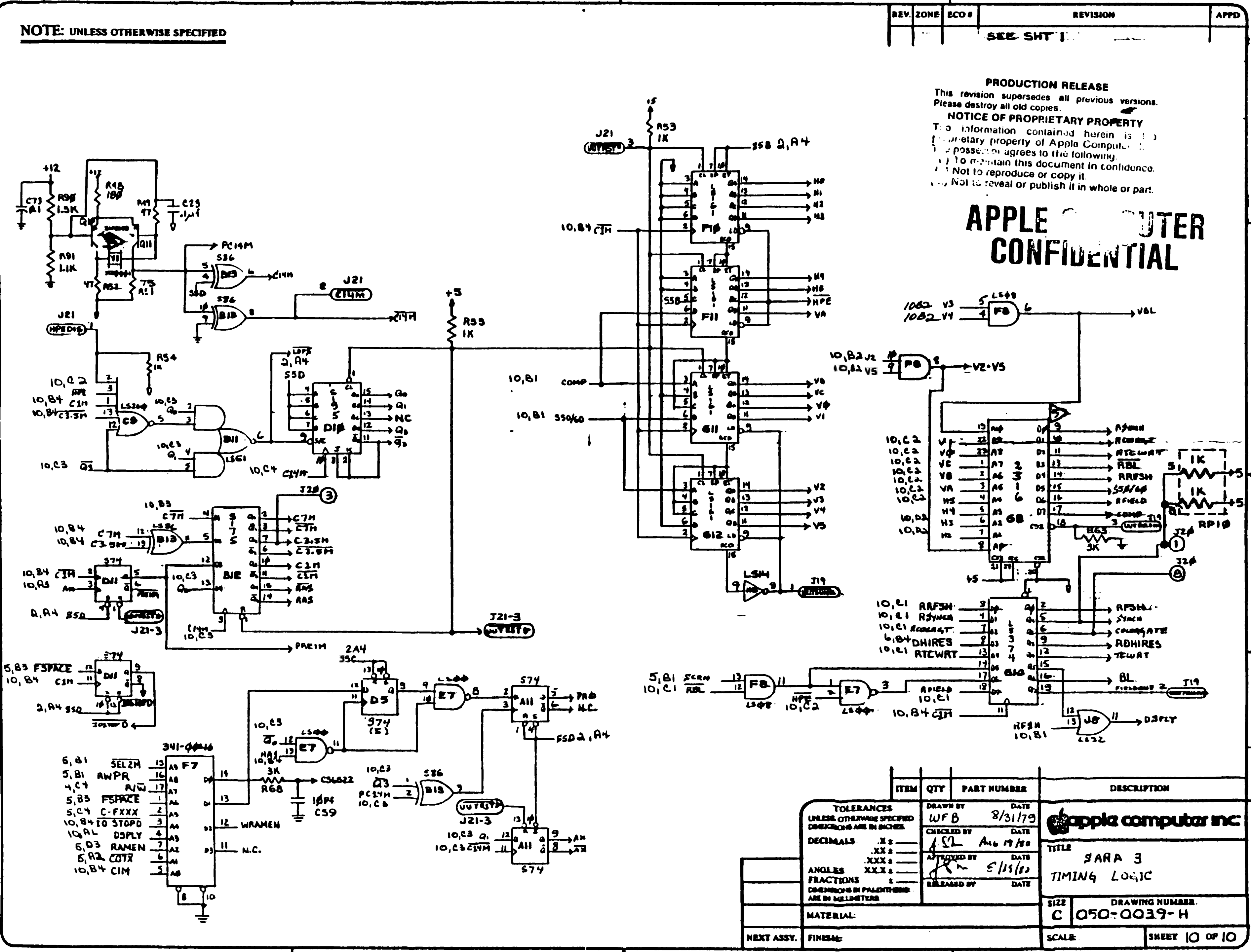
SIZE C
DRAWING NUMBER 050-0039-H

SCALE:

SHEET 9 OF 10

DRAWING NUMBER 050-0039-H SH 9 OF 10

NOTE: UNLESS OTHERWISE SPECIFIED



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REV.	ZONE	ECO #	REVISION	APPD
			SEE SHT 1	

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS .X ± .XX ± .XXX ±
ANGLES .XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS

DRAWN BY WFB DATE 8/31/79
CHECKED BY LSL DATE Aug 19/80
APPROVED BY DATE 8/15/80
RELEASED BY DATE

apple computer inc

TITLE SARA 3 TIMING LOGIC

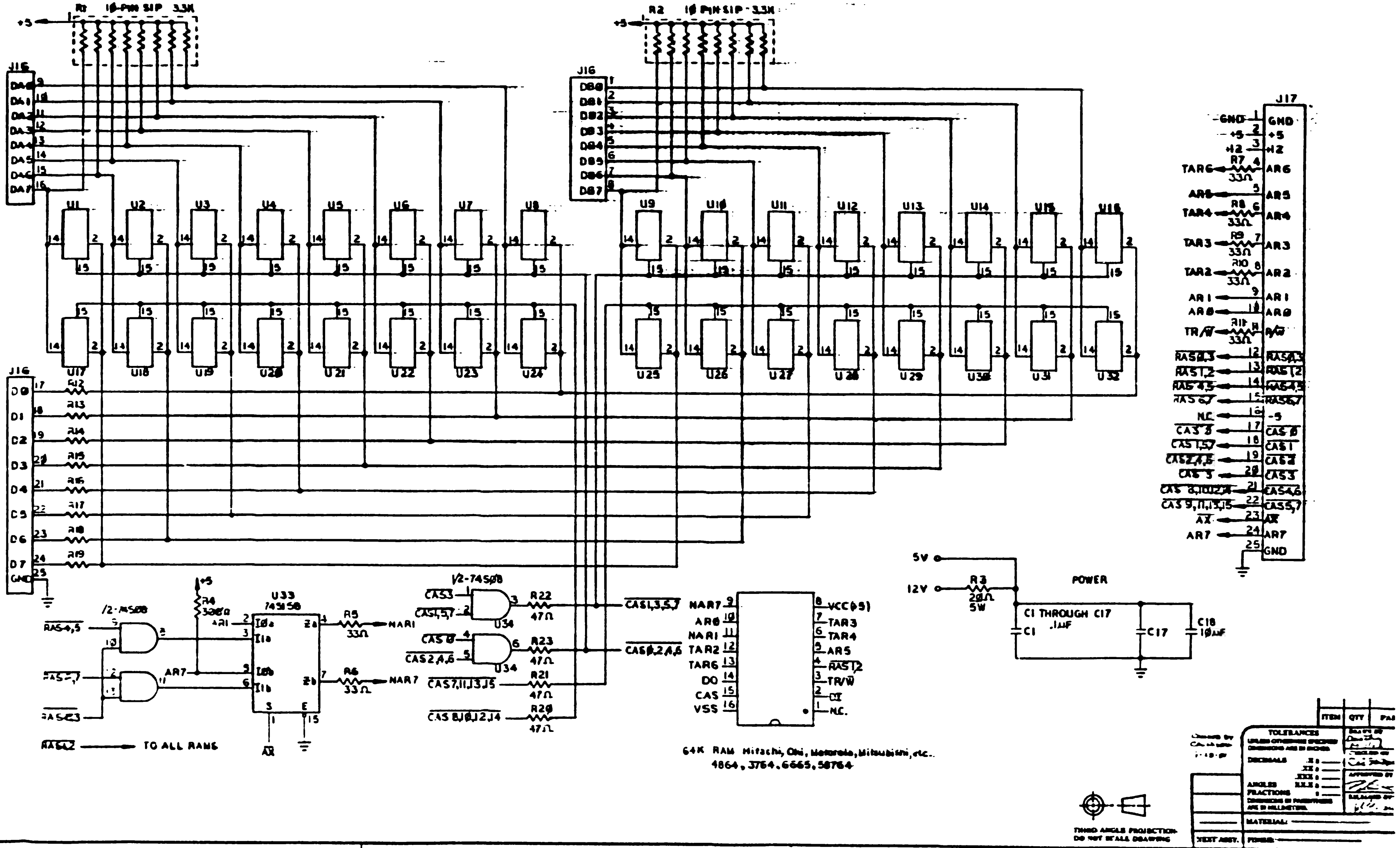
MATERIAL:
FINISH:
NEXT ASSY.

SIZE C DRAWING NUMBER 050-0039-H
SCALE SHEET 10 OF 10

DRAWING NUMBER 050-0039-H SH 10 OF 10

NOTE: UNLESS OTHERWISE SPECIFIED
1. R12 THRU R19 ARE 100Ω.

APPLE /// 5V MEMORY BOARD



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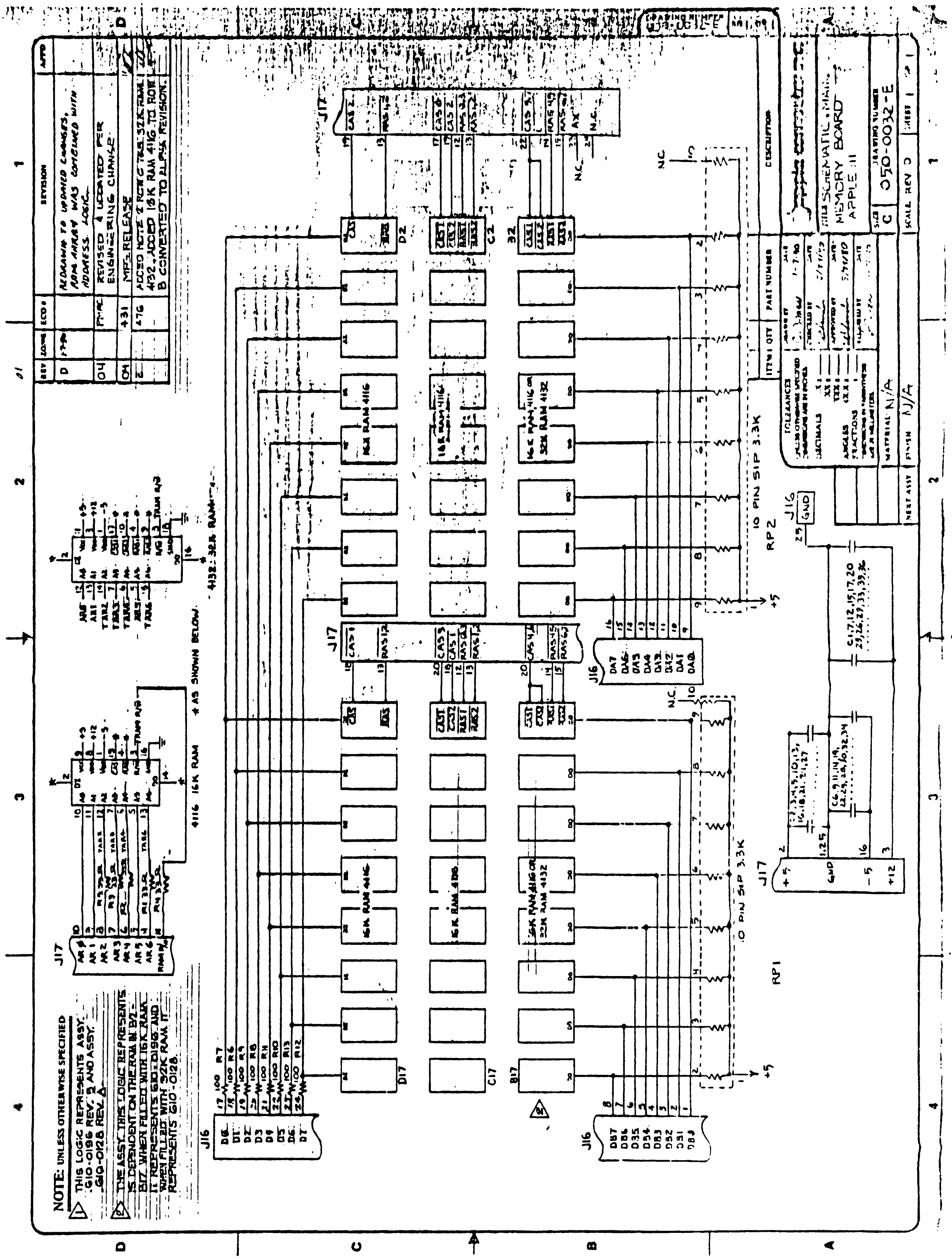


REDRAWN TO UPDATED CHANGES, ROM ARRAY WAS COMBINED WITH ADDRESS LOGIC.
REVISED & UPDATED PER ENGINEERING CHANGE
MFG RELEASE
ADDED NOTE 2 ROW C THRU 32K RAM 4132. ADDED 16K RAM 4116 TO ROW B CONVERTED TO ALPHA REVISION
NOTE: UNLESS OTHERWISE SPECIFIED
1. THIS LOGIC REPRESENTS ASSY. 610-0196 REV. 2 AND ASSY. 610-0128 REV. A
2. THE ASSY. THIS LOGIC REPRESENTS IS DEPENDENT ON THE RAM IN B2-B17. WHEN FILLED WITH 16K RAM IT REPRESENTS 610-0196 AND WHEN FILLED WITH 32K RAM IT REPRESENTS 610-0128.
J17
J16
16K RAM 4116
16K RAM 4116 OR 32K RAM 4132
4116 16K RAM
4132 32K RAM
* AS SHOWN BELOW
10 PIN SIP 3.3K
RP1
RP2
D2
C2
B2
D17
C17
B17
+5
+12
-5
GND
N.C.
MEMORY BOARD APPLE II
050-0032-E

THE DISK /// SUBSYSTEM

I THEORY OF OPERATION

The Disk /// subsystem, is a self contained Apple /// peripheral which allows user programs and data to be stored and retrieved on 5 1/4" floppy diskettes. The Apple /// supplies DC power, control signals, and a parallel data path to the Disk /// via the A///s main logic board Disk Conditioner (Controller) Circuit. The Disk Conditioner sends DC power, control signals, and serial data to the Analog Card via a 26-conductor ribbon cable.

The Analog Card contains disk read-write electronics, drivers for positioning Stepper Motor, and a transistor power switch. Analog Card also contains circuitry which causes its output signals to the disk conditioner circuit to be active only when the card is enabled. This allows up to 4 Analog Cards to share the same data path for a 4 drive system (one internal, three external drives).

Within the drive itself, movement of Stepper Motor rotates Actuator Cam. Head and Carriage Assembly's Cam Follower, rides in Actuator Cam's spiral groove. Two Guide Rods allow motion of Head and Carriage Assembly either towards, or away from Drive Door. This positions Read/Write Head to appropriate track, so that serial data may then be transferred to and from disk using high-level commands.

A - DISK CONDITIONER CIRCUIT

There are seven sections in the Disk Conditioner circuit:
(Refer to Schematic of Disk Conditioner Logic)

1. Power-On Reset

   This circuit consists of one half of 556 Timer and one open-collector inverter. When power is applied, the outputs of the 9334/LS259 Address Latch (DPh0-3) are brought low which places the Disk Conditioning logic in the read mode, the Q output of the 556 timer (pin 5) goes high for about 65 ms, bringing inverter's output to ground. This resets the State Machine (Prom P6A), and the Drive Enable Multiplexers. The drive enable multiplexer's Z output is prevented from enabling the internal and external drives.

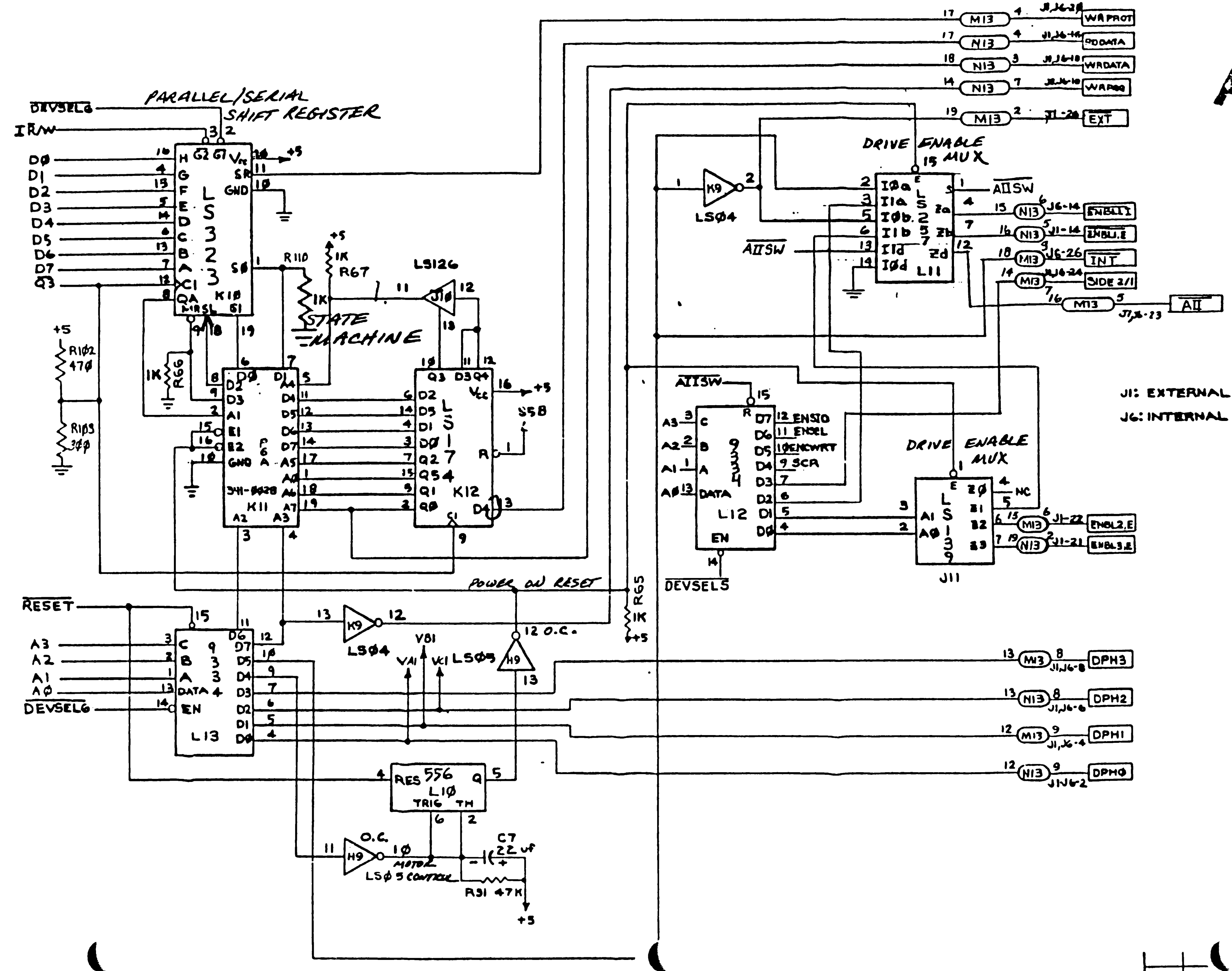
2. The BOOT ROM

   The Boot ROM, though not a part of the disk conditioning circuit, contains the routine which down loads the operating system (SOS) from disk and then jumps into it. The LS323, an 8 Bit Parallel/Serial Register, is enabled (DEVSEL6*) whenever the address C0Exxn is presented. the data, from the boot rom, is converted to serial at the output of pin 1 in the 74LS323 in a write operation.

3. Addressable Latch (9334 or 74LS259).

REV.	ZONE	ECO #	
G		778	SEE SHT I

NOTE: UNLESS OTHERWISE SPECIFIED



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Please de
NOTICE
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proprietary
The posses
(I) To mai
(II) Not to
(III) Not to

ITEM	QTY	ART NUMBER

This chip provides an eight software-controlled output. When DEVSEL6* (pin 9 of LS138 I/O Address Decoder) signal goes low (one of 16 addresses starting at [C0Exxn†, value of Address Line A0 becomes the new value of D output pointed to by Address Lines A1-A3. Latch output D6 and D7 set operating mode of controller (read, write, etc). Q5 selects the internal drive. D4 controls MOTOR ON signal and D0 to D3, set position of the Stepper Motor. Drive enable signals ENBL1I and ENBL1E are true when MOTOR ON signal is true and appropriate drive is selected.

4. State Machine (PROM P6A and 74LS174)

These two parts contain nucleus of Disk Conditioning Logic. A State Machine is a device capable of storing a value in a register. That value, in conjunction with external input, determines what the next register value should be and what output should be generated. Value in register is, machines's Current State and next value is machine's Next State. State machine updates at each clocking, going from state to state and producing output base on state its in and value of its input just before clocking.

Current State, is value at Q2, Q5, Q1, and Q0 from 74LS174. Next state is value of D4-D7 from P6A PROM. Input to State Machine includes D6 and D7 from 9334, QA* output from 74LS174 Shift Register and A2-11. Output from State Machine is PROM signals D0-D3, which effect Shift Register. Q0 from 74LS174, which is high-order bit of Current State, forms WR DATA output. Since State Machine is clocked by two Megahertz Q3* signal, the state lasts for 500 ns.

Flux transitions on diskette are detected by Analog Card and are sent to Disk Conditioning Circuitry as RD DATA. These one microsecond positive going pulses appear at D4 input to 74LS174. NAND Gate and Inverter, which connect to 74LS174's Q3 and Q4 output, cause A4 input to P6A PROM to go low for one state following the falling edge of RD DATA. This information is ignored when writing out to disk. When reading from disk, however, this input forms the basis for determining whether a logic one or zero has been read. A logic one is indicated by a four microsecond period. A logic zero, by an eight microsecond period between flux transitions.

5. Shift Register

74LS323 Universal 8 Bit Parallel/Serial Shift Register, transfers data to and from the Apple ///. When writing to disk, Shift Register under control of State Machine, parallel loads a data byte from the A/// and shifts it left. This causes QA* output to effect State Machine's A1 input. State Machine goes through a different state sequence for a logic one and a logic zero, which causes WR DATA to change value every four and eight microseconds, respectively.

When reading from disk, State Machine shifts appropriate logic levels into Shift Register's SL input. Resulting byte can be read by the A///.

Status of Write Protect switch in Disk Drive, comes into SR input of

Shift Register from Analog Card. Under control of State Machine, Shift Register is placed into a shift right mode, allowing status of switch to be read by software.

6. MOTOR ON Circuit.

Q output from one half of 556 timer, forms MOTOR ON signal. MOTOR ON becomes true when B2-6 is brought to ground under software control. An enable is sent to one of the drives, and Drive Motor in selected drive turns on. When software causes B2-6 to become high-impedance in order to turn off drive, C7 and R31 give drive a 2/3 second grace period before MOTOR ON times out. This prevents drive from being turned on and off when repeated accesses are made.

7. AII EMULATION MODE

With the AIISW* true and DEVSEL5* (addressed by C0Dxxn) selected, the internal and external drives are fooled into operating as an Apple II Disk Drive.

B - ANALOG CARD (Refer to Analog Card Schematic Diagram)

1. Enable Circuit

A Disk Drive connected to the Apple /// is always in one of three operating modes:

a - Read Mode

Flux transitions on diskette are detected by MC3470P Floppy Disk Read Amplifier on Analog Card and are sent to the Disk Conditioner as one microsecond positive-going pulses across RD DATA* line.

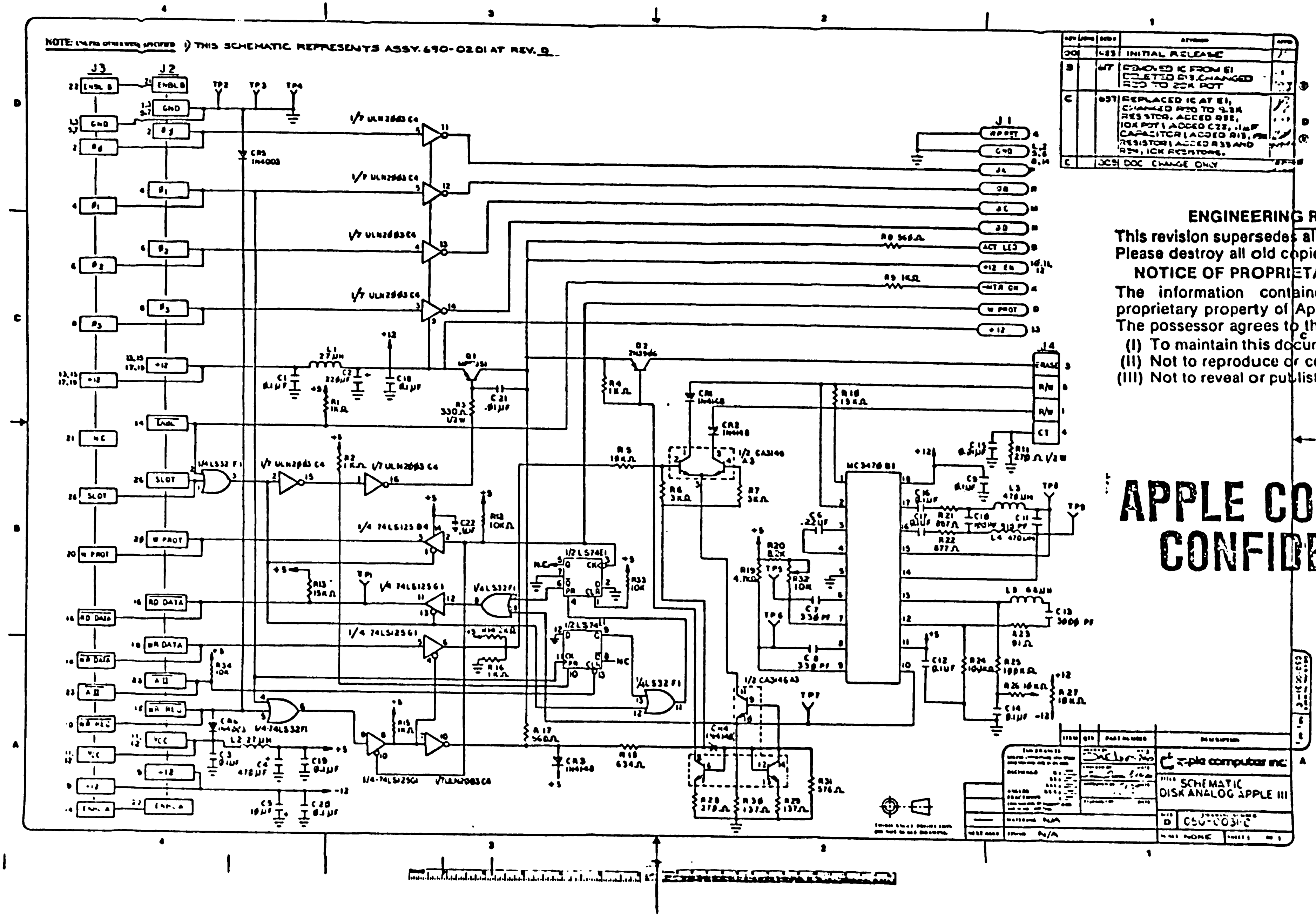
b. Write Mode

Here WR DATA input to Analog Card determines polarity of write current passing through head.

c. Deselected Mode

In this state, drive is not currently performing any data transfers with the Apple ///.

A drived becomes enabled, when ENBL1I input to the Analog Card on the selected drive goes low. This causes Q1 to turn on because current flows through R3 into pin 16 of ULN2003's Darlington output. +12 volts is then supplied to Stepper Motor. Q1 also provides a power source for Write and Erase Current circuits. In addition, ENBL1I signal also enable RD DATA* and W PROT tristate buffers and supplies a MTR ON control signal to Motor Control Board through resistor R9.


NOTE: UNLESS OTHERWISE SPECIFIED 1) THIS SCHEMATIC REPRESENTS ASSY. 690-0201 AT REV. C
J3
J2
J1
J4
ENBL B
GND
Ø0
Ø1
Ø2
Ø3
+12
NC
ENBL
SLOT
W PROT
RD DATA
WR DATA
A II
WR REQ
VCC
-12
ENBL A
TP2
TP3
TP4
CR5 1N4003
1/7 ULN2003 C4
1/4 74LS125 B4
1/4 74LS125 G1
1/4 LS32 F1
1/4 74LS32 F1
1/2 LS74 E1
1/2 CA3146 A3
MC3470 B1
Q1
Q2 2N3906
L1 27µH
L2 27µH
L3 470µH
L4 470µH
L5 68µH
R8 560Ω
R9 1KΩ
ACT LED
+12 EN
WTR CH
W PROT
ERASE
R/W
CT
TP1
TP5
TP6
TP7
TP8
TP9
REV	ECO	DESCRIPTION
00	483	INITIAL RELEASE
B	617	REMOVED IC FROM E1 DELETED R13, CHANGED R20 TO 20K POT
C	637	REPLACED IC AT E1, CHANGED R20 TO 8.2K RESISTOR, ADDED R32, 10K POT, ADDED C22, .1µF CAPACITOR, ADDED R13, 15K RESISTOR, ADDED R33 AND R34, 10K RESISTORS.
C	3C9	DOC CHANGE ONLY
apple computer inc.
TITLE SCHEMATIC DISK ANALOG APPLE III
D
050-0031-C
SCALE NONE
SHEET 1 OF 1
N/A
N/A

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d. Read Electronics

MC3470P Floppy Disk Read Amplifier and associated discrete components, provide a one-chip interface between magnetic head of Disk Drive and RD DATA* input to Disk Conditioning circuit of the main logic board. MC3470P contains both analog and digital circuits which cause a TTL compatible pulse to be generated for each positive and negative peak of input signal.

Input voltage from head appears across pins 1 and 2 of MC3470P. This signal passes through an amplifier and is differentially applied to a noise filter made up of R21 and R22, C10 and C11 and L3 and L4. Filter's output feeds back into MC3470P, where a differentiator circuit provides an output proportional to rate of change, with time, of input signal. In addition, a 90 degree phase lead is introduced which causes a zero crossing at differentiator's output to correspond with a peak at its input. L5, C13 and R23 determine characteristics of differentiator. R27 allows for correction of current imbalances within differentiator so that a sinusoidal input waveform produces evenly spaced RD DATA* pulses.

Zero crossings at output of differentiator cause output of a comparator within MC3470P, in conjunction with digital circuits, create a Time Domain Filter which checks against false zero crossing readings due to distored input waveforms or noise. When a zero crossing is detected, mono #1, formed by R20, R32, and C7, is triggered. At end of its two microsecond period, output of comparitor is again checked. If it has not changed (valid zero - crossing), mono #2 gets a trigger pulse that uses R19 and C8 to generate one microsecond RD DATA* pulse at pin 10 of MC34709P.

3. Write Electronics

During Read Mode (WR REQ* high), ULN2003 Darlington output at C4-10, is close to ground potential. This prevents erase current switch Q2 from turning on and disables write current return path. During Write Mode, the anode of CR3 is pulled up to +5.7 V. Q2 receives base current through A3-8, and provides current to erase coil of head. R11 serves as return for erase current, which is roughly 44 milliamps. Erase coil in head straddles both sides of read-write head, preventing write current from spreading into adjacent tracks on diskette.

When writing out to diskette, flux transistions are placed on surface of diskette by changing polarity of current flow in head's read-write coil. Write current enters read-write coil through its center tap, which is connected to return side of erase coil. Two of CA3146's transistors connected to R29 and R30 form a current mirror which drives pin three of CA3146.

This establishes write current return path. When writing out to disk, WR DATA causes a differential voltage to be applied to pins 2 and 4 of CA3146, which causes a differential current flow in write coil. Each polarity reversal places a flux reversal on diskette. (Current in R/W coil -6.8 ma P-P)

4. Write Protect Circuit

Ananlog Card only allows erase and write current to be generated when diskette has its write protect notch uncovered. If notch is absent (write protected), the Write Protech switch is held open even though diskette is fully inserted into drive. This causes pullup resistor R12 to disable G1-8, which causes WR REQ* signal to be pulled up to a false level by R15. This prevents write current mirror from supplying write current to head. Write Protect status is ent to Disk Conditioning circuitry on Main Logic board as W PROT.

If Write Protect notch has been uncovered, it cause Write Protect switch within drive to close. Phase 1 signal from the Disk Conditioning circuitry provides return path for current passing through switch. If Phase 1 signal is high, it indicates that Stepper Motor is in one of its two transient states between tracks. Write Protect circuits behave as they do when the diskette is write protected. This provides partial coverage against writing when Stepper Motor is off track.

5. Stepper Motor Drivers

A ULN2003 Darlington Buffer-Inverter, provides a current return path for each of four Steper Motor windings, Phase A through Phase D. Q1 provides windings with source current when dirve is enabled. Since input to each ULN2003 stage is provided by the Disk Conditioning circuit's 9334 Addressalbe Latch output, Stepper Motor is then under software control.

Stepping in from Track 0 towards Track 34 (towards hub), requires Stepper Windings to be energized in Phase A, B, C, D order. Each phase rotates Cam Follower enough to provide one-half track movement of Head and Carriage assembly. Phase Ad and C are energized when head is on track, and Phase B and D are between track positions. Once head is positioned to desired track, power is removed from Stepper Motor to reduce power consumption.

Stepping out requires Stepper Motor windings to be enegized in Phase D, C, B, A order. When booting, windings are pulsed enough times to guarantee that head is positioned over Track 0.

NOTE: UNLESS OTHERWISE SPECIFIED

1. THESE ITEMS ARE SUPPLIED WITH O.E.M. DISK DRIVE (ITEM 2).
2. ITEM 12 (CARRIAGE LOCK CARD) TO BE INSERTED AFTER UNIT IS ASSEMBLED.

REV	ZONE	ECO #	REVISION	APPD
00	..	441	INITIAL RELEASE	
B		018	ADDED ITEM 12, NOTE 2 & DETAIL A.	

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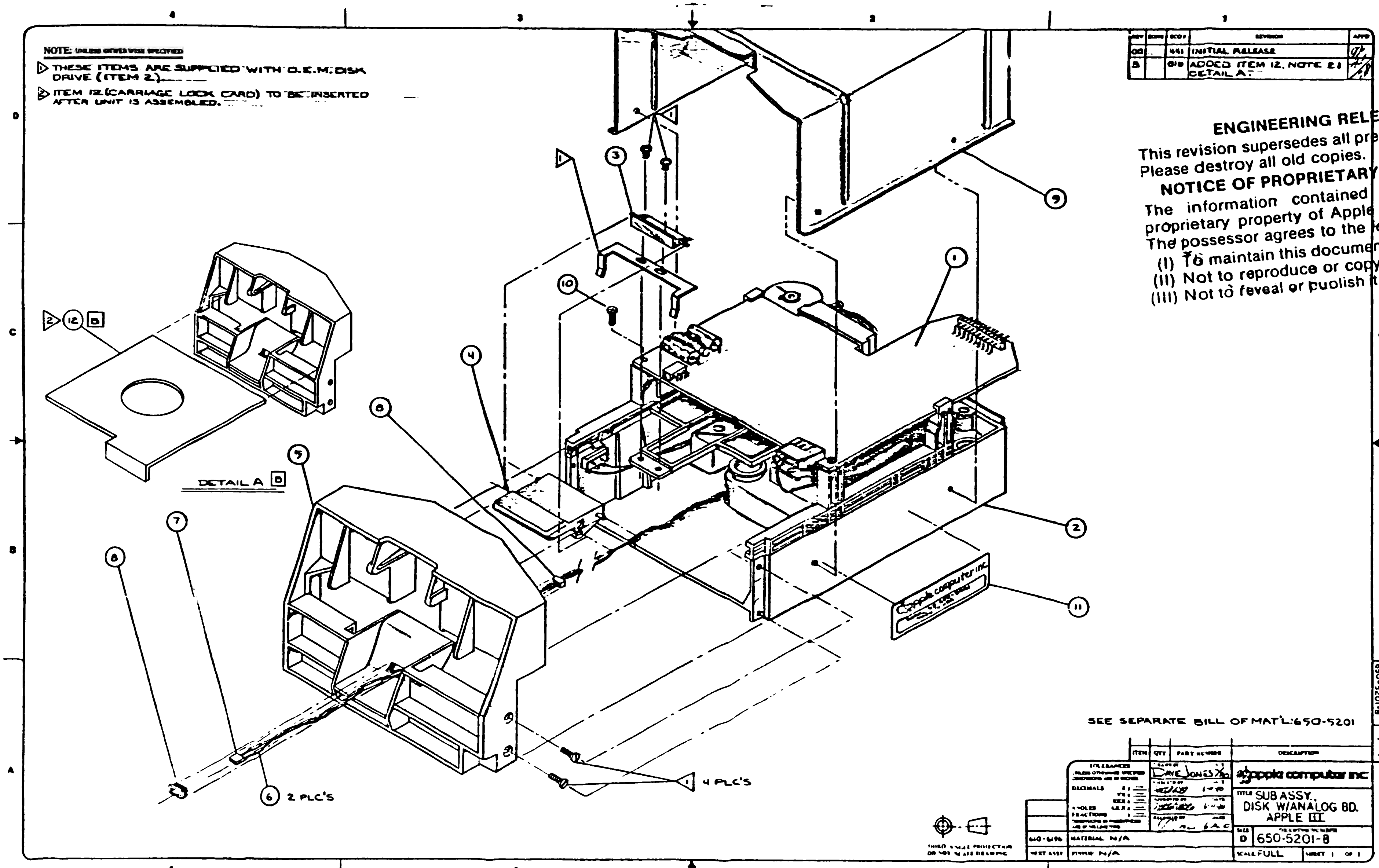

SEE SEPARATE BILL OF MAT'L: 650-5201

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMALS

ANGLES

FRACTIONS

DRAWN BY Dave Jones

apple computer inc

TITLE SUB ASSY., DISK W/ANALOG BD. APPLE III

SIZE D DRAWING NUMBER 650-5201-B

640-6196 MATERIAL N/A

NEXT ASSY FINISH N/A

SCALE FULL SHEET 1 OF 1

DRAWING NUMBER 650-5201-B SH 1 OF 1

THIRD ANGLE PROJECTION DO NOT SCALE DRAWING

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DOCUMENT NO. 064-0156

PAGE 5 OF 14

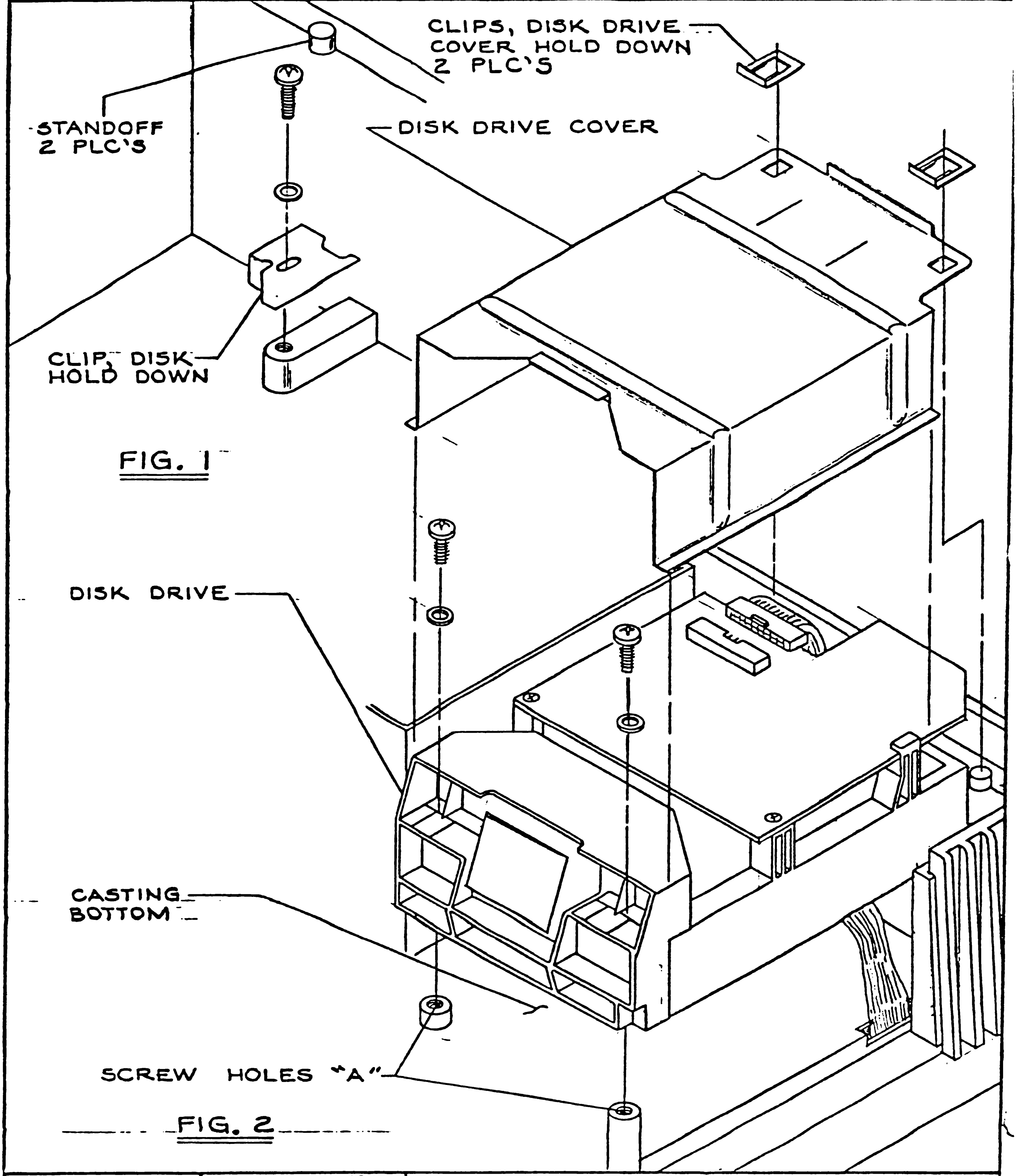


FIG. 1

FIG. 2

DRAWN BY	OPERATION NO.	TITLE
	010	INSTALL DISK DRIVE

APPLE III

DISK ENABLE(S)

1) TO ENABLE THE INTERNAL DRIVE 1, THE FOLLOWING CODE SHOULD BE TYPED IN: $\overline{\text{C0EA}}$ @ PIN #10 (L13)

2) TO ENABLE THE $\overline{\text{EXT.}}$ DRIVES (1,2,OR3), THE FOLLOWING CODE MUST BE TYPED IN:

$\overline{\text{C0EB}}$ @ PIN #10 (L13)

3) THE FOLLOWING TRUTH TABLE WILL EXPLAIN HOW DRIVES ($\overline{\text{INT}}$ AND $\overline{\text{EXT}}$) *0, 1, 2 AND 3 ARE ENABLED

* 0 ≡ INT. DRIVE

	DRIVE#	CODES TO TYPE IN	ENABLE	A1	A0	Z0	Z1	Z2	Z3	FROM J11(LS
			1	DON'T CARE	DON'T CARE	1	1	1	1	
1I	0	C0D4, C0D2, C0D0	0	0	0	0	1	1	1	★
1E	1	C0D2, C0D1	0	0	1	1	0	1	1	★
2E	2	C0D3, C0D0	0	1	0	1	1	0	1	PIN #6 J11 (LS139)
3E	3	C0D3, C0D1	0	1	1	1	1	1	0	PIN# 7 J11 (LS139)

★ ≡ COINCEDENTAL LOGIC LEVELS.

4) C0E9 WILL ENABLE J11 (LS139), HENCE THE APPROPRIATE DRIVE WILL BE ENABLED.

EXAMPLE:

LETS ENABLE DRIVE #2

A) TYPE IN THE CODE : C0EB

B) TYPE IN THE CODE : C0D3 AND C0D0

C) TYPE IN THE CODE : C0E9 NOW DRIVE #2 IS ON

D) TYPE IN THE CODE : C0E8 NOW DRIVE #2 IS OFF. S. WOITH

281

apple computer inc.

Title: Apple /// Final Test

Purpose: This test is for the assembled Apple /// and for testing Apple /// modules.

A. Equipment:

1. B/W Monitor with cable
2. Color Monitor, Sup'r'mod II, and adaptor (make your own adaptor)
3. (3 cables) External Disk. Paddle Port, External Speaker Cables
4. External Speaker Test Box
5. RS-232 Test Adaptor
6. Printer test card
7. (4 each) Interrupt test cards
8. Apple /// Test Diskette (889-0009 rev R)

B. Equipment Setup for Part 1 of test: (Note: Unless noted otherwise, ALWAYS make sure that the power is OFF, before connecting or disconnecting ANYTHING from the Apple ///.)

1. Connect all of the power cords to a suitable AC outlet. Note: Make sure that all power switches are in the OFF position before plugging in any equipment.

2. Connect the B/W monitor cable to the RCA video output jack.

3. Connect the Color Monitor/Sup'r'mod II to the DB-15 jack.

4. Connect the joystick as follows:
    a. Connect the paddle port cable connector to the external disk drive socket.
    b. Connect the 2 DB-9 plug to the 2 DB-9 sockets. (The one with the shortest cable connects to the socket nearest the external drive connector, Port A. The other connects to Port B.

5. Plug one Interrupt test card into each of the four slots on the Apple /// logic board.

6. Plug the RS-232 Test Adaptor into the DB-25 connector on the logic board. (P/N 890-0130)

7. Insert the Apple /// Test Diskette into the drive and close the drive door.

C. Test Procedure: (for part 1 of the test.)
Follow the test procedure described in this section. The test should run as described. If there is a failure, some of the tests will automatically proceed to the next test, while others will require the operator to press certain keys, to tell the system what has failed. Proceed through all of the tests. If the system will not proceed through all of the tests, indicate on the RRT which test failed. Reject and repair any unit which does not perform as described in this procedure.

*TEST DISKETTES HAVE BEEN KNOWN TO CRASH - KEEP AN EXTRA COPY ON HAND

1. Power On. Turn the power supply switch on. The unit will perform a self test first. If the self test passes, the disk will boot. If there is a failure in the self test, or the disk drive does not boot, record the failure on the RRT and send the logic board for rework. (ALWAYS TURN THE POWER OFF BEFORE DISCONNECTING ANYTHING FROM THE LOGIC BOARD.) When the disk drive boots, you will hear an audio signal of three beeps, followed by two beeps. You will then see a menu. Press the 1 key on the keyboard to run Automatic Test 1.

2. Interrupt test. The interrupt test will run automatically. If you see any of the following error messages, attempt to repair the A3 system and re-run the test. Write the failure down on the RRT.

ERROR MESSAGE	SUGGESTED ACTION TO TAKE
unable to set or clear D.xxx	6522 at H-10 (U 73) *
unable to set or clear E.xxx	6522 at G-10 (U 97) *
(anything) from SLOT X	check slot for bad connector

* locations will be as follows for the "NEW" logic board:

D.xxx	6522 at B-6
E.xxx	6522 at B-4

3. Video Test. The video tests will be loaded and run next. At the beginning of each test the screen will briefly display the name of the test being performed next and which keys to press, depending on the results. For reference, the following table lists the keys used for all of the video tests:

Space bar	Test passes
Return key	Test fails
Escape key	Abort video test (QUIT)
Left arrow key	Retry the test

Except for the text mode test, each of the tests will display the same pattern. A picture of Winston Churchill will appear in the upper right corner. The lower half of the screen will display the following message:

> If you can read this, and
> the test patterns above
> are clear, press space bar.
> Otherwise, press return.

a. HIRES MODE PAGE 1 - B & W pattern
b. HIRES MODE PAGE 2 - B & W pattern (same as above)
c. 280 x 192 COLOR HIRES MODE PAGE 1 - Will appear as a negative image. The color monitor will show red and black.

d. 280 x 192 COLOR HIRES MODE PAGE 2 - Will appear as a green and white (or possibly green and yellow) pattern.
e. SUPER HIRES MODE PAGE 1 - B & W pattern (same as above)
f. SUPER HIRES MODE PAGE 2 - B & W pattern (same as above)
g. AHIRES TEST PAGE 1 - On this and the following test the screen will be divided into 4 horizontal sections, each one being a different color. The top half of Winston Churchill and the diagonal pattern should be VIOLET. The bottom half of Winston Churchill and the diagonal pattern should be BLUE. The first two lines of the message should be GREEN, and the last two lines of the message should be GOLD or ORANGE.
h. AHIRES TEST PAGE 2 - This test should display the same four color bars as the above test.
i. COLOR BAR 7 GRAY SCALE TEST - will show vertical bars of different colors on the color monitor and bars of varying brightness on the B & W Monitor. The border is blue and the colors are : (from left to right) white, aqua, yellow, green, pink, grey, orange, brown, light blue, medium blue, grey, dark green, light purple, dark blue, magenta, and black. These colors correspond to white darkening to black on the Black & White monitor. (IMPORTANT. Make sure that there are sixteen (16) different shades on the Black & White monitor.)
j. Apple II TEXT MODE PAGE 1 - The screen will display the following:

```
THE QUICK BROWN FOX JUMPS OVER LAZY DOGS

abcdefghijklmnopqurstuvwxyz   0123456789
                               (inverse)


         . . .


     (flashing)
```

k. APPLE II TEXT MODE PAGE 2 - The screen will show the following:

```
22222222222222222222
22222222222222222222
22222222222222222222
                 222
                 222
                 222
22222222222222222222
22222222222222222222
22222222222222222222
222
222
222
22222222222222222222
```

```
22222222222222222222
22222222222222222222
```

l. APPLE /// 40 COLUMN TEXT MODE TEST - The screen will be filled with blocks of colors with the name of each color in each block.

m. APPLE /// 80 COLUMN TEXT MODE TEST - The screen will contain characters that are smaller than before. There will be 80 characters to a line. The characters may not appear clear on the color monitor, and this is OK. It is mainly important that they are clear on the B & W monitor. The first line of the display should read:

```
THIS LINE OF TEXT IS EXACTLY 80 CHARACTERS
   LONG AND USES THE ENTIRE SCREEN WIDTH
```

4. Keyboard Test. This test will load and display a pattern on the screen.

   a. Main Keyboard. Press the Left shift key and while holding it down press the 2 key. Press the Right shift key and while holding it down press the = key. Press the ctrl key and while holding it down press the A key. Press all of the remaining keys on the MAIN key board. Each time a key is pressed its character should disappear from the screen. Press the space bar last.
   b. Numeric Keypad. A new pattern should appear on the screen which corresponds to the numeric keypad. This test should perform the same as the main keyboard test.
   c. Special Function Keys.
      1. Press the Alpha-Lock key ONCE. It should lock into its new position.
      2. Press the space bar and hold it down.
      3. While still holding the space bar, press and hold both apple keys at the same time.
      4. Release all of the keys at the same time.
      5. Press the solid apple key and hold it down.
      6. While still holding down the solid apple key, press the space bar and hold it down.
      7. Release all of the keys at the same time.
   d. Keyboard Interrupt test. Press any key on the keyboard except the alpha-lock, shift, control, or either of the apple keys to perform this test.

5. Clock/Calendar Test: This test is available for testing the clock/calendar when it becomes incorporated into the system.

6. Serial Port Test: This test will also load and run automatically. If it fails, replace the ACIA chip (6551) and run the test again. If it still fails, write ACIA on the RRT and repair the main

logic board.

7. Joystick Port test: This test will run automatically. If any failures should occur, write the failure message on the RRT.

8. Test Results: The screen should show the following results:

```
                    TEST RESULTS

     A.  INTERRUPT               (PASSED)
     B.  VIDEO                   (PASSED)
     C.  KEYBOARD                (PASSED)
     D.  CALENDAR/CLOCK          (NOT TESTED)
     E.  ACIA PORT               (PASSED)
     F.  PADDLE PORTS            (PASSED)
     G.  RAM                     (NOT TESTED)
     H.  PRINTER PORT            (NOT TESTED)
     I.  DISK                    (NOT TESTED)
     J.  SOUND                   (NOT TESTED)
     K.  ROM                     (NOT TESTED)

     1.  AUTOMATIC TEST 1
     2.  AUTOMATIC TEST 2
    ESC ABORT TESTING
```

Tests A through F should always show passed, (except for test D) and tests G through K and test D should always show not tested. If any of tests A through F show failed, mark the RRT with the test that failed. If all of tests A through F show passed, proceed with part 2 of the Final test.

D. Equipment Setup for part 2 of test:

1. TURN THE POWER OFF!
2. Remove the following items from the logic board:
    a. The joystick cables
    b. The four interrupt test cards.
    c. The RS-232 test adaptor.
    d. The DB-15 video connector
3. Plug the Printer Test Card into slot 1, and connect the printer cable to the DB-9 connector nearest the disk drive sockets and the other cable to the external disk drive socket. Connect the external speaker plug to the 2-pin connector on printer test card.

E. Test Procedure: (for part 2 of the test.)
Please follow the test procedure described in this section. The test should run as described. Reject any assembly or unit which does not perform as described in this procedure. Complete all of the tests if possible. If the system will not perform any test, indicate on the RRT which test failed and diagnose, repair, and retest.

1. POWER ON. Turn the power on and the unit should perform

a self-test and boot just as it did earlier. If there is a failure in the self-test or the drive does not boot, record the failure on the RRT and repair. ALWAYS TURN THE POWER OFF BEFORE DISCONNECTING ANYTHING FROM THE LOGIC BOARD. After the disk boots, a menu will appear on the screen. Press the 2 key to run automatic test 2.

2. Ram Address Test. This test will load and run automatically. The test results will depend on the amount of ram in the memory board. If the memory board is a 256K board the results should say "RAM MAP GOOD FOR A 256K SYSTEM". If the correct message appears, press the space bar, otherwise press the return key. Faulty RAM chips are reported in a message that identifies the board location of the chip in error.

   Note: If a fault is discovered while testing the RAM on the 12 volt board, disregard the chip referred to in the error message and run the Final Test Revision 14. Revision 14 will correctly identify the chip in error. Revision R reports bad chip locations as defined on the 5 volt board and these messages are innaccurate for the older board.

   If the space bar is pressed the system will perform a test on all of the ram in the system and report any failures. For this reason it is very important for you to have made the correct decision for the ram map address test above. If the system is a 256K system and the ram map says good for a 128K system and you press the space bar, only half of the ram will be tested and you may incorrectly PASS a system which FAILED.

3. Printer Port Test. This test will run automatically.
4. Disk Controller Test. This test will run automatically.
5. Sound Test.
   a. C030 SOUND TEST - The speaker will beep on and off.
   b. C040 SOUND TEST - The speaker will beep on and off as before but at a different pitch. Press the space bar if you hear the sound, and return if you do not.
   c. Connect the external speaker cable from the printer port test card to the external speaker jack on the back of the Apple /// and press the return key.
   d. FFE0 SOUND TEST - The sound from the speaker should start quietly and grow gradually louder. It should then repeat. Press the space bar if it performs as described here, and press the return key if it does anything else. The sound should be coming from the EXTERNAL speaker.
   e. Disconnect the external speaker cable from the logic board and press return. (NOTE: These are the ONLY times that you can connect or disconnect anything from the Apple /// with the power still on, and the ONLY thing that can be connected or

disconnected is the external speaker cable.)

f. The same sound as the previous test should be heard. The sound should come from the INTERNAL speaker again.

6. Rom Test. This test will load and run automatically.
7. Test Results: The screen should show the following results:

```
                    TEST RESULTS

A. INTERRUPT                          (NOT TESTED)
B. VIDEO                              (NOT TESTED)
C. KEYBOARD                           (NOT TESTED)
D. CALENDAR/CLOCK                     (NOT TESTED)
E. ACIA PORT                          (NOT TESTED)
F. PADDLE PORTS                       (NOT TESTED)
G. RAM                                (PASSED)
H. PRINTER PORT                       (PASSED)
I. DISK                               (PASSED)
J. SOUND                              (PASSED)
K. ROM                                (PASSED)

1.  AUTOMATIC TEST 1
2.  AUTOMATIC TEST 2

ESC ABORT TESTING
```

Tests A through F should always show not tested, and tests G through K should always show passed. If any of the tests G through K show failed, record which test failed on the RRT and repair the module under test.

8. Additional keyboard tests:
   - a. Press any key and hold it down. The key should automatically repeat.
   - b. While still holding the same key down, press the Apple key nearest the space bar and the repeating key should repeat at a faster rate. (Approximately twice the speed)
   - c. Press the right arrow key and the cursor dot should move to the right. Press the key harder and it should move twice as fast.
   - d. Repeat the same test with the left arrow and down arrow keys. They should behave in the same manner described for the right arrow key except that they will of course move left and down, respectively.
   - e. Press and hold the ctrl key with some finger on your left hand and then press and hold the Apple Key next to the alpha lock with your left thumb. Use your other hand to press the Reset key. The system should respond with a right

pointing arrow and a blinking line cursor.

   f. If any of these keyboard tests do not perform exactly as described here, record the failure on the reject tag, and send the unit for rework.

F. If the logic board passes all of the tests as described above, turn the power off and complete the RRT. If any of the tests failed, record the appropriate information on the RRT and repair. Retest after repair.

G. If you have a system or module that passes all these tests but suspect it to have a failure run other software on the unit/modules. Examples: Business Basic, AII Emulation, A /// Dealer Diagnostic.

PRE-RELEASE
VERSION

16 SECTOR DISK III FINAL TEST (1000T)

DESCRIPTION

1000T is a general purpose internal disk exercizer. It performs 1000 reads of ramdomly selected tracks on the disk. It is to be used as a diagnostic tool and not as a qualification/acceptance test. The rest of this document provides a short description of how to interpret the displayed results.

When you first boot this diskette you will observe:

```
"*** 16 SECTOR DISK III FINAL TEST ***"
```

This will indicate that the test booted up correctly with no problems. You will then observe the following:

```
                TRACK ERRORS
                ------------
 3    (0)   0        *     19    (0)     0
 4    (0)   0        *     20    (0)     0
 5    (0)   0        *     21    (0)     0
 6    (0)   0        *     22    (0)     0
 7    (0)   0        *     23    (0)     0
 8    (0)   0        *     24    (0)     0
 9    (0)   0        *     25    (0)     0
10    (0)   0        *     26    (0)     0
11    (0)   0        *     27    (0)     0
12    (0)   0        *     28    (0)     0
13    (0)   0        *     29    (0)     0
14    (0)   0        *     30    (0)     0
15    (0)   0        *     31    (0)     0
16    (0)   0        *     32    (0)     0
17    (0)   0        *     33    (0)     0
18    (0)   0        *     34    (0)     0

 -------------------------------------
TOTAL:           SEEK:          DATA:
TIME:            ADDR:          AVER:
```

WHAT DOES IT ALL MEAN?

The first column, numbered 3 to 18, and the column with numbers going from 19 to 34 represent track numbers. The column in brackets represents the number of seek occurances that occur for each track. The column that has zeroes is the number of errors that were encountered for each track. You will observe that each time a track is read, it is shown in inverse, the number of occurances is incremented. If any seek, address, or data errors are found the number of errors are displayed.

A summary of the disk test is displayed at the very bottom of the monitor screen. The following are definitions as to what the messages mean.

- TOTAL: -- the total number of errors for all tracks
- TIME: -- the number of track seeks performed for all tracks
- SEEK: -- the total number of track seek errors observed for all tracks
- ADDR: -- the total number of address errors observed for all tracks
- DATA: -- the total number of data errors observed for all tracks
- AVGE: -- the number of track seeks divided by the total number of errors observed for all tracks

NOTE: PLEASE MAKE BACKUP DISKETTES OF THIS 1000T DISKETTE

WHAT CAN THIS TOOL TELL ME?

This tool is useful for getting a good idea as to the performance of the A/// internal disk drive. Based on the results, 1000T can give you an indication of electrical and mechanical problems. Examples: Errors within a small range of tracks could indicate cam or rail problems. Multiple data errors could indicate head wear. Address/seek errors could indicate a poor motor control board. These examples are not absolute nor do they exhaust all possibilities. This tool is also very useful for debugging intermittant disk problems.

WARNING: Do not rely solely on this diskette as a pass/fail indicator. If you find very many errors, run other Disk tests such as the DSPEED and Disk Alignment Aide.

Catastrophic errors are eas~~il~~y to find - your monitor screen will display "FAILS TEST". Other than catastrophic errors your monitor screen will display "PASSED TEST" at the end of 1000 passes(seeks).

HAPPY HUNTING!!!

PRE-RELEASE
VERSION

APPLE /// TROUBLESHOOTING

The following flowchart is a guide for troubleshooting the Apple ///. You will carry out various troubleshooting steps based on symptoms that may occur when first booting up or that may be found by running the Dealer Service Diagnostics. Start with the instruction in Box 1 of the flowchart. Then follow the operation of the Apple /// through the flowchart until you reach one of the lettered boxes (A through Q). Each lettered box has a list of numbers in it; each number corresponds with one of the troubleshooting steps listed on the following page. The order of the troublshooting steps in each box is based on two rules:

1) Check out the more likely causes of the problem before the less likely causes.

2) Make the checks that can be done quickly and easily before those that take more time and energy.

Rule 1 is broken only when rule 2 applies.

Once you have produced the problem symptom on the Apple ///, the first thing you should do before trying any of the numbered steps below is:

a) Power OFF.

b) Check to make sure all connecting cables are properly hooked up.

c) Check all boards to make sure all IC chips are properly seated.

d) Power ON again to see if the problem still exists.

ALWAYS POWER OFF BEFORE PERFORMING ANY OF THE STEPS BELOW.
CARRY OUT THE DESIGNATED STEP.
THEN POWER ON AGAIN TO SEE IF THE PROBLEM HAS BEEN ELIMINATED.

Each swap step listed below involves exchanging a known good part from your spares kit with the questionable part from the Apple ///. When swapping, first just connect the cable(s) to the new module so you can see if the swap fixes things or not. Don't fully install the new module and screw everything down---if the new module doesn't solve the problem you'll just have to take it out again.

HERE ARE THE STEPS REFERRED TO IN THE BOXES ON THE DIAGNOSTIC FLOWCHART:

1) Swap the appropriate connecting cable.

    V = Video cable (if available)
    PS = Power Supply cable
    DD = Disk Drive cable
    KB = Keyboard cable

    (The keyboard and disk drive cables are identical to each other. Your Spares Kit may only list the DD cable, but you can use it whenever you need to swap the KB cable.)

2) Swap the power supply.

    a) Check the power supply fuse first; swap it if it's burned out.

3) Swap the drive.

    If the drive proves to be the problem, take the problem drive and further isoloate the defective module down to the analog card or mechanical assembly:

    a) Swap the analog card.

    b) Swap the mechanical assembly.

4) Swap the main logic board.

5) Swap the keyboard.

6) Swap the RAM memory board. (You may have to reload the new board with the RAM from the original board.)

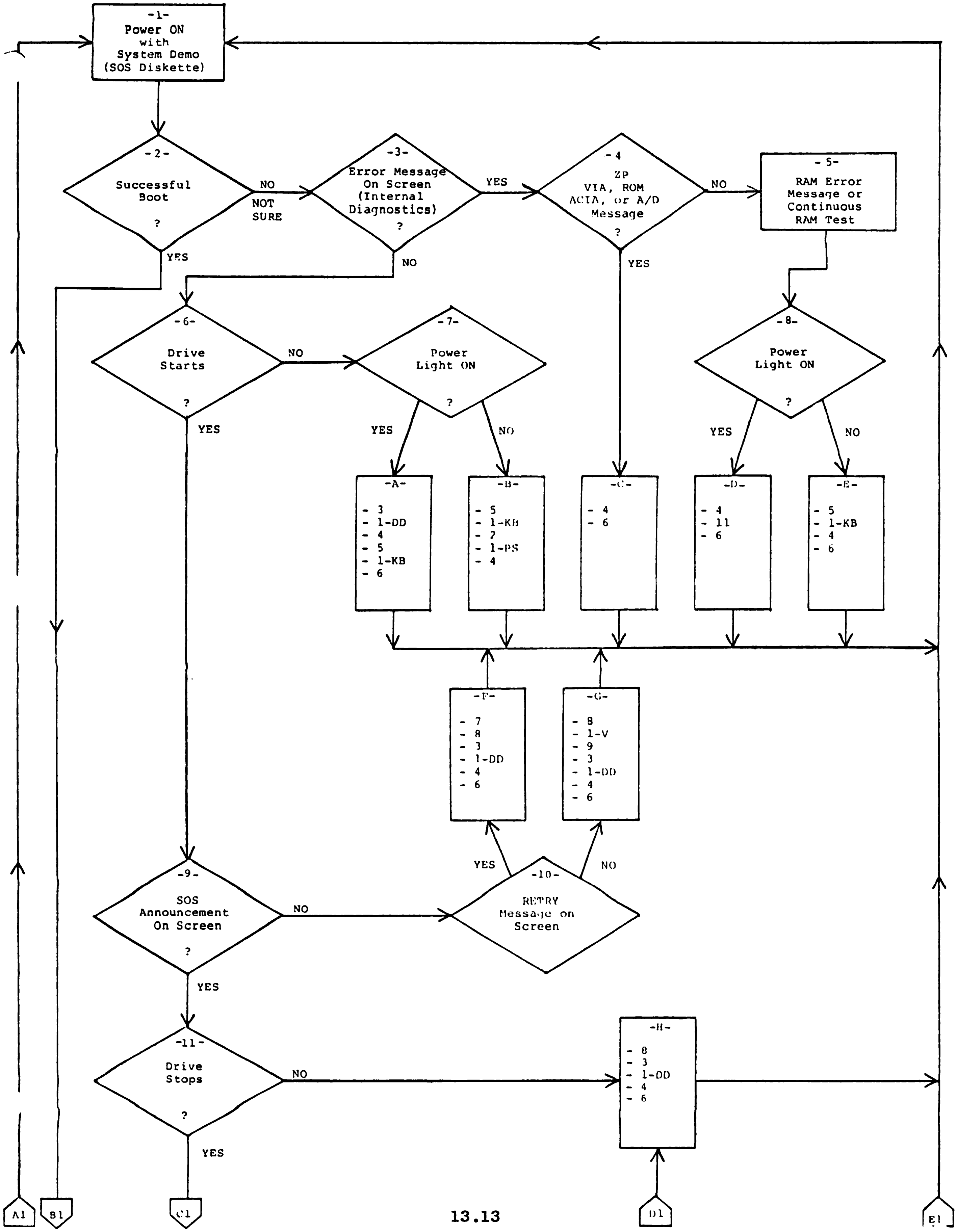
7) Try booting again.

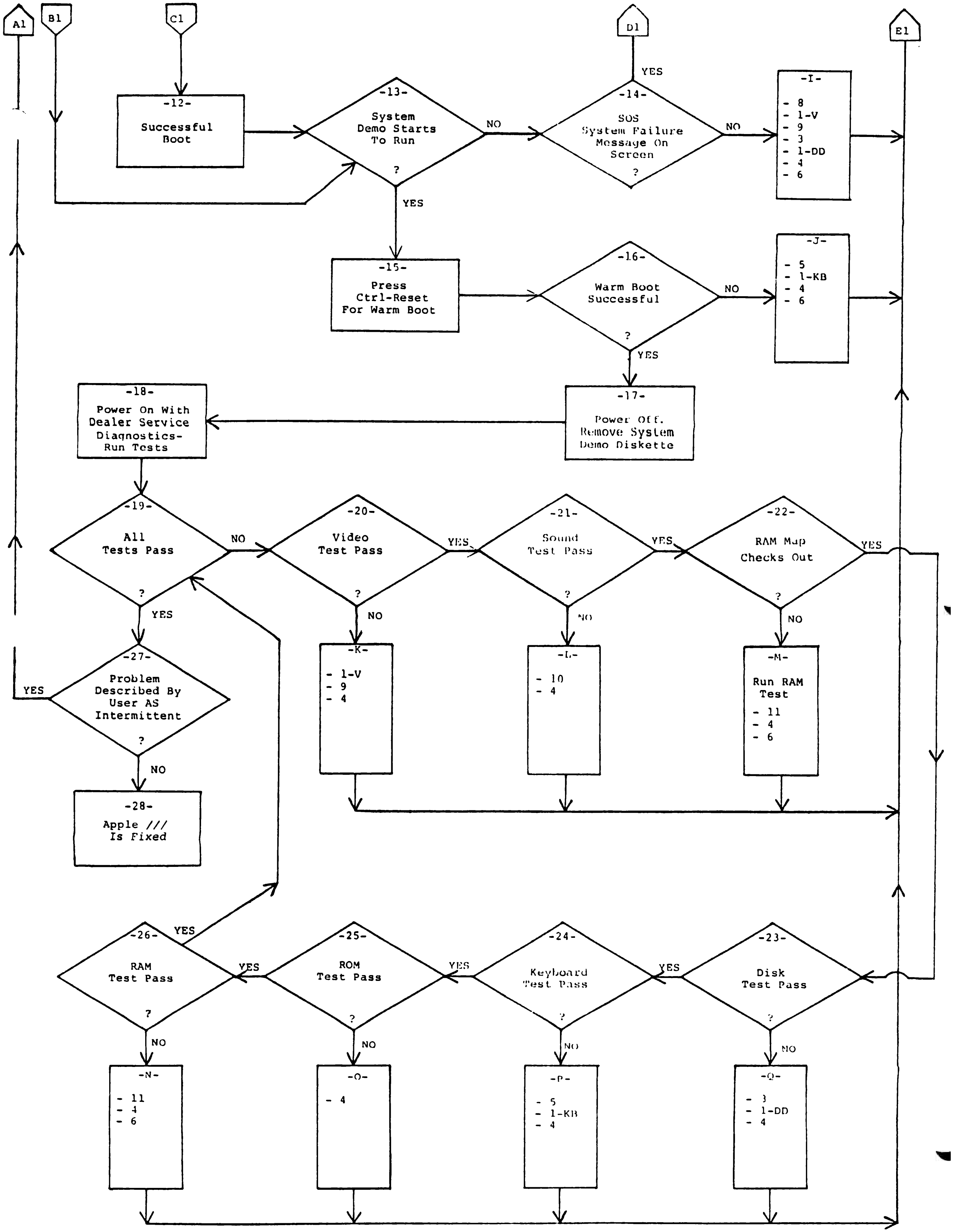
8) Try booting a different SOS boot diskette.

9) Swap the video monitor (if you have a spare available).

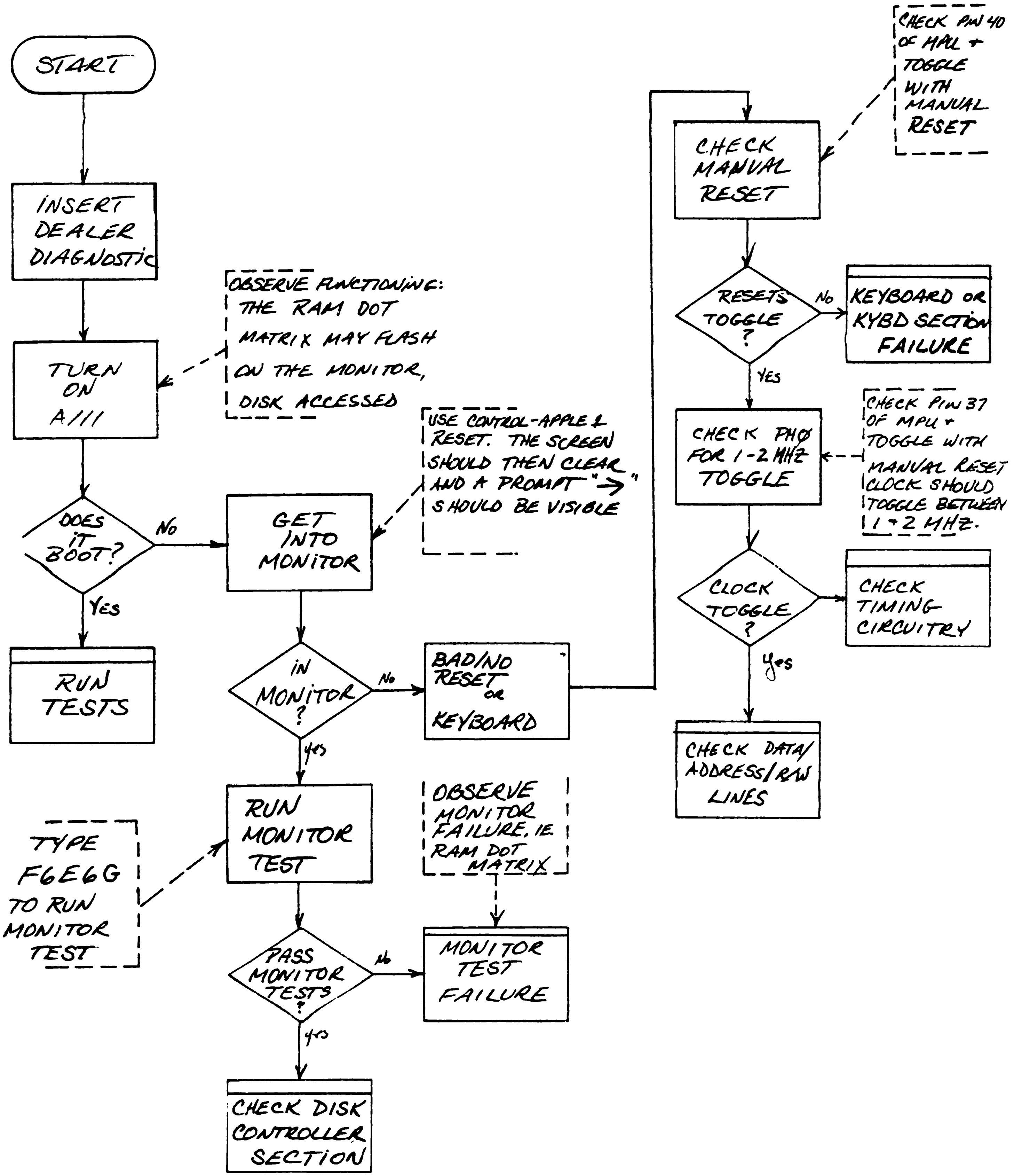
10) Swap the speaker (if you have a spare available).

11) Swap (or add) the designated RAM IC chips. (Consult the chip map in the Running Diagnostics Job Aid.)


-1-
Power ON
with
System Demo
(SOS Diskette)
-2-
Successful
Boot
?
NO
NOT
SURE
YES
-3-
Error Message
On Screen
(Internal
Diagnostics)
?
YES
NO
-4
ZP
VIA, ROM
ACIA, or A/D
Message
?
NO
YES
-5-
RAM Error
Message or
Continuous
RAM Test
-6-
Drive
Starts
?
NO
YES
-7-
Power
Light ON
?
YES
NO
-8-
Power
Light ON
?
YES
NO
-A-
- 3
- 1-DD
- 4
- 5
- 1-KB
- 6
-B-
- 5
- 1-KB
- 2
- 1-PS
- 4
-C-
- 4
- 6
-D-
- 4
- 11
- 6
-E-
- 5
- 1-KB
- 4
- 6
-F-
- 7
- 8
- 3
- 1-DD
- 4
- 6
-G-
- 8
- 1-V
- 9
- 3
- 1-DD
- 4
- 6
YES
NO
-9-
SOS
Announcement
On Screen
?
NO
YES
-10-
RETRY
Message on
Screen
-11-
Drive
Stops
?
NO
YES
-H-
- 8
- 3
- 1-DD
- 4
- 6
A1
B1
C1
D1
E1


A1
B1
C1
D1
E1
-12-
Successful Boot
-13-
System Demo Starts To Run ?
NO
YES
-14-
SOS System Failure Message On Screen ?
YES
NO
-I-
- 8
- 1-V
- 9
- 3
- 1-DD
- 4
- 6
-15-
Press Ctrl-Reset For Warm Boot
-16-
Warm Boot Successful ?
NO
YES
-J-
- 5
- 1-KB
- 4
- 6
-17-
Power Off. Remove System Demo Diskette
-18-
Power On With Dealer Service Diagnostics- Run Tests
-19-
All Tests Pass ?
NO
YES
-20-
Video Test Pass ?
YES
NO
-21-
Sound Test Pass ?
YES
NO
-22-
RAM Map Checks Out ?
YES
NO
-K-
- 1-V
- 9
- 4
-L-
- 10
- 4
-M-
Run RAM Test
- 11
- 4
- 6
-27-
Problem Described By User AS Intermittent ?
YES
NO
-28-
Apple /// Is Fixed
-26-
RAM Test Pass ?
YES
NO
-25-
ROM Test Pass ?
YES
NO
-24-
Keyboard Test Pass ?
YES
NO
-23-
Disk Test Pass ?
YES
NO
-N-
- 11
- 4
- 6
-O-
- 4
-P-
- 5
- 1-KB
- 4
-Q-
- 3
- 1-DD
- 4

A/// NO BOOT FLOW DIAGRAM


START
INSERT DEALER DIAGNOSTIC
TURN ON A///
OBSERVE FUNCTIONING: THE RAM DOT MATRIX MAY FLASH ON THE MONITOR, DISK ACCESSED
DOES IT BOOT?
No
Yes
RUN TESTS
GET INTO MONITOR
USE CONTROL-APPLE & RESET. THE SCREEN SHOULD THEN CLEAR AND A PROMPT "→" SHOULD BE VISIBLE
IN MONITOR ?
No
Yes
BAD/NO RESET OR KEYBOARD
RUN MONITOR TEST
TYPE F6E6G TO RUN MONITOR TEST
OBSERVE MONITOR FAILURE, IE. RAM DOT MATRIX
PASS MONITOR TESTS ?
No
Yes
MONITOR TEST FAILURE
CHECK DISK CONTROLLER SECTION
CHECK MANUAL RESET
CHECK PIN 40 OF MPU + TOGGLE WITH MANUAL RESET
RESETS TOGGLE ?
No
Yes
KEYBOARD OR KYBD SECTION FAILURE
CHECK PHØ FOR 1-2 MHZ TOGGLE
CHECK PIN 37 OF MPU + TOGGLE WITH MANUAL RESET CLOCK SHOULD TOGGLE BETWEEN 1 + 2 MHZ.
CLOCK TOGGLE ?
Yes
CHECK TIMING CIRCUITRY
CHECK DATA/ADDRESS/R/W LINES

apple computer inc.

5V MEMORY BOARD

RAM

TROUBLESHOOTING

PROCEDURE

AUG 1982

5V VOLT MEMORY BOARD RAM TROUBLESHOOTING PROCEDURE

To start with, be sure that your problem is caused by the 5V Memory Card. Some problems on the motherboard of the Apple /// will cause the symptoms similar to those caused by a bad 5V Memory Card. To check, replace the Memory Card with a known good one and check to see if the symptoms have disappeared.

1) If the problem has been isolated to the Memory Card, reconnect the bad 5V Memory Card in the Apple /// system under test and try to boot the Apple /// Confidence Diskette Version 1.1.

2) If it boots, select the memory test.

3) Relate your system´s symptoms to the symptoms on the Apple /// 5V Memory Card Troubleshooting Chart.

4) The corrective actions are listed in the order of most probable cause; therefore perform the corrective action in the order presented.

5) If all of the possiblities have been exhausted and the problem still exists, replace the bad 5V Memory Card with a good one and send the bad one back to a Level II repair center.

Note: This interim RAM troubleshooting procedure is to be used with the Confidence Diskette Version 1.1. The memory test, in the current Confidence Diskette, does not test each and every memory location in RAM. This procedure will be superceded by the next version of the A/// Dealer Diagnostic.

Apple /// 5V Memory Card Troubleshooting Chart

Symptom	Recommened Action
Black Screen on Monitor; drive does not boot.	Replace RAM chips B10 - B17 one at a time; Replace the non-RAM chips at locations D2 and E2.
Monitor Screen contains garbage; Drive may try to boot.	Replace RAM chips B2 - B9 one at a time; Replace the non-RAM chips at locations D2 and E2.
Confidence Program loads into memory, displays menu, but will not run.	Replace the non-RAM chips at locations D2 and E2; Replace RAM chips B2 - B17 one at a time.
Memory test runs; displays RAM error message at the bottom of the screen.	Decode the message using the procedure on Page 4. Replace the failed RAM.
Memory test runs; sections of the memory map are missing.	Determine which section on the Memory Card contains the failed RAM using the procedure on page 8. Replace the RAM chips in that section one at a time; Replace non-RAM chips at locations D2 and E2.

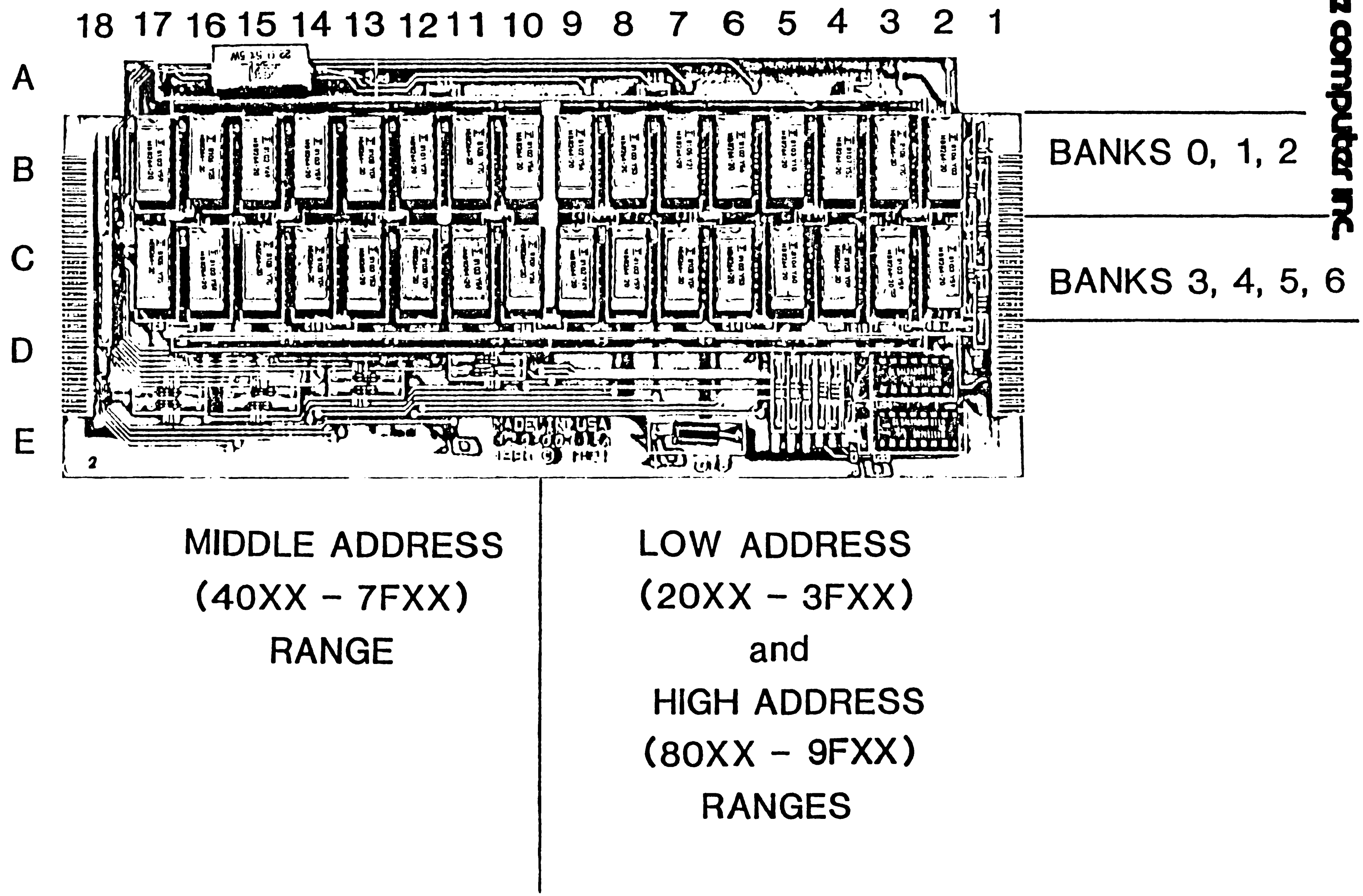

18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A
B
C
D
E
BANKS 0, 1, 2
BANKS 3, 4, 5, 6
MIDDLE ADDRESS
(40XX – 7FXX)
RANGE
LOW ADDRESS
(20XX – 3FXX)
and
HIGH ADDRESS
(80XX – 9FXX)
RANGES

FIGURE 1

TRANSLATING ERROR MESSAGES INTO PHYSICAL RAM LOCATIONS

When you get an error message from the RAM test, you must translate it to determine which chip caused the failure. This procedure will show you how to do that. For example, suppose we get the error message:

```
BNK 83, ADR 20XX, EXP DF, GOT 5F
```

That means in Bank 83, Address Range 20XX, we expected DF but got 5F.

Now, how do you translate that into what to do?

1) To find out which row the failed RAM chip is in, disregard the 8, and look at the second number, in this case 3. If the second number is 0, 1, or 2, the bank is in row B. If the second number is 3, 4, 5, or 6, the bank is in row C. (See Figure 1). In our example, the bank was BNK 83, so we know it is in row C.

2) Now the meaning of the address. There are three address ranges, low, middle, and high. Low and high are in columns 2-9, and middle is in columns 10-17. Look at Figure 1 for the specific address ranges. In our example, the address was 20XX (which is in the low address range), so we see that the trouble is in columns 2-9.

3) The problem is now narrowed down to a block of eight chips, the ones located in row C, columns 2 - 9 (positions C2 - C9). To find which of the eight it is, we have to decode the EXP and GOT parts of the message.

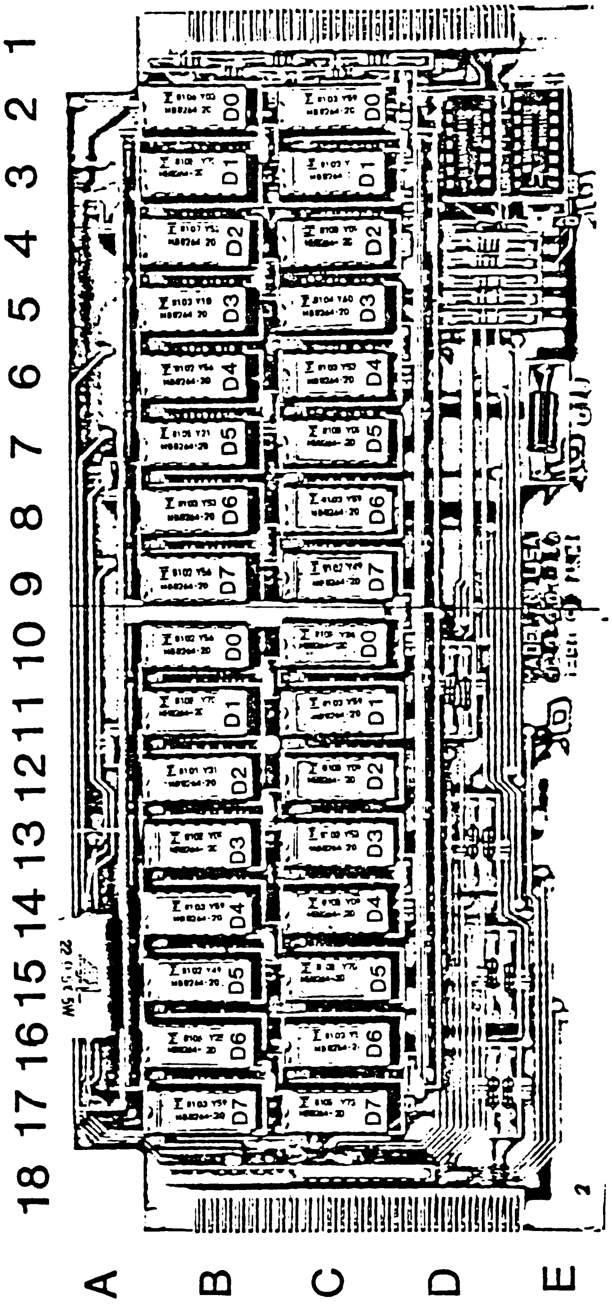


FIGURE 2

4) Translate the two hexadecimal digits from the EXP into binary.

HEX	BINARY	HEX	BINARY	HEX	BINARY	HEX	BINARY
0 =	0000	4 =	0100	8 =	1000	C =	1100
1 =	0001	5 =	0101	9 =	1001	D =	1101
2 =	0010	6 =	0110	A =	1010	E =	1110
3 =	0011	7 =	0111	B =	1011	F =	1111

EXAMPLE (DF): D=1101, F=1111, DF=11011111

5) Translate the two hexadecimal digits from the GOT onto binary.

EXAMPLE (5F): 5=0101, F=1111, 5F=01011111

6) Determine the binary digit (bit) that is different between the EXP and the GOT. The leftmost bit is D7 and the rightmost bit is D0. In our example the D7 bit is different. This indicates that the chip marked D7 in Figure 2 in the position C9 (remember, we already got it down to C2 - C9) is defective.

```
                 D        76543210
EXAMPLE:        EXP    DF=11011111
                GOT    5F=01011111
                       ===========
                          X-------  (D7 is different)
```

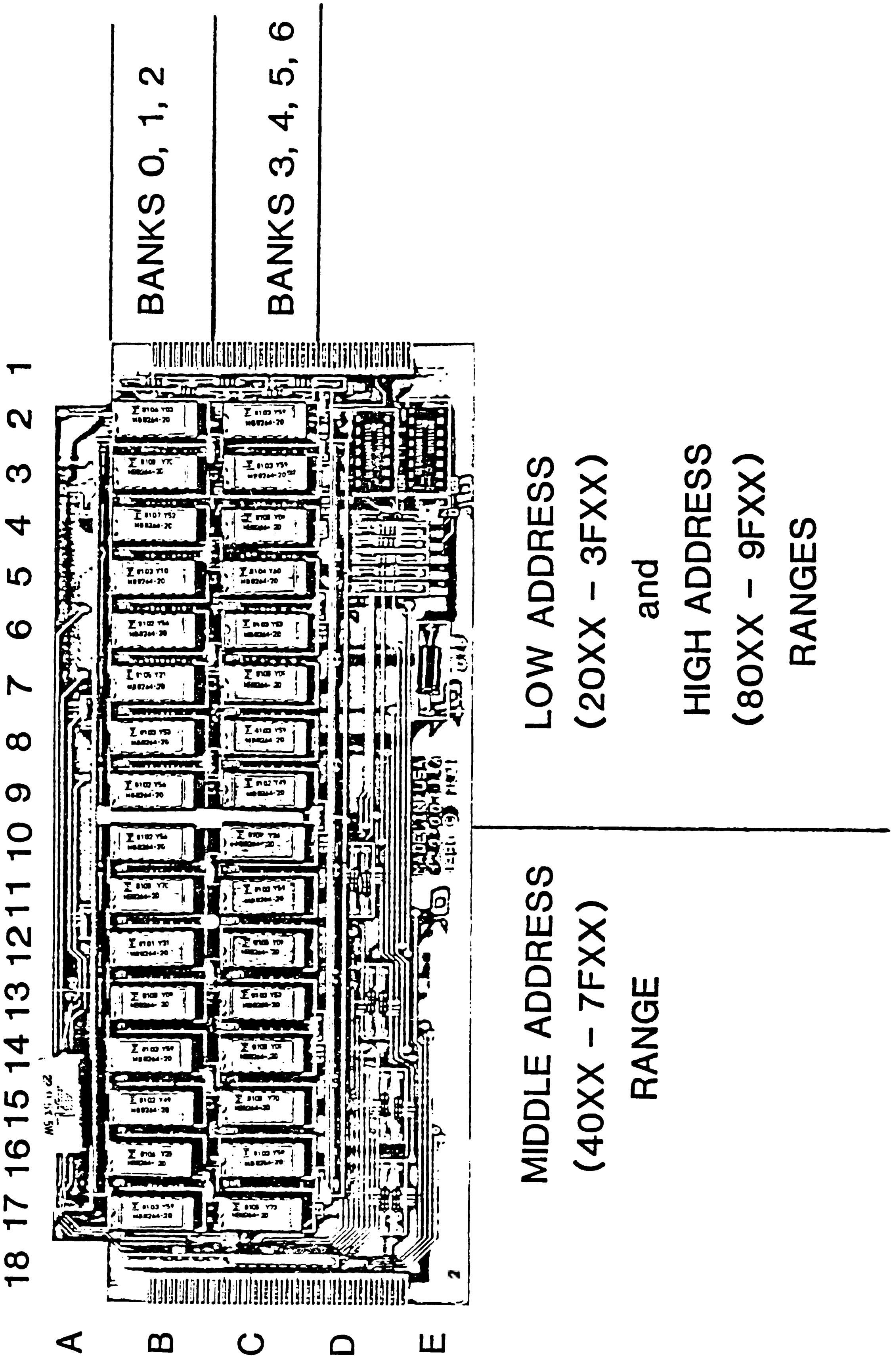

BANKS 0, 1, 2
BANKS 3, 4, 5, 6
LOW ADDRESS (20XX - 3FXX) and HIGH ADDRESS (80XX - 9FXX) RANGES
MIDDLE ADDRESS (40XX - 7FXX) RANGE
A
B
C
D
E

FIGURE 3

TRANSLATING MISSING SEGMENTS OF THE MEMORY MAP DISPLAY INTO PHYSICAL RAM LOCATIONS

Sometimes the Memory Test does not give an error message, but instead erases a portion of the memory map display, and continues to test the RAM. Figure 4 below is an example of a memory map display with a missing segment.

1) First, notice the bank(s) that are missing in Figure 4 (listed down the left side). Correlate the bank(s) to the physical row of memory. In our example, banks 3,4,5 and 6 are missing. This means that the failed RAM is somewhere in row C.

2) Determine the address range(s) that are missing (listed across the top.) Translate the address range(s) to the physical section. In our example, address ranges 50XX - 5FXX and 70XX - 7FXX are missing. This falls within the address range 40XX - 7FXX and tells us that the failed RAM is one of the eight which is physically located between C10 - C17 on the memory board.

3) Change the chips in that section, one at a time, retrying the RAM test each time. If the problem still remains, replace the old RAM back in the board and try another of the eight.

4) If you change all eight chips without fixing the problem, try the two non-RAM chips at location D2 and E2 on the 5V Memory Board.

```
                                        ADDRESS RANGES
                                        (20XX - 9FXX)

 K      Bank    2        3        4        5        6        7        8        9     9
                0        0        0        0        0        0        0        0     F
 64     0       XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
 96     1       XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
128     2       XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
160     3       XXXXXXXXXXXXXXXXXXXXXXXXXX---------XXXXXXXXX---------XXXXXXXXXXXXXXXXX
192     4       XXXXXXXXXXXXXXXXXXXXXXXXXX---------XXXXXXXXX---------XXXXXXXXXXXXXXXXX
224     5       XXXXXXXXXXXXXXXXXXXXXXXXXX---------XXXXXXXXX---------XXXXXXXXXXXXXXXXX
256     6       XXXXXXXXXXXXXXXXXXXXXXXXXX---------XXXXXXXXX---------XXXXXXXXXXXXXXXXX
Extension ($8F) XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
```

FIGURE 4

SUMMARY

Translating Error Messages Into Physical RAM Locations

Error Message: BNK 84, ADR 37XX, EXP 40, GOT 48.

1. The physical row is determined by the bank number which is the bank is the last digit of the number in the BNK section. (Bank 4 in our example puts the problem in row C.)

2. Which half of the row is determined by the address range. Our example puts the problem in the right half of the Memory board (Columns 2-9).

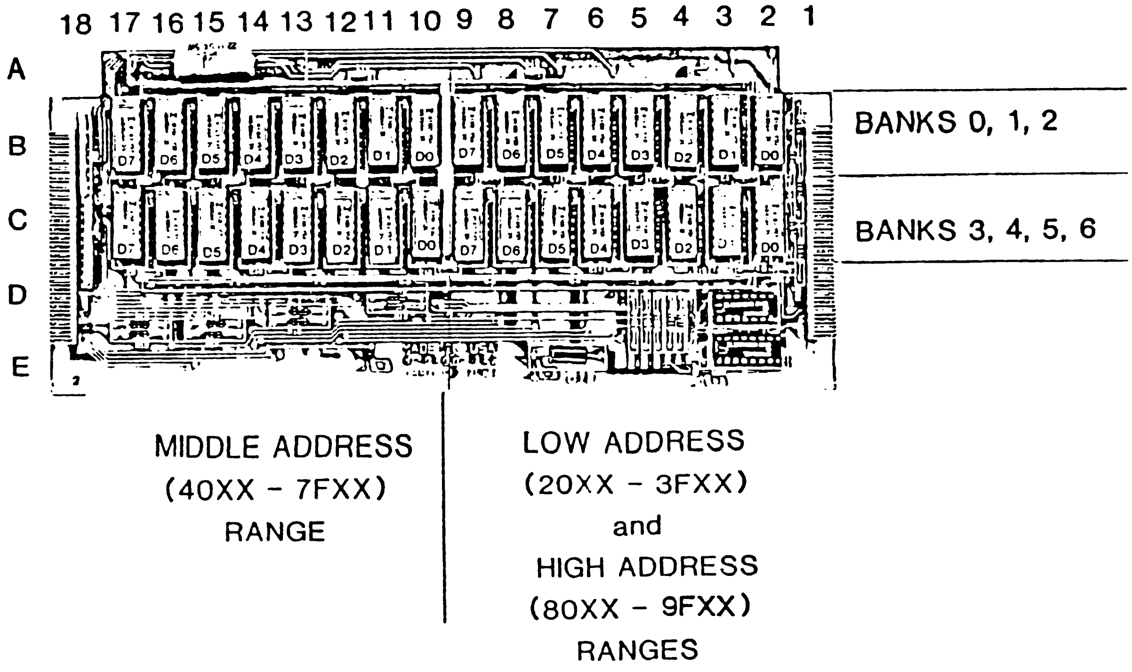
3. The location of the failed RAM chip within the half row is determined by decoding the EXP and GOT messages.

HEX	BINARY	HEX	BINARY	HEX	BINARY	HEX	BINARY
0 =	0000	4 =	0100	8 =	1000	C =	1100
1 =	0001	5 =	0101	9 =	1001	D =	1101
2 =	0010	6 =	0110	A =	1010	E =	1110
3 =	0011	7 =	0111	B =	1011	F =	1111

EXP (40): 4=0100, 0=0000, 40=01000000

GOT (48): 4=0100, 8=1000, 48=01001000

```
     76543210
40:  01000000
48:  01001000
=============
     ----X---   (D3 is different, so the RAM chip at
                 C5 is bad in our example.)
```


18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A
B
C
D
E
D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0
BANKS 0, 1, 2
BANKS 3, 4, 5, 6
MIDDLE ADDRESS (40XX - 7FXX) RANGE
LOW ADDRESS (20XX - 3FXX) and HIGH ADDRESS (80XX - 9FXX) RANGES

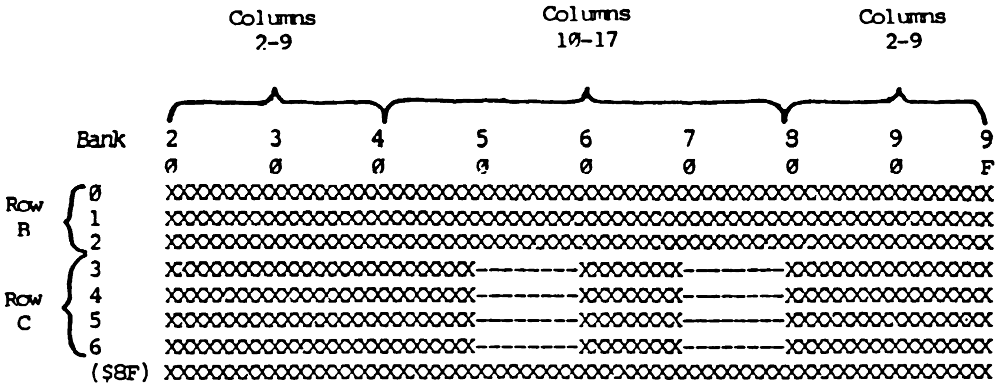
Translating Missing Sections on the Memory Map Display into Physical RAM Locations

1. Determine which row the failed RAM is located from the Memory Map display.

2. Determine the half row the failed RAM is located from the Memory Map display.

3. Replace the eight RAM chips in that half row, one at a time.

4. Replace the non-RAM chips D2 and E2.



USING THE APPLE /// FLOWCHART

How to use this flow chart:

1) Start with the box at the top of the EXEC page.

2) Perform the action(s) indicated in each block. It's a good idea to take notes on what tests you've done and what the results were.

3) The diamond-shaped blocks are decision points. Many of them contain a test to be made, and a description of a possible result. After doing the test, take the YES exit path if the result you got from the test matches the one given; otherwise take the NO exit path.

Some decision blocks direct your path based on the results of a previous test (usually just before the decision point). Take the YES or NO exit path based on the results of the indicated test.

4) If the system successfully does everything that it should do in the EXEC flowchart, you will be directed to go to the flowchart section appropriate to the problem that you have (**** list here ****). If the system fails, a corrective action may be indicated, or you may be directed to the NO BOOT/NO RESET flowcharts for further tests.

5) Most terminal blocks (ones with no exit) contain a list of motherboard chip locations. Replace the chips at the indicated locations one at a time. After each substitution, test the system to see if the original problem has been fixed. If it is gone, great. If it is still there, try the next chip. If you run out of chips in the list, check the inputs and enables to the listed chips. If you find any that are faulty, trace the fault back towards the source.

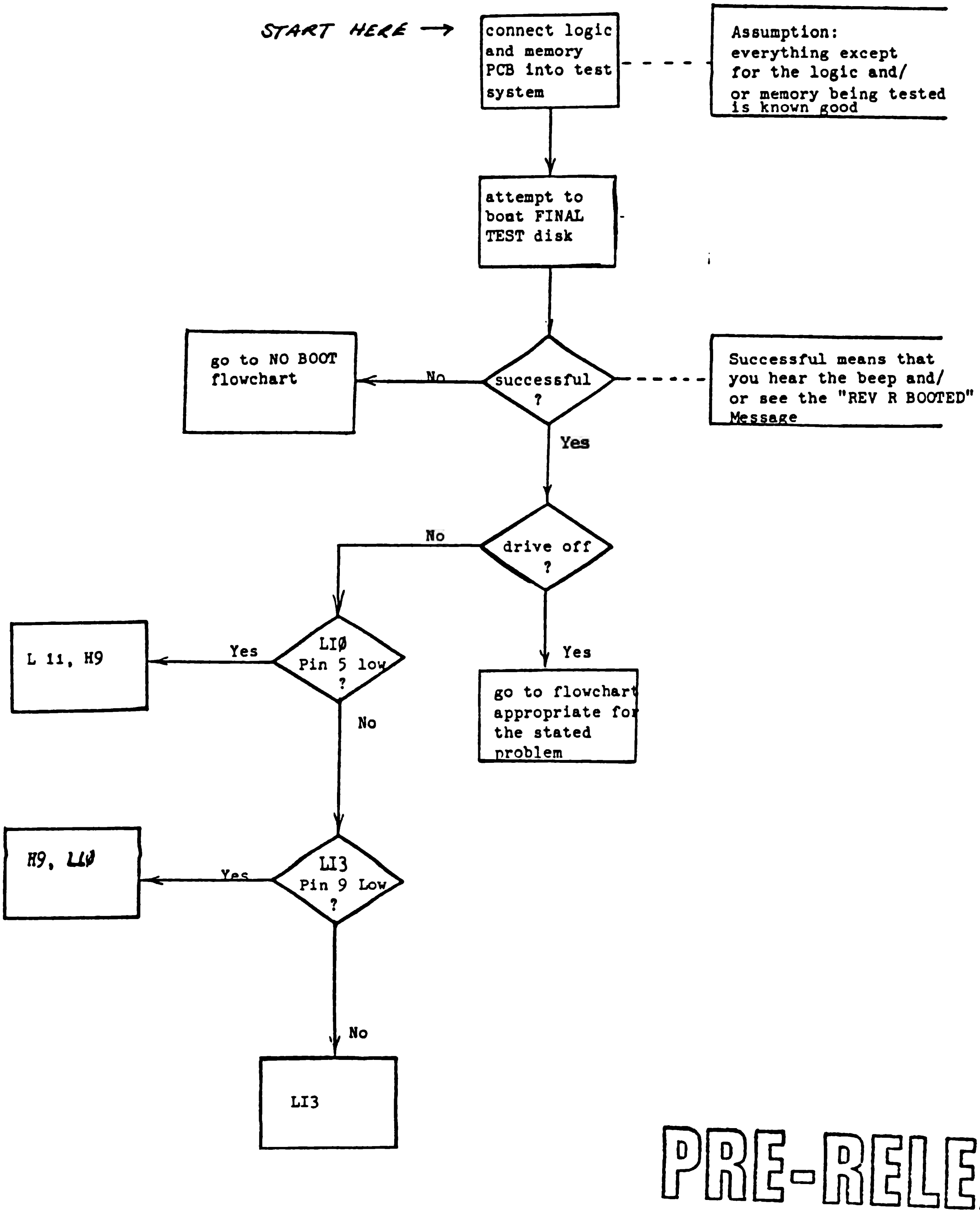
Some terminal blocks will contain instructions for corrective action. Do what it says, then test the system.

If you haven't fixed the problem, you have reached a place where the flowchart won't help you (though you should suspect the area of the circuit that it has led you to). Good luck. Once you find the problem, see if you can fix the flowchart so that it will cover that problem. Notify Service Engineering in Cupertino of any errors you find in the flowchart, and of any additions or other suggestions you want to make.

PRE-RELEASE
VERSION

Flowcharting Worksheet

PROGRAMMER	PROGRAM NO	DATE	PAGE 1 OF 1
CHART ID	CHART NAME A/// FLOWCHART	PROGRAM NAME EXEC	

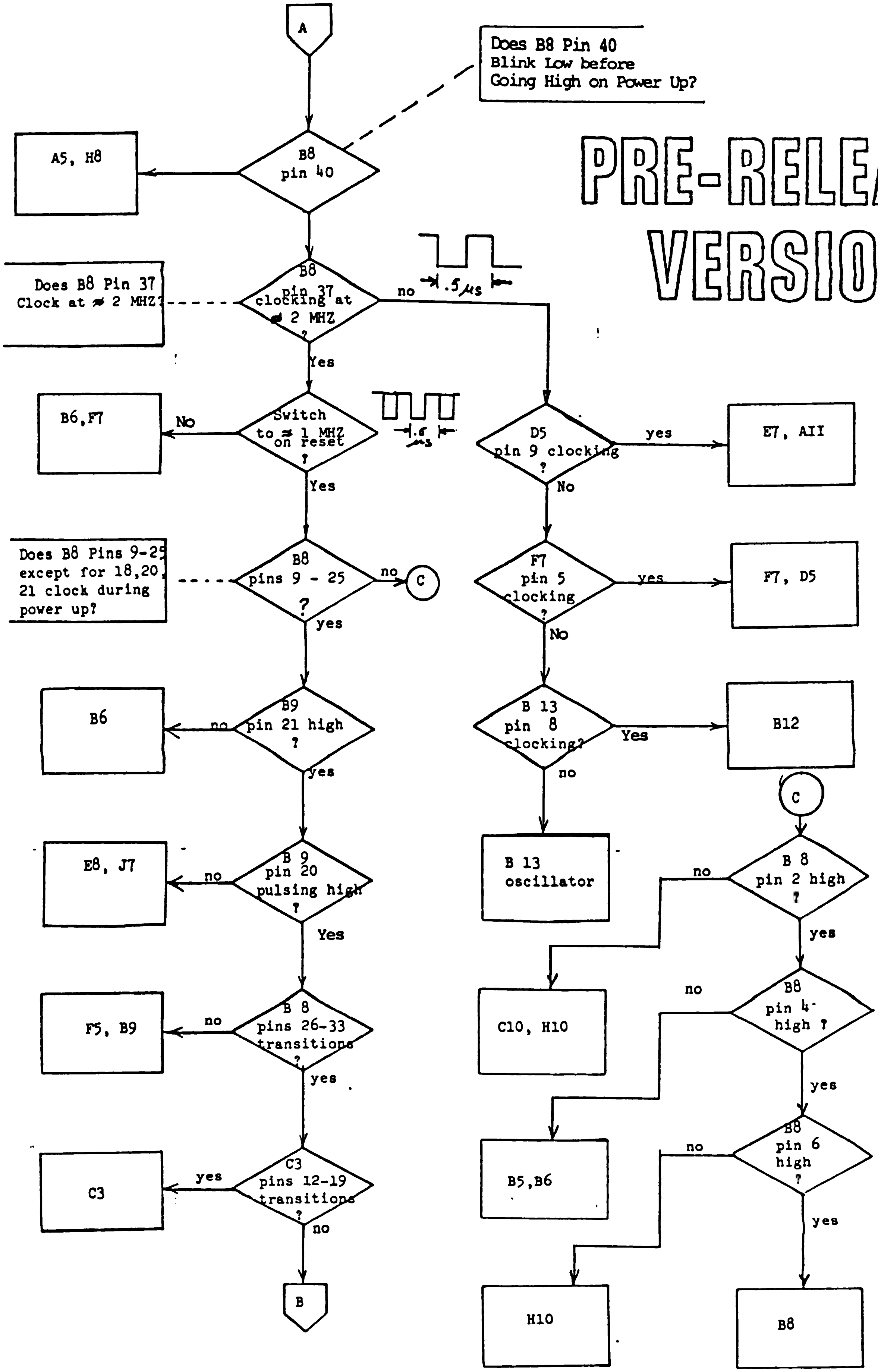

START HERE →
connect logic and memory PCB into test system
Assumption: everything except for the logic and/ or memory being tested is known good
attempt to boot FINAL TEST disk
successful ?
No
go to NO BOOT flowchart
Successful means that you hear the beep and/ or see the "REV R BOOTED" Message
Yes
drive off ?
No
Yes
go to flowchart appropriate for the stated problem
LI0 Pin 5 low ?
Yes
L 11, H9
No
LI3 Pin 9 Low ?
Yes
H9, LI0
No
LI3

PRE-RELEASE VERSION

Flowcharting Worksheet

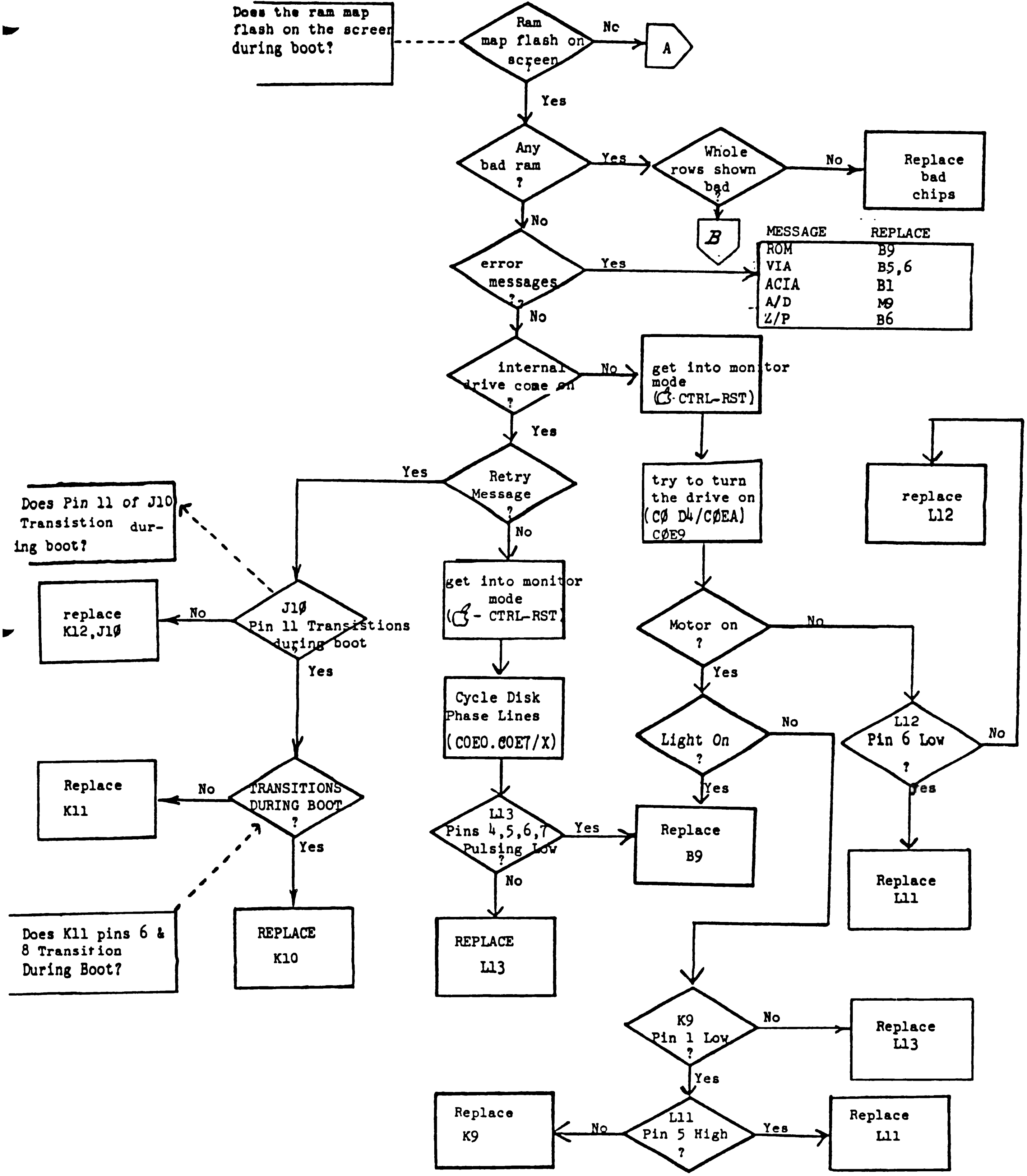
PROGRAMMER ______ PROGRAM NO ______ DATE ______ PAGE 2 OF 3
CHART ID ______ CHART NAME NO BOOT (NO RESET) ______ PROGRAM NAME ______

PRE-RELEASE VERSION



Flowcharting Worksheet

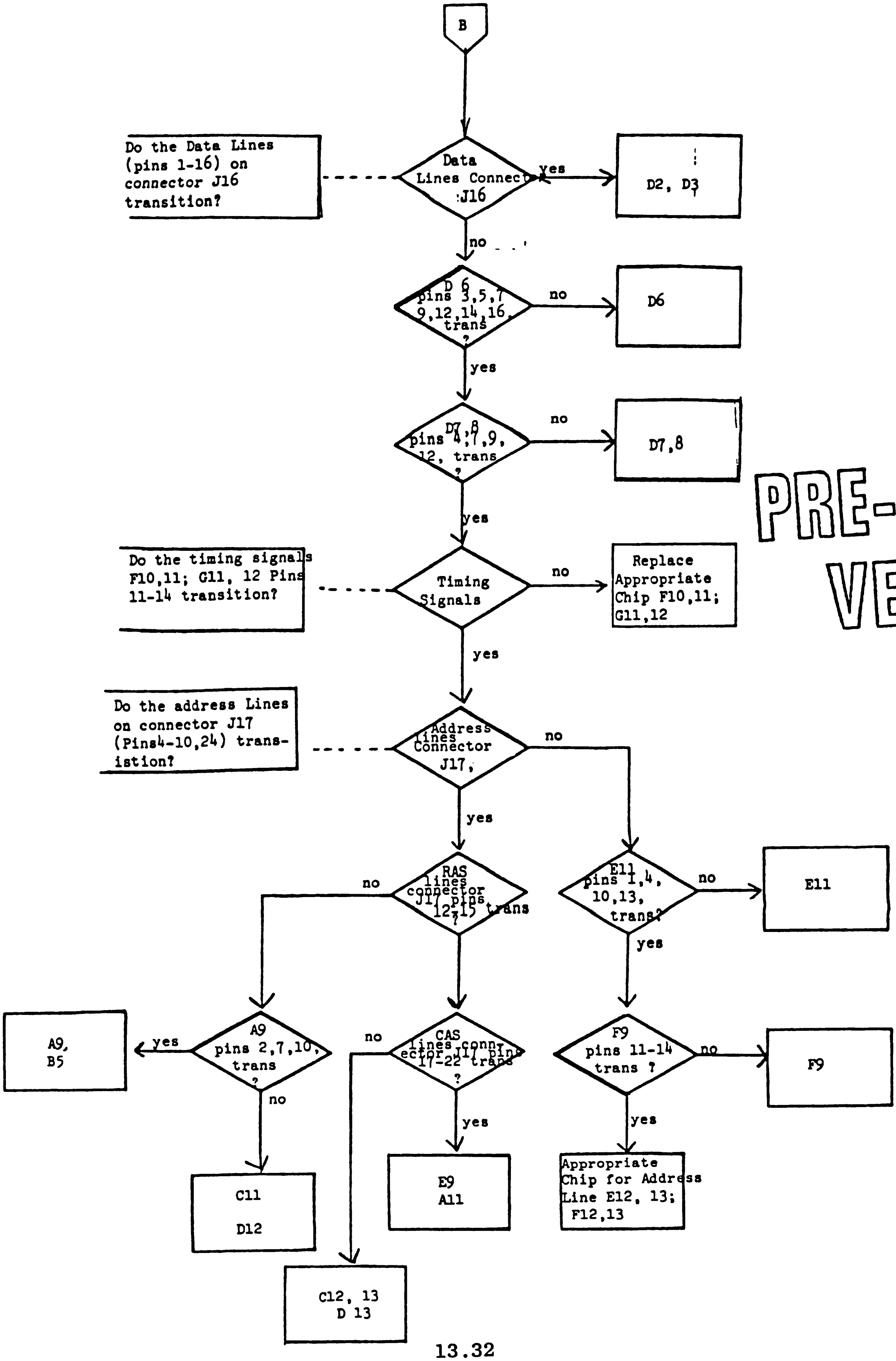
PROGRAMMER ______ PROGRAM NO ______ DATE ______ PAGE 1 OF 3
CHART ID ______ CHART NAME NO BOOT PROGRAM NAME ______



PRE-RELEASE VERSION

Flowcharting Worksheet

PROGRAMMER ______ PROGRAM NO ______ DATE ______ PAGE 3 OF 3
CHART ID ______ CHART NAME NO BOOT (MEMORY) PROGRAM NAME ______



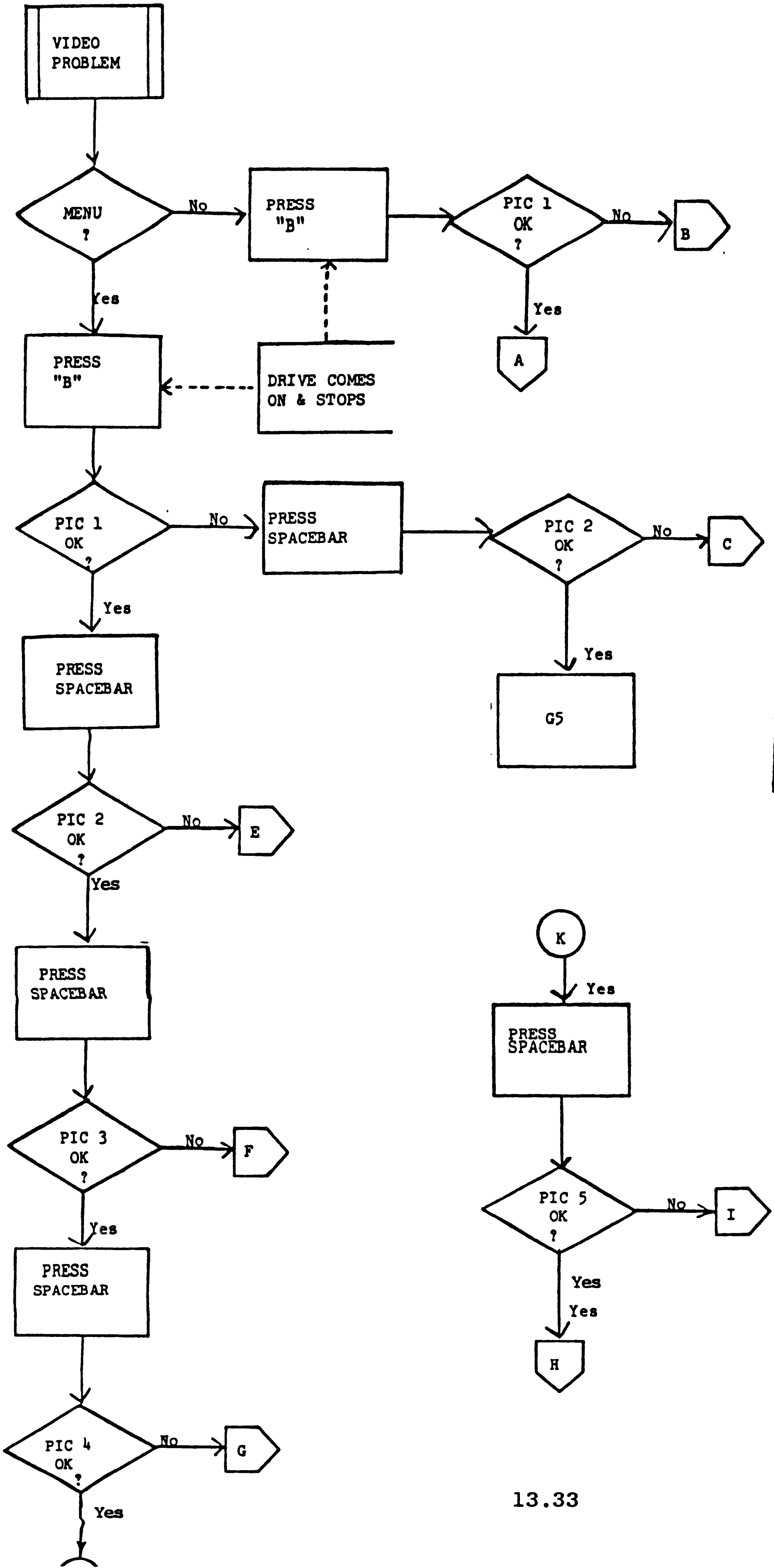
B
Do the Data Lines (pins 1-16) on connector J16 transition?
Data Lines Connector J16
yes
D2, D3
no
D 6 pins 3,5,7 9,12,14,16, trans ?
no
D6
yes
D7,8 pins 4,7,9, 12, trans ?
no
D7,8
yes
Do the timing signals F10,11; G11, 12 Pins 11-14 transition?
Timing Signals
no
Replace Appropriate Chip F10,11; G11,12
yes
Do the address Lines on connector J17 (Pins4-10,24) transistion?
Address lines Connector J17,
no
yes
RAS lines connector J17 pins 12,15 trans ?
no
E11 pins 1,4, 10,13, trans?
no
E11
yes
A9 pins 2,7,10, trans ?
yes
A9, B5
no
C11 D12
CAS lines connector J17 pins 17-22 trans ?
no
C12, 13 D 13
yes
E9 A11
F9 pins 11-14 trans ?
no
F9
yes
Appropriate Chip for Address Line E12, 13; F12,13

PRE-RELEAS
VERSION

Flowcharting Worksheet

PROGRAMMER ____________ PROGRAM NO ____________ DATE 3/10/82 PAGE 1 OF 6

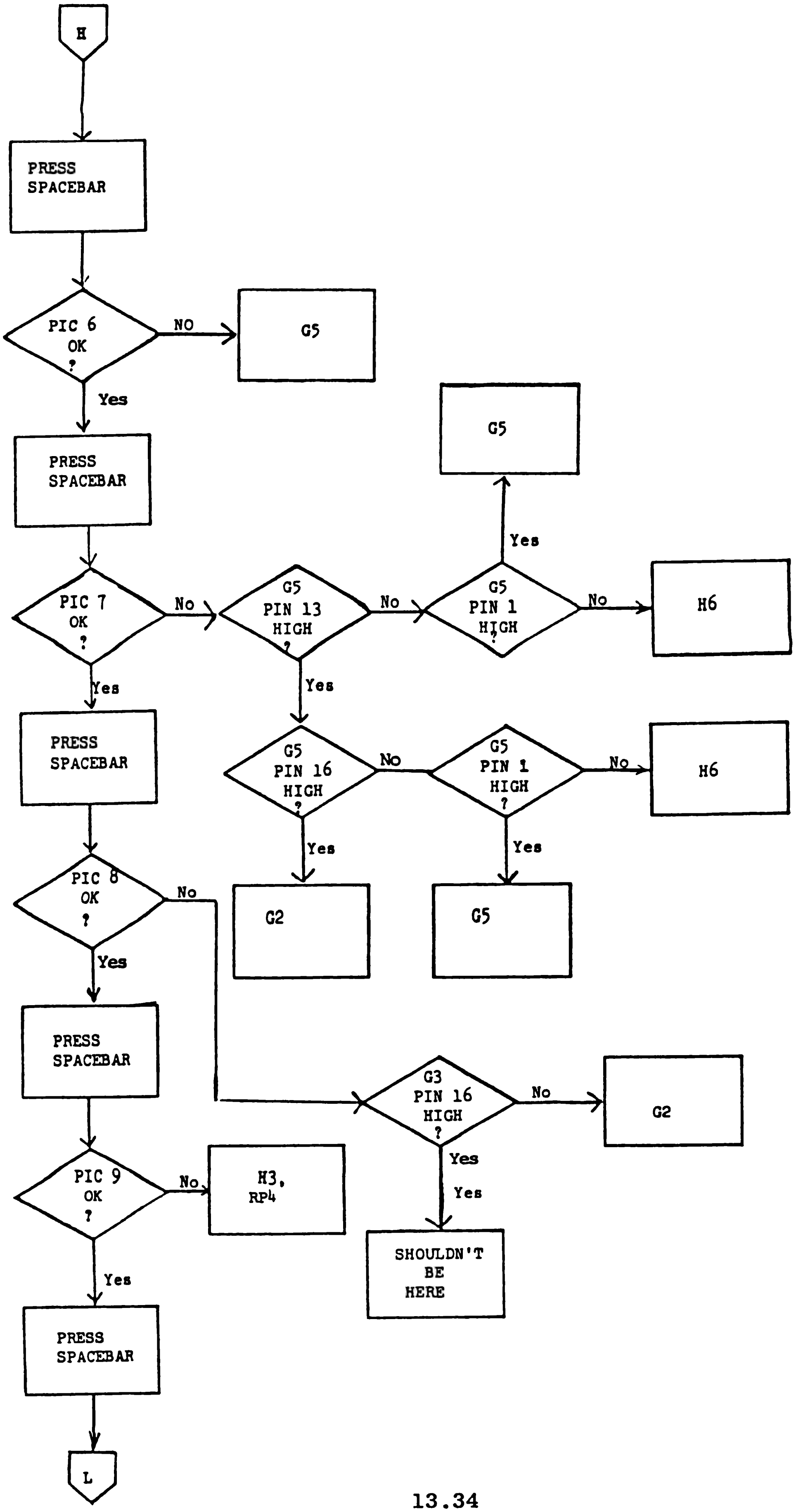
CHART ID ____________ CHART NAME VIDEO ____________ PROGRAM NAME ____________



PRE-RELEASE VERSION

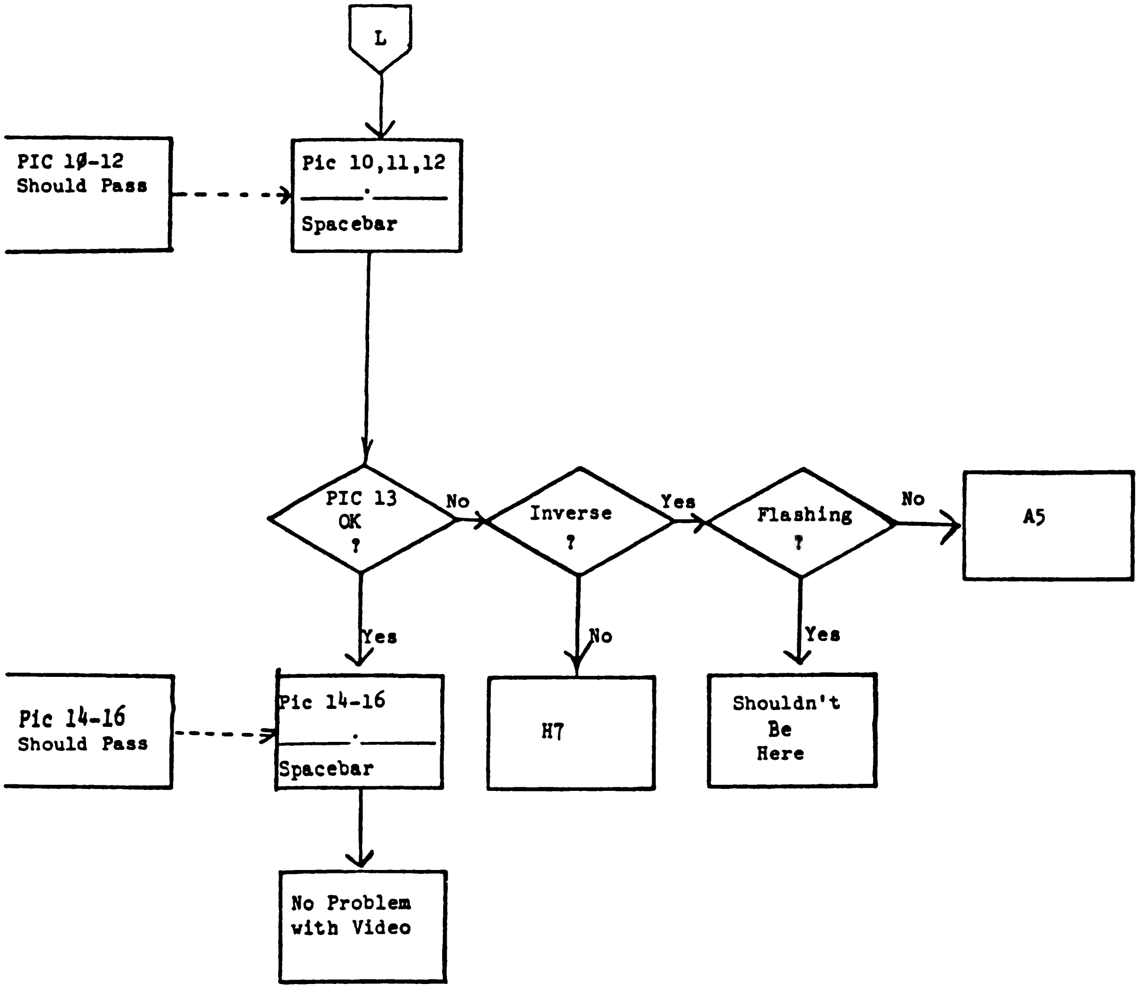
Flowcharting Worksheet

PROGRAMMER ____________ PHOGRAM NO ____________ DATE 3/10 PAGE 2 OF 6
CHART ID ____________ CHART NAME VIDEO ____________ PROGRAM NAME ____________

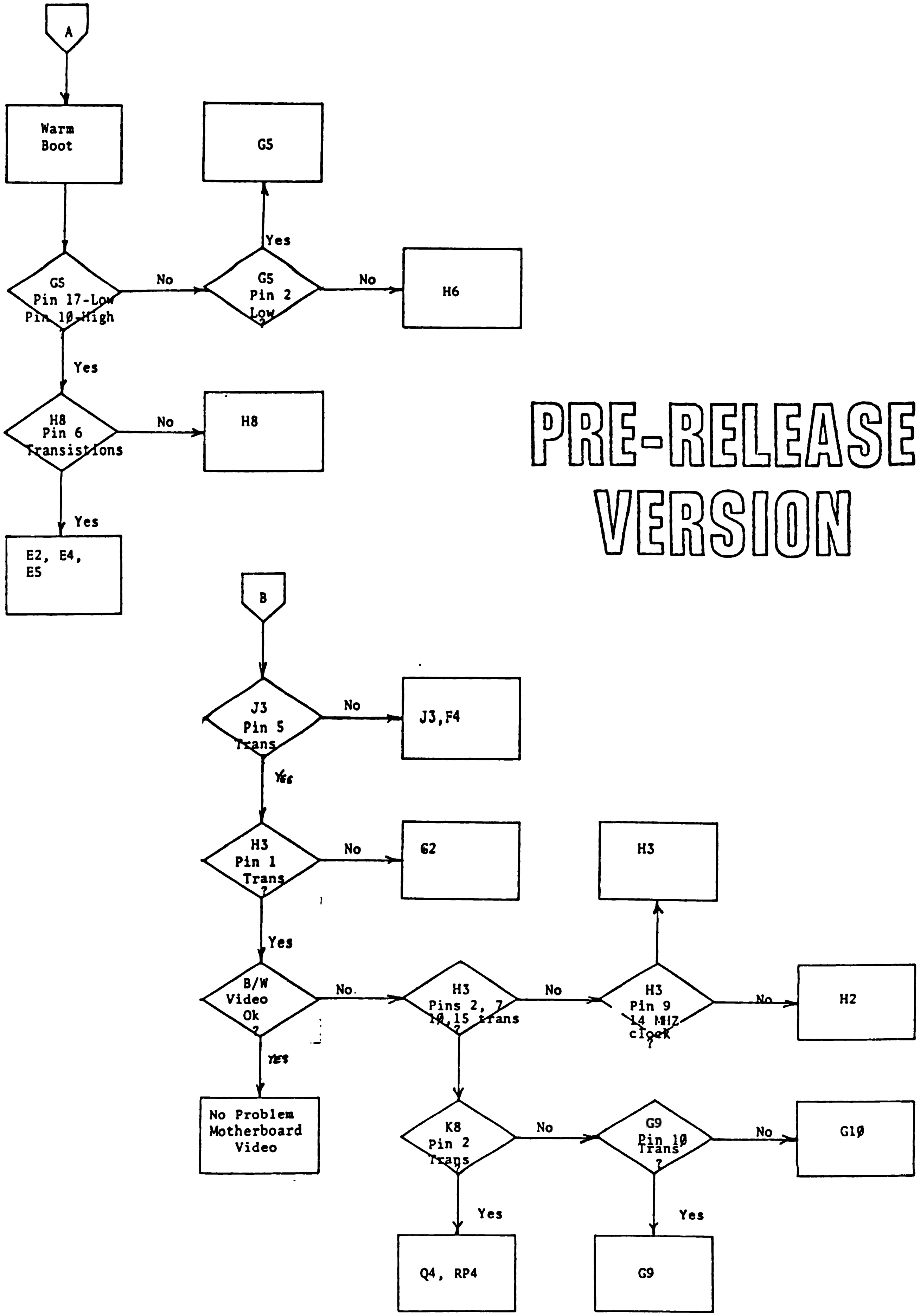


Flowcharting Worksheet

PROGRAMMER	PROGRAM NO.	DATE 3/10	PAGE 3 OF 6
CHART ID	CHART NAME VIDEO	PROGRAM NAME	



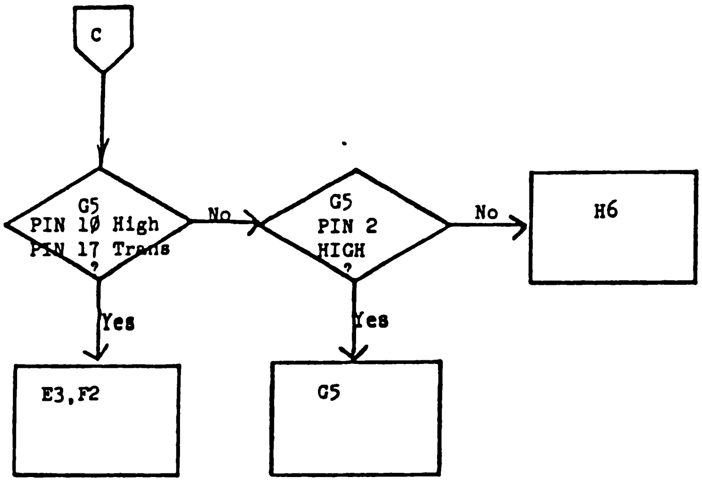
PROGRAMMER ______ PROGRAM NO ______ DATE 3/10 PAGE 4 OF 6
CHART ID ______ CHART NAME Video PROGRAM NAME ______



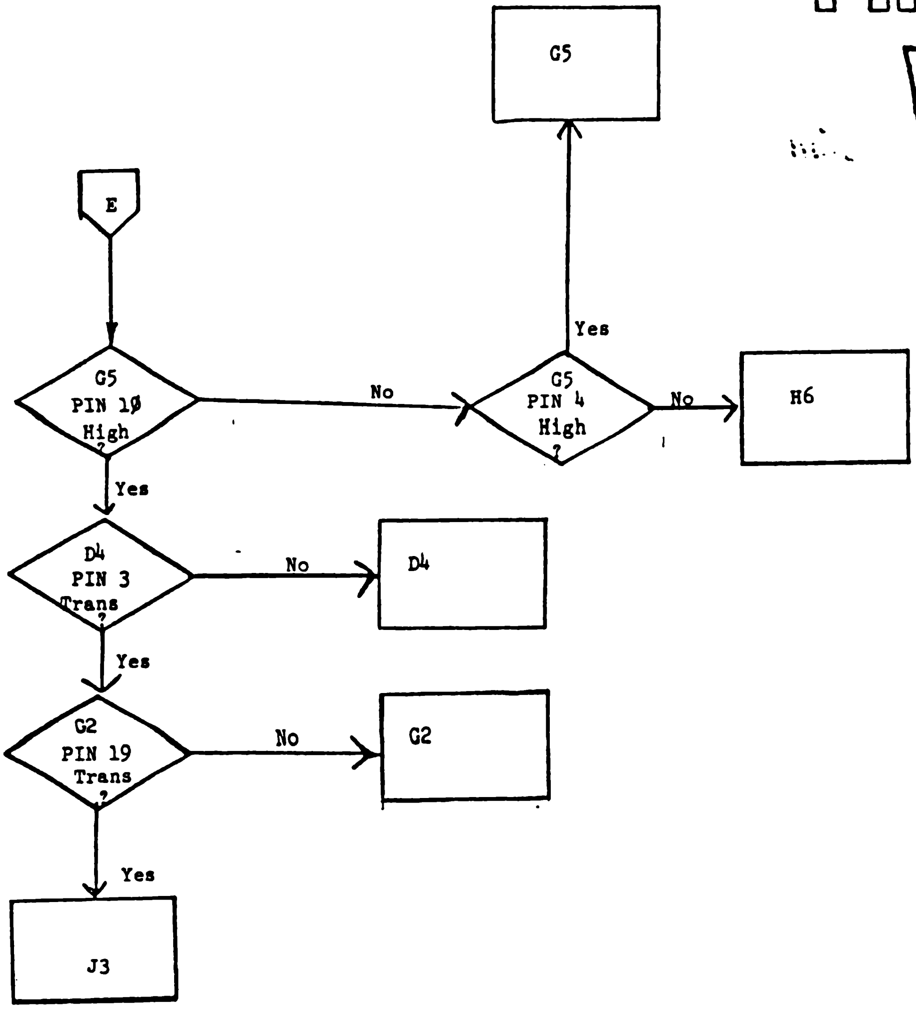
PRE-RELEASE VERSION

Flowcharting Worksheet

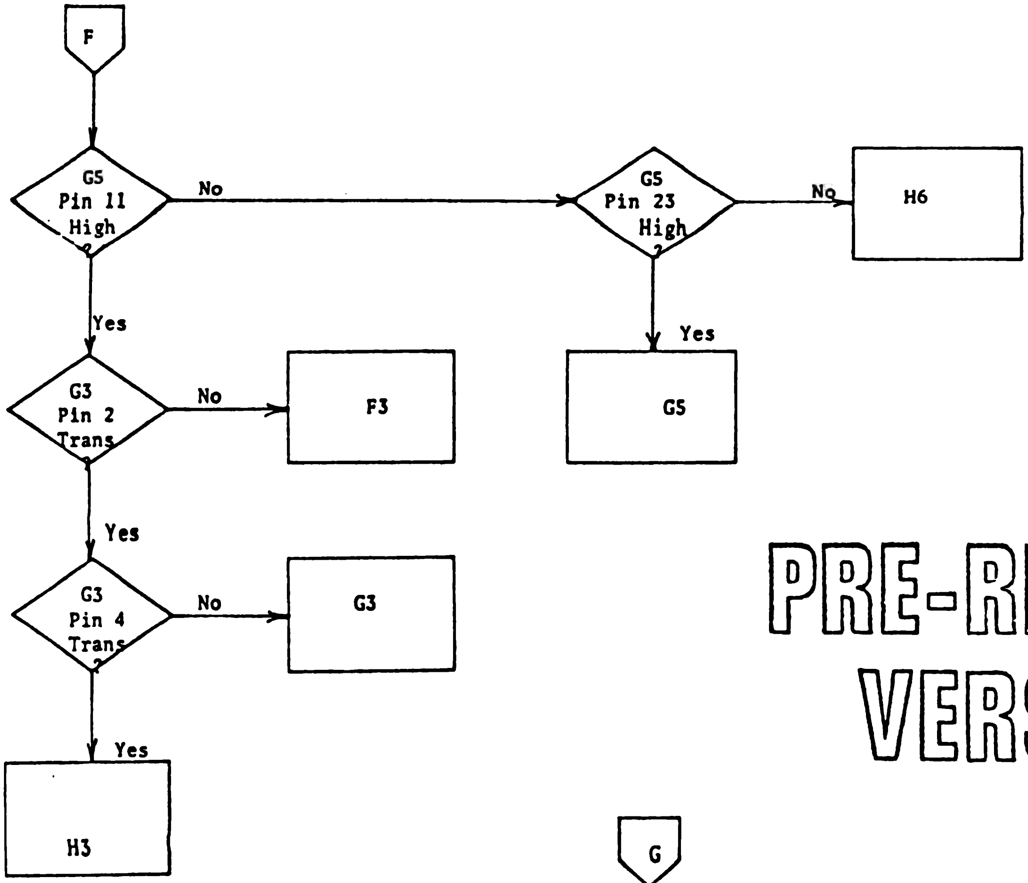
PROGRAMMER ______ PROGRAM NO. ______ DATE ______ PAGE 5 OF 6
CHART ID ______ CHART NAME VIDEO PROGRAM NAME ______



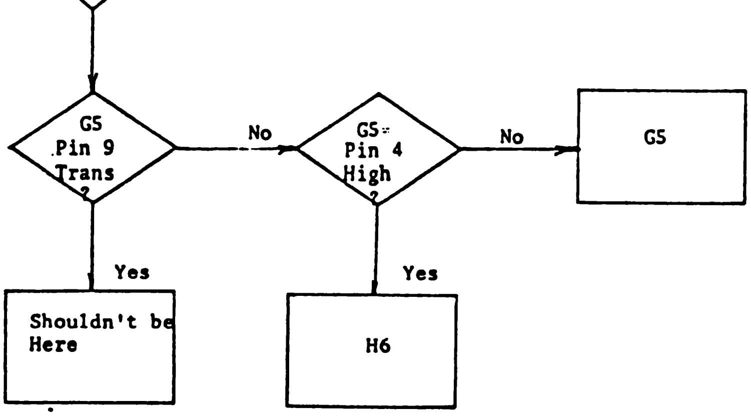
PRE-RELEASE VERSION

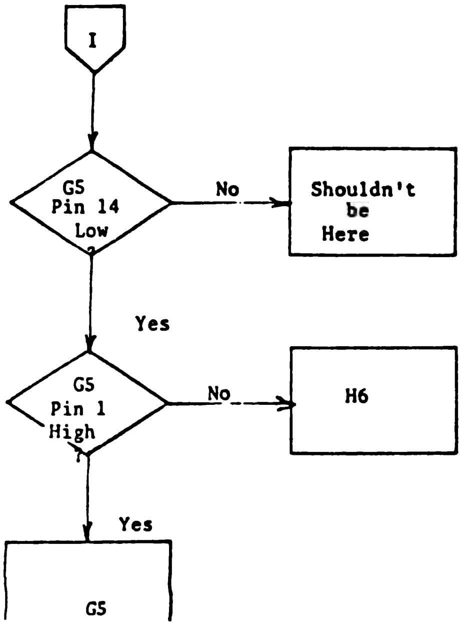


PROGRAMMER ____ PROGRAM NO ____ DATE 3/10 PAGE 6 OF 6
CHART ID ____ CHART NAME Video PROGRAM NAME ____

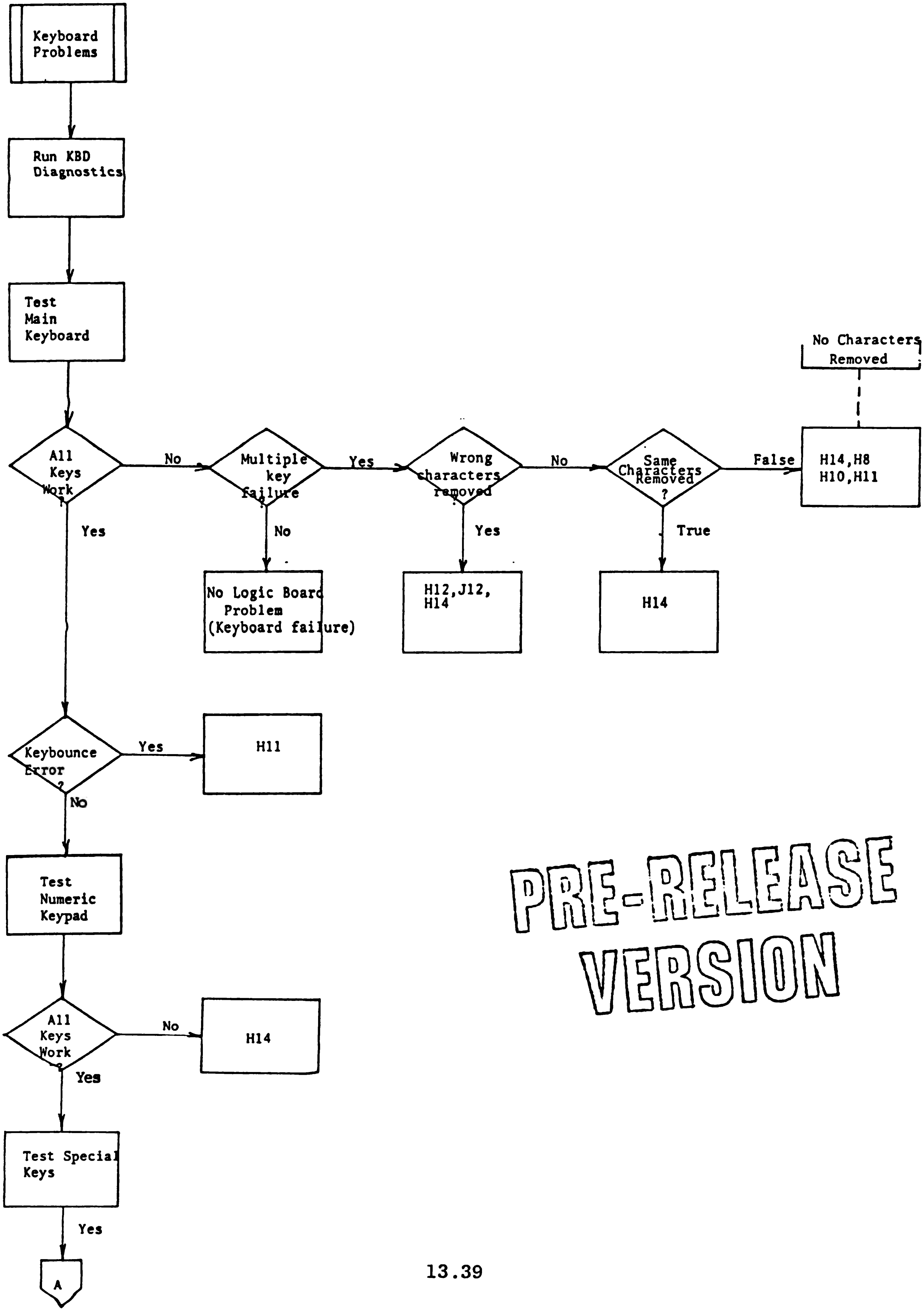


PRE-RELEASE VERSION



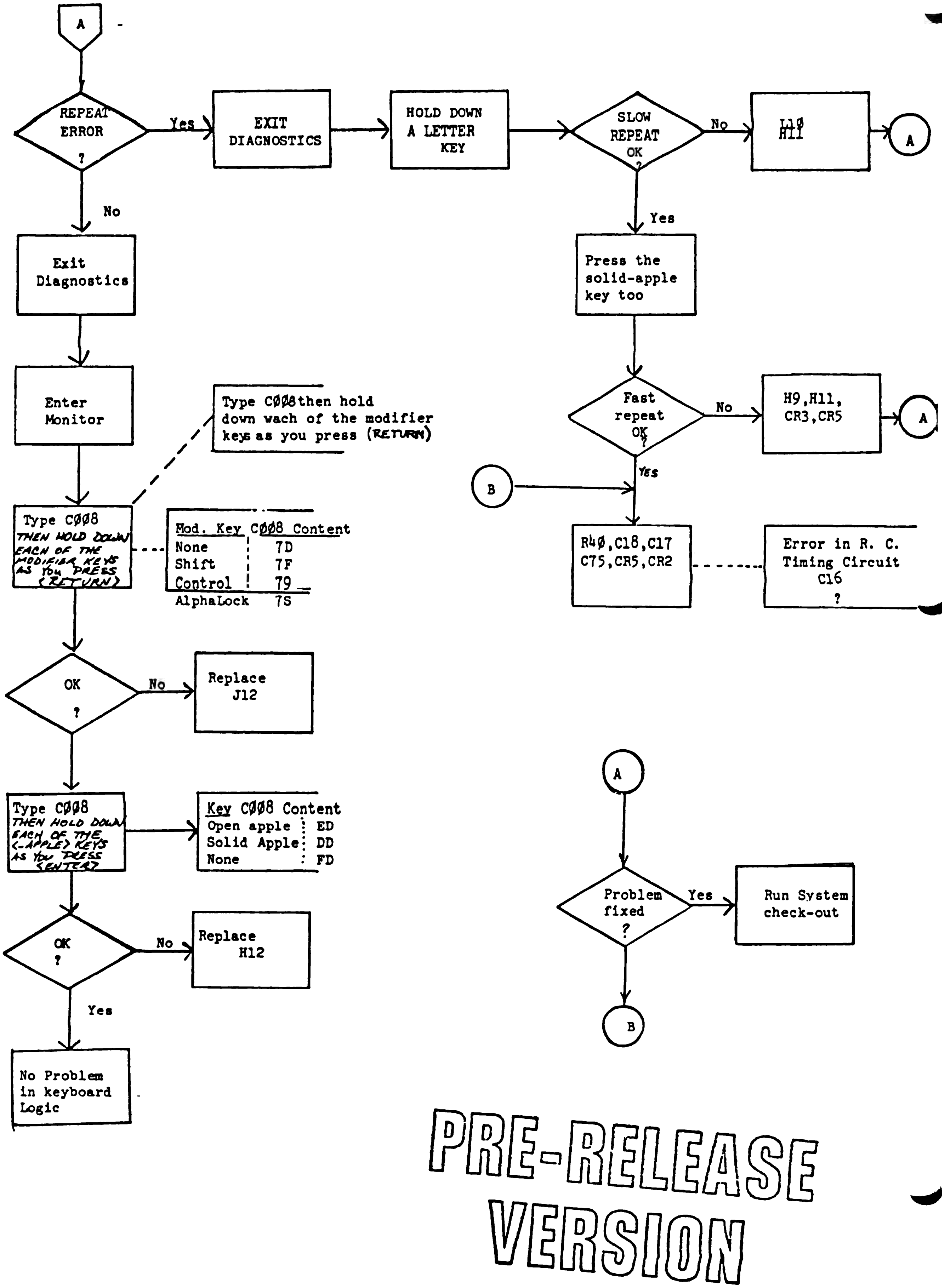


PROGRAMMER ______ PROGRAM NO. ______ DATE 3/11/82 PAGE 1 OF 2
CHART ID ______ CHART NAME Keyboard PROGRAM NAME ______



PRE-RELEASE VERSION

PROGRAMMER ______ PROGRAM NO. ______ DATE 3/14/82 PAGE 2 OF 2
CHART ID ______ CHART NAME KEYBOARD PROGRAM NAME ______


A
REPEAT ERROR ?
Yes
EXIT DIAGNOSTICS
HOLD DOWN A LETTER KEY
SLOW REPEAT OK ?
No
L10 H11
A
No
Exit Diagnostics
Yes
Press the solid-apple key too
Enter Monitor
Type C008 then hold down wach of the modifier keys as you press (RETURN)
Fast repeat OK ?
No
H9,H11, CR3,CR5
A
B
YES
Type C008 THEN HOLD DOWN EACH OF THE MODIFIER KEYS AS YOU PRESS <RETURN>
R40,C18,C17 C75,CR5,CR2
Error in R. C. Timing Circuit C16 ?
OK ?
No
Replace J12
A
Type C008 THEN HOLD DOWN EACH OF THE <-APPLE> KEYS AS YOU PRESS <ENTER>
Problem fixed ?
Yes
Run System check-out
OK ?
No
Replace H12
Yes
B
No Problem in keyboard Logic

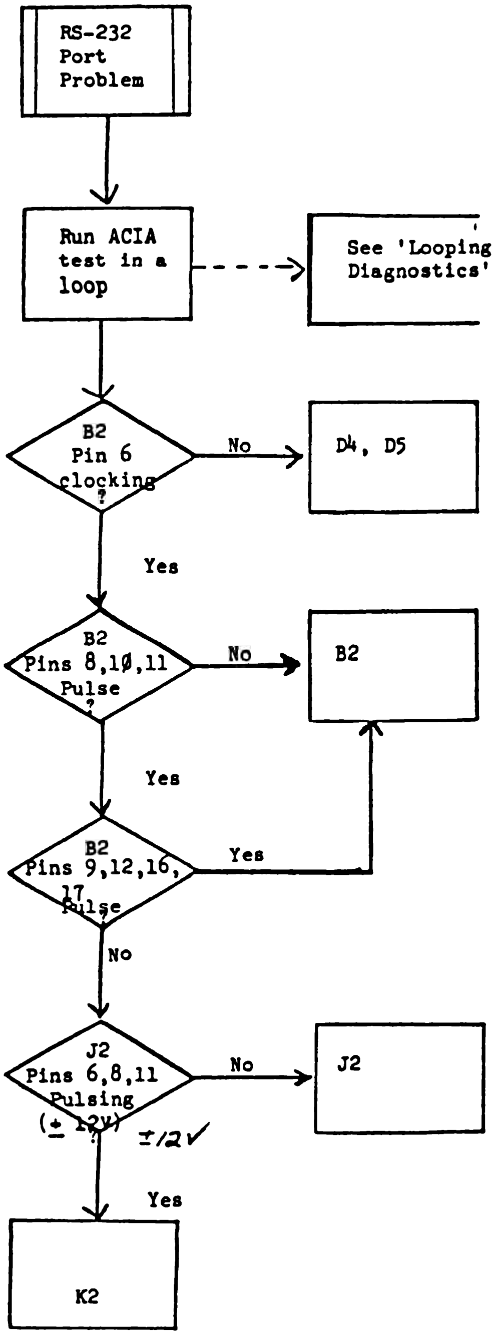
Mod. Key	C008 Content
None	7D
Shift	7F
Control	79
AlphaLock	7S

Key	C008 Content
Open apple	ED
Solid Apple	DD
None	FD

PRE-RELEASE VERSION

Flowcharting Worksheet

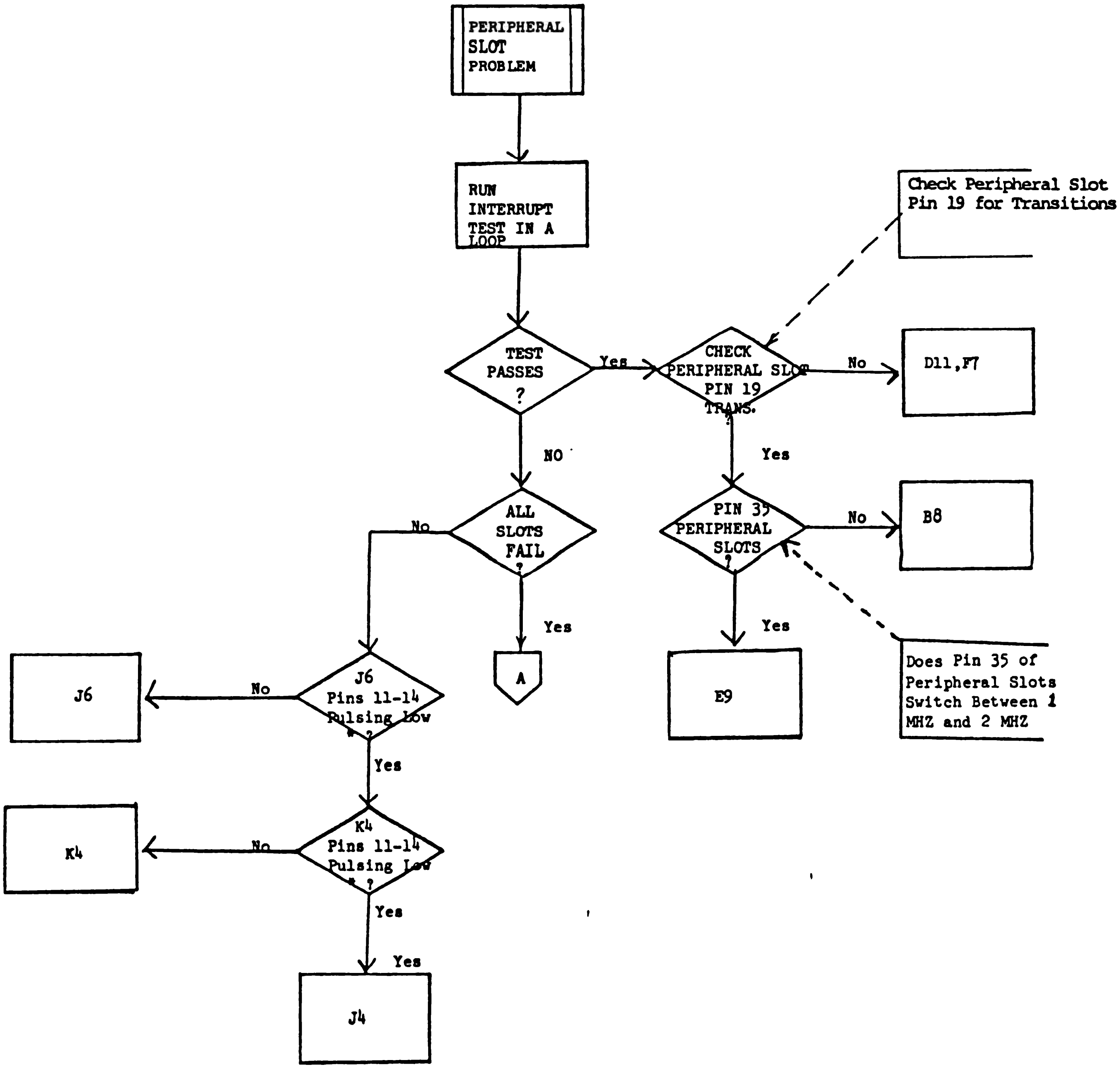
PROGRAMMER ____ PROGRAM NO ____ DATE ____ PAGE 1 OF 1
CHART ID ____ CHART NAME RS-232 PROGRAM NAME ____



PRE-RELEASE VERSION

Flowcharting Worksheet

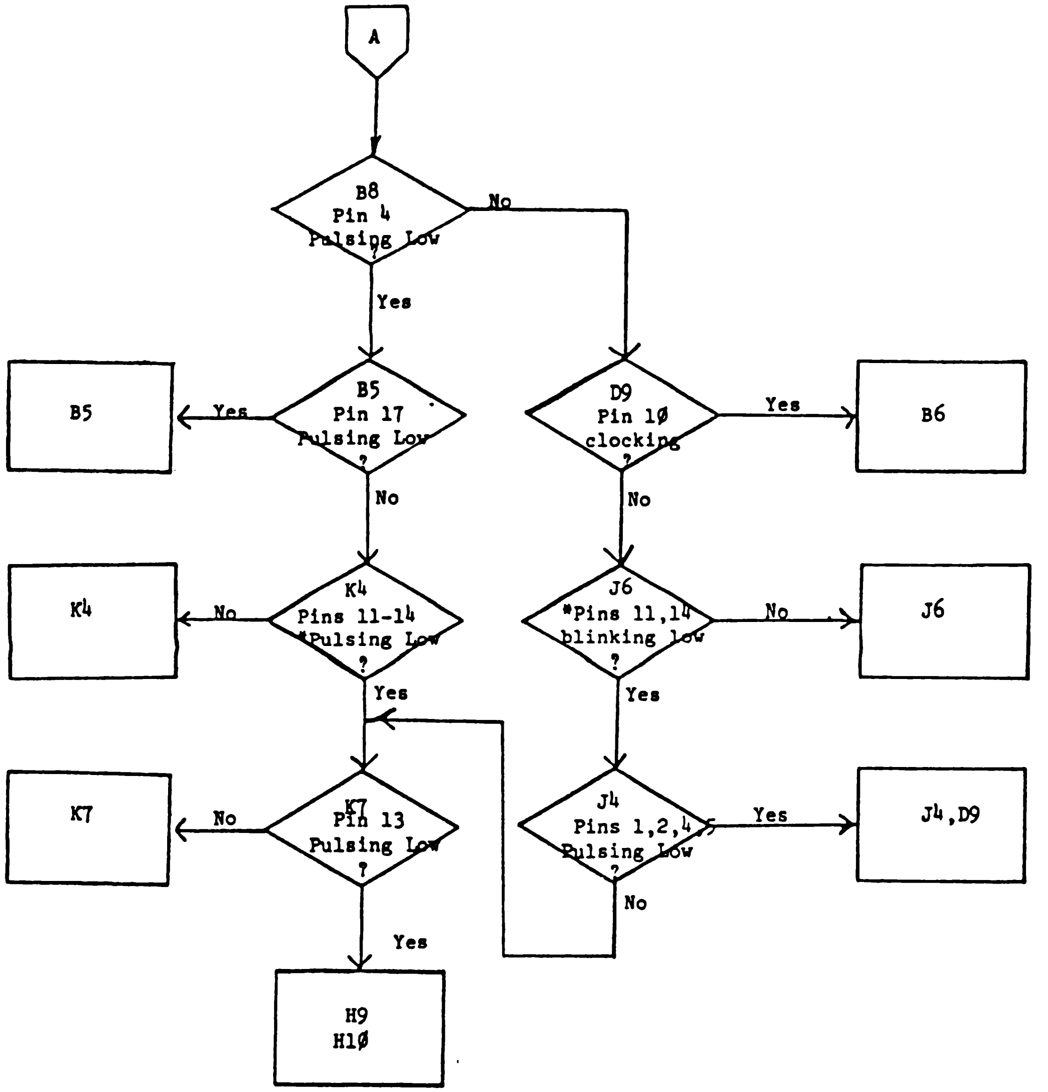
PROGRAMMER ____ PROGRAM NO. ____ DATE ____ PAGE 1 OF 2
CHART ID ____ CHART NAME PERIPHERAL SLOT PROBLEM PROGRAM NAME ____


PERIPHERAL SLOT PROBLEM
RUN INTERRUPT TEST IN A LOOP
TEST PASSES ?
Yes
NO
CHECK PERIPHERAL SLOT PIN 19 TRANS. ?
No
D11,F7
Check Peripheral Slot Pin 19 for Transitions
Yes
PIN 35 PERIPHERAL SLOTS ?
No
B8
Yes
E9
Does Pin 35 of Peripheral Slots Switch Between 1 MHZ and 2 MHZ
ALL SLOTS FAIL ?
No
Yes
A
J6 Pins 11-14 Pulsing Low * ?
No
J6
Yes
K4 Pins 11-14 Pulsing Low * ?
No
K4
Yes
Yes
J4

*K4 and J6 Pins 11-14 are very hard to see. If they trigger the scope, they're probably okay.

PRE-RELEASE VERSION

PROGRAMMER ____ PROGRAM NO. ____ DATE ____ PAGE 2 OF 2
CHART ID ____ CHART NAME PERIPHERAL SLOT PROBLEM PROGRAM NAME ____

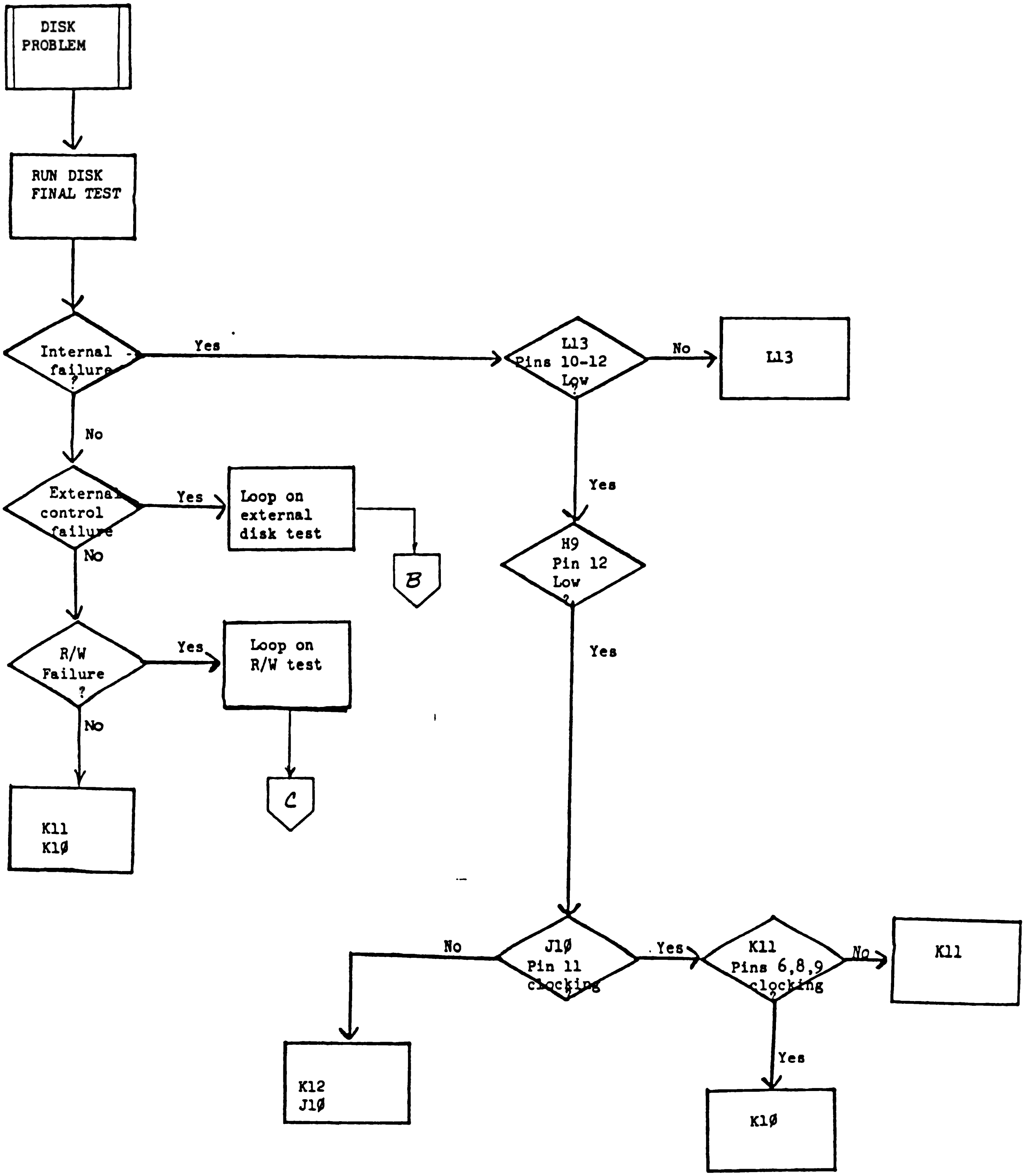


*K4 and J6 pins 11-14 are very hard to see. If they trigger the scope, they're probably okay.

PRE-RELEASE VERSION

Flowcharting Worksheet

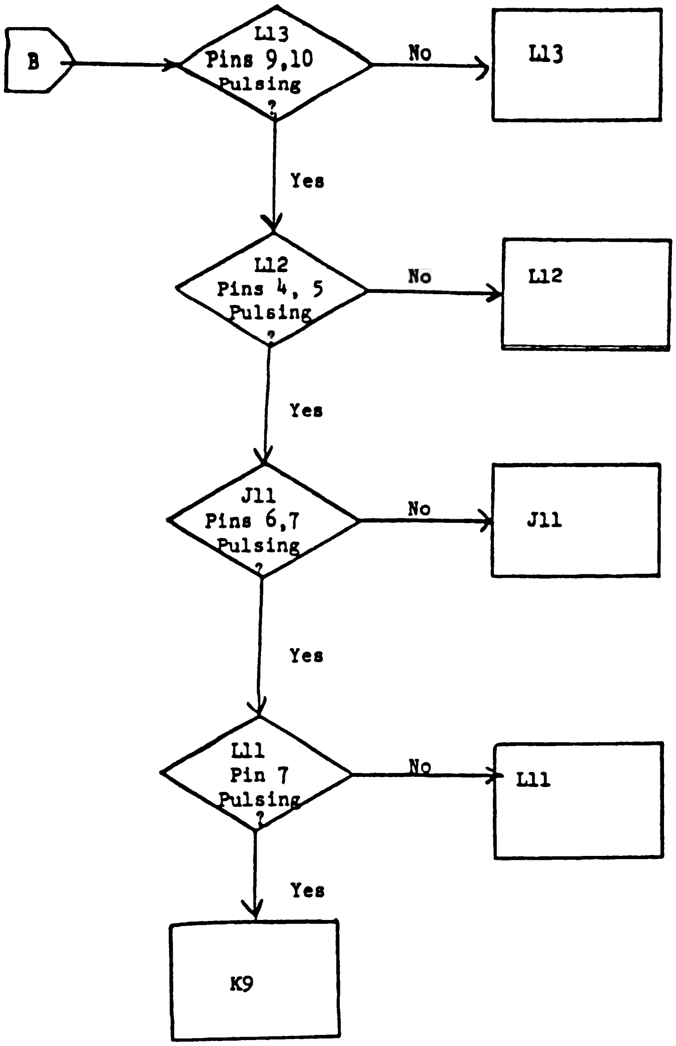
PROGRAMMER ______ PROGRAM NO ______ DATE 3/15 PAGE 1 OF 3
CHART ID ______ CHART NAME DISK PROGRAM NAME ______



PRE-RELEASE VERSION

Flowcharting Worksheet

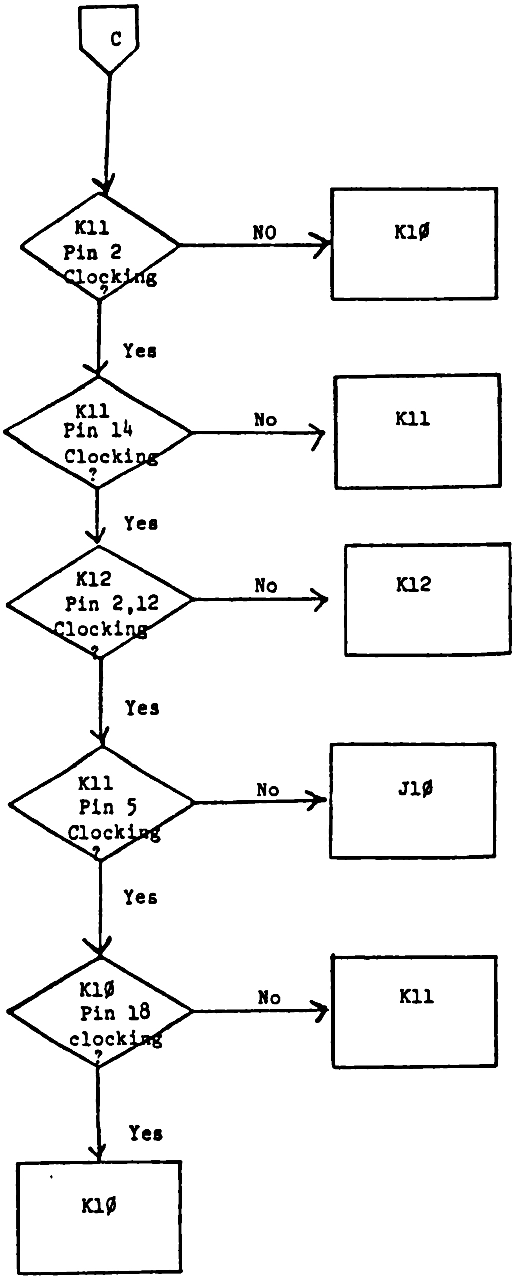
PROGRAMMER ______ PROGRAM NO. ______ DATE 3/15 PAGE 2 OF 3
CHART ID ______ CHART NAME DISK ______ PROGRAM NAME ______



PRE-RELEASE
VERSION

Flowcharting Worksheet

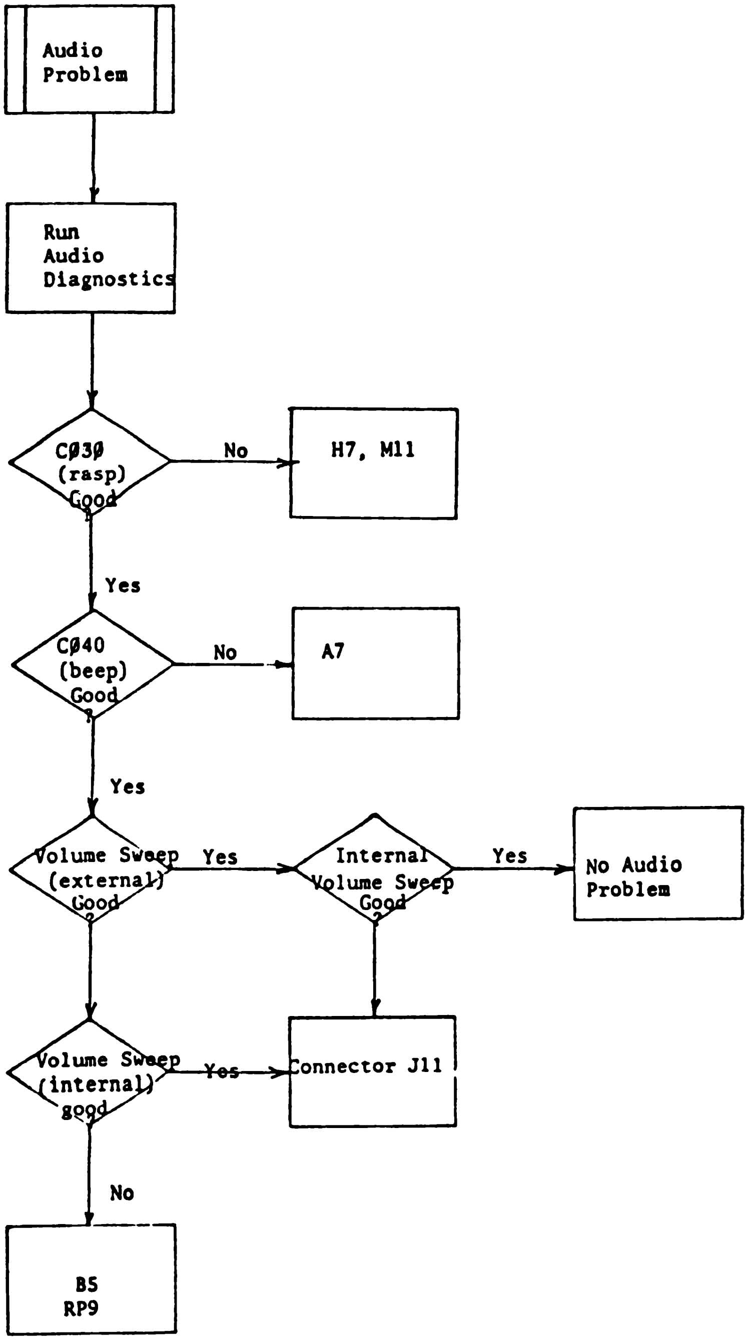
PROGRAMMER ____ PROGRAM NO. ____ DATE ____ PAGE 3 OF 3
CHART ID ____ CHART NAME DISK ____ PROGRAM NAME ____



PRE-RELEASE VERSION

Flowcharting Worksheet

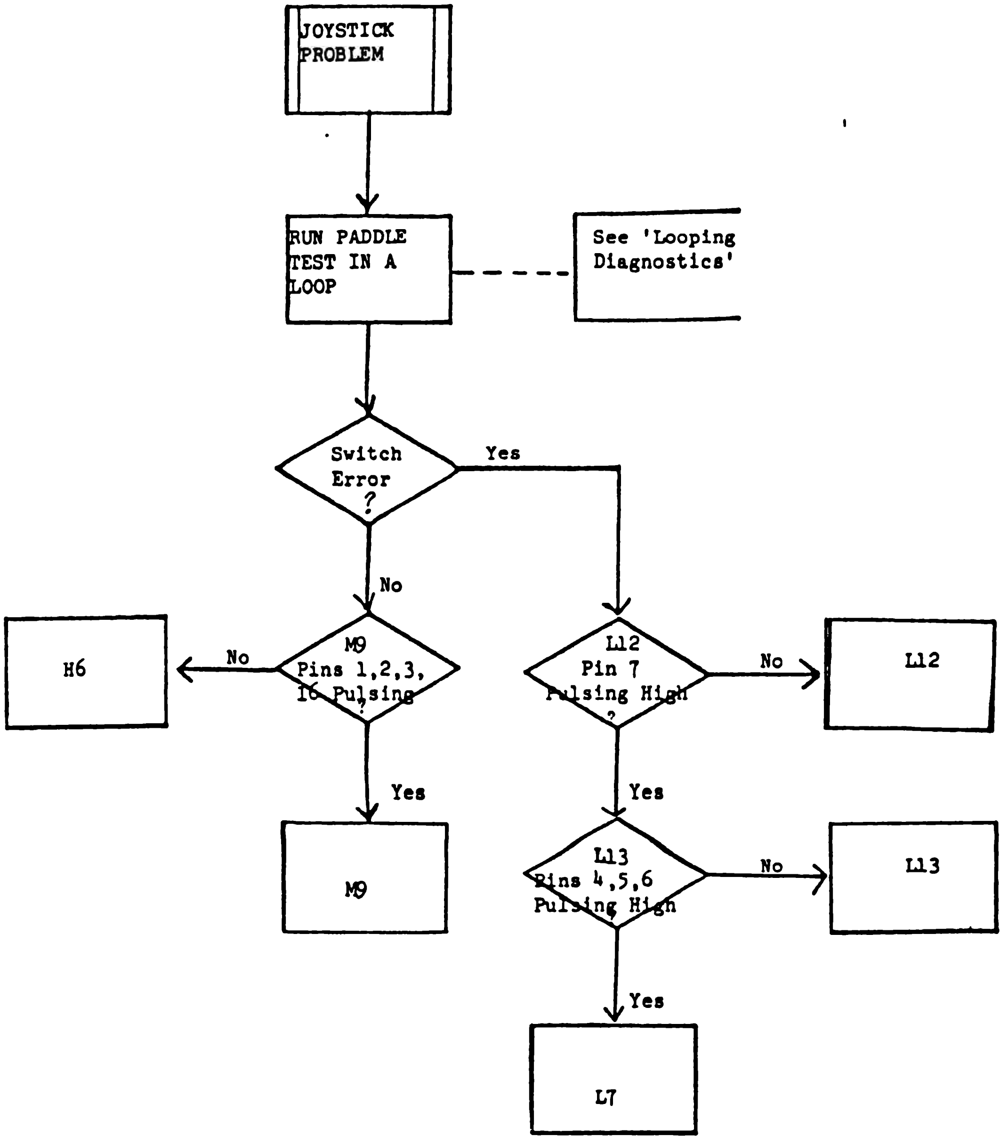
PROGRAMMER ______ PROGRAM NO. ______ DATE ______ PAGE 1 OF 1
CHART ID ______ CHART NAME SOUND ______ PROGRAM NAME ______



PRE-RELEASE VERSION

Flowcharting Worksheet

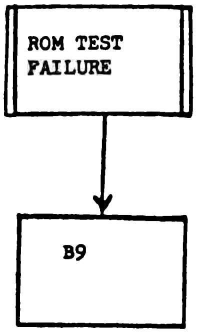
PROGRAMMER ______ PROGRAM NO ______ DATE ______ PAGE 1 OF 1
CHART ID ______ CHART NAME JOYSTICK PROGRAM NAME ______


JOYSTICK PROBLEM
RUN PADDLE TEST IN A LOOP
See 'Looping Diagnostics'
Switch Error ?
Yes
No
M9 Pins 1,2,3, 16 Pulsing ?
No
H6
Yes
M9
L12 Pin 7 Pulsing High ?
No
L12
Yes
L13 Pins 4,5,6 Pulsing High ?
No
L13
Yes
L7

PRE-RELEASE VERSION

Flowcharting Worksheet

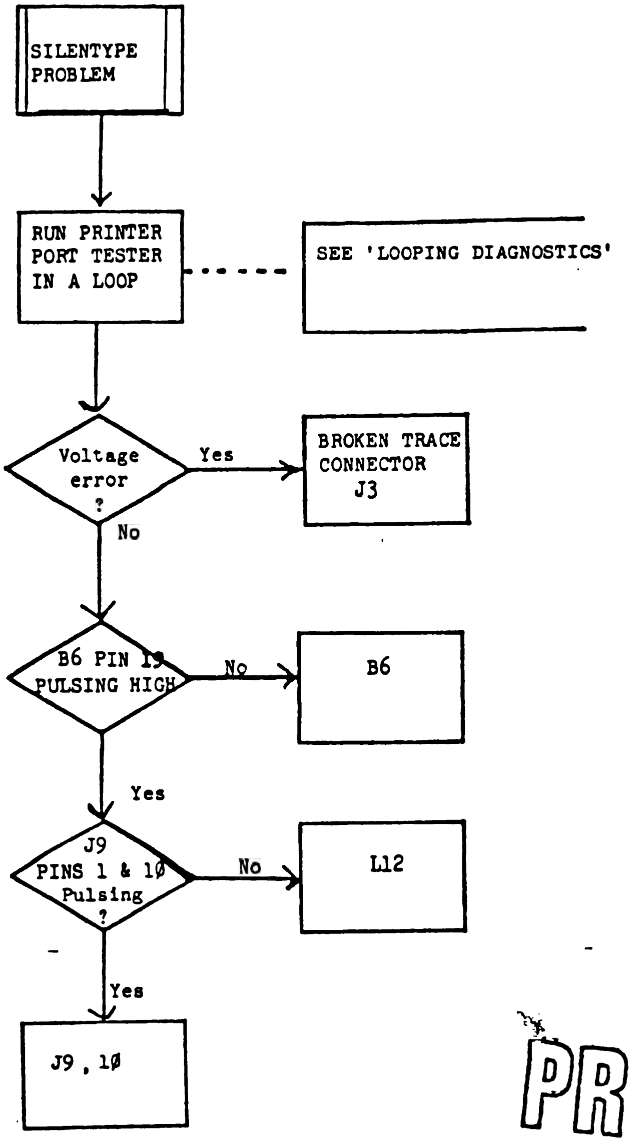
PROGRAMMER ____ PROGRAM NO ____ DATE ____ PAGE 1 OF 1
CHART ID ____ CHART NAME ROM PROGRAM NAME ____



PRE-RELEASE
VERSION

Flowcharting Worksheet

PROGRAMMER ______ PROGRAM NO. ______ DATE ______ PAGE 1 OF 1
CHART ID ______ CHART NAME silentype PROGRAM NAME ______



PRE-RELEASE VERSION

FAULT ISOLATION - TIPS AND HINTS

The following pieces of information are by no means an absolute guarantee of success in isolating a failure mode. This is intended only as a GUIDE or AID to assist you in finding a logical and likely place to begin your troubleshooting of the particular failure mode.

F6E6 TEST (12V MAIN LOGICS)

RAM indicates a memory failure. Use the chart included below to determine which chip on the moemory board is failing. Other possibilities are the memory board connectors. If is is an addressing problem, check J17, (the connector on the right) and if it is a data problem, check J16, (the connector on the left).

RAM FAILURE CHART 128K SYSTEM DISPLAY

DIAGNOSTIC RAM

```
........
........
........
........
........
........
........
........
```

A 1 showing any place that a dot is shown here indicates a failure. The position of the one shows which chip has failed. The chart below shows the chip location on the memory board.

B9	B8	B7	B6	B5	B4	B3	B2
B17	B16	B15	B14	B13	B12	B11	B10
B9	B8	B7	B6	B5	B4	B3	B2
B17	B16	B15	C14	B13	B12	B11	B10
C17	C16	C15	C14	C13	C12	C11	C10
D9	D8	D7	D6	D5	D4	D3	D2
D17	D16	D15	D14	D13	D12	D11	D10
C9	C8	C7	C6	C5	C4	C3	C2

ROM indicates that the ROM failed. Check the ROM at B9 (341-0031-01). Usually the ROM itsely is bad when this message appears.

VIA indicates that a register in one of the 6522's has failed. These two parts are the 40-pin IC's at location B6 and B5.

ACIA indicates that the 6551 located at B1 has failed. A/D ia an indicator of a bad read of either the high or lw reference voltage of the 9708 chip located at M9.

ZP indicates a zero page register failure. The zero page register is port B of the 6522 located at B6. Other possible chips for this failure are the S257s at locations D7 and D8 or the Ls132 at D4. This is where the zero page portion of the address gets fed to the system memory. Also note the NOT ZPAGE signal which should originate at the LS51 at B11.

RETRY is a message the system gives when it is unable to "boot" the disk that is (or should be) in the internal disk drive.

OTHER FAILURE MODES:

These are usually idetified when running the normal system test diskette.

NO RESET is probably the most difficult porblem to fix and the easiest to identify. It's main symptom is that when power is truned on, absoultely NOTHING happens. The disk does not even ATTEMPT to boot and there are no beeps. Keep in mind that SIGNATURE ANALYSIS is a very good way to find a NO RESET problem. Below are some of the things that you can check fairly quickly:

Is the keyboard light lit and is the LED on the PC boared lit. It not make sure all power is available. +5VDC, -5VDC, +12VDC, & -12VDC.

Make sure that +5VDC and ground is available at each row. (Especially rows B, D, F, & G).

Check the levels at the RESET, NMI, IRQ, and RDY pins of the CPU at B7.

Swap the ROM (B9) with a known good ROM. If there is no difference replace the original.

Swap the CPU (B7) with a known good CPU. If there is no difference replace the original.

NOTE: These last two items are the most common reasons for NO RESET.

Power OFF and check for shorts on the Address or Data Bus.

Make sure that all clocks are runing. Phase 0, PRE1M, 14M, 3.5M, and 7M.

Other devices that are frequently causes of NO RESET are listed below:

LOCATION	DEVICE	COMMENTS
Row F & C	7643	high failure items
Row B	6522	B6 is more likely
C3	8304	high failure items
Row E & F	74S153	high failure items
A5	NE556	and supporting circuitry
D13	74S374	high failure items
D6	74LS244	high failure items
D3 & D7	74S257	Not very often
K9	74LS04	not very often
D9	74LS02	moderate failure item
D11	74S74	Make sure its not LS

G7 & J7	74LS133	high failure items
G8	74LS139	high failure items
H8	74LS04	high failure item
J8	74LS32	moderate failure item

For a RAM addressing problem check the memory board connector on the right side, (J17), and for a RAM data problem check the memory board connector on the left, (J16). NOTE: A RAM data problem will USUALLY run the F6E6 test.

Miscellaneous reset problems have been caused by the following:
diode CR4 ....reversed, open or missing
RP19 (S19)............3.3K shorted
Xtal..................not oscillating
reset key.............bad
power or ground.......missing due to open pin/trace

It may also help you to know that there is an 85% chance of the problem being found on sheets 2 and 3 of the Apple /// schematic, and a 13% chance of being found on sheets 9 and 4. Good luck on the other 2%.

NO BOOT is recognized by the fact that the system actualy ATTEMPTING to boot even though it doesn't succeed. Video may or may not be present. You may see the RETRY message, and the disk may run itself off, or it may stay on. Some of the more common things to check are:

The 9334's at L12 and L13.
The 74LS04 at K9.
The mostly likely choices are:

device	location
74LS323	K10
74S471	K11 (P6A prom)
74LS174	K12

Concentrate your troubleshooting efforts on sheet 6 of the Apple /// schematic, unless you find a problem with the NOT devsel-6, or the NOT Q3 signals. Any other problem external to sheet 6 would most likely also show up in a RAM test, or video test.

VIDEO problems can be very simple at times and downright troublesome at other times. Some of the mose common failures are:

By far, the most likely candidates, are the 74LS374's, located at E2, E3, F2, F3, G2, & G10. These IC's are the cause of >70% of the video problems.

It is also a good idea to check the two 2114's located at E4 and E5.

The next most frequent failure is the 74LS153 at L8. This is U90 as shown on sheet 5 of the schematic.

Video problems are also very likely to be misdiagnosed timing problems. For these check the 64S195 at D10 and the 74LS374 at D11.

If the video horizontal or vertical sync appears to be messed up, check the 74LS161's located at F10, F11, G11, and G12.

If none of the above items point you toward the real problem, begin your troubleshooting on sheet 5 of the schematic where 80% of the problems occur, and if necessary, go on to sheet 9, where most of the remaining video problems will be found.

Keep in mind that an off-frequently crystal can kill the color or produce bad color.

INTERRUPT problems almost always end up being one of the VIA's (or 6522's). However, there have been a few other reasons for interrupt failures as described below:
I/O NMI is a symptom for sheet 8 of the schematic. Check the 74LS132 at H10 and the 74LS139 at J11.
IRQ signal missing can be caused by the 74LS21 at J4.
Sometimes the problem is noit actually an interrupt problem but the systems inability to communicate with the interrupt test cards. In the case of a missing IO SELECT, check the 74LS138 at J6, and in the case of a missing DEVICE SELECT, check the 74LS138 at K4.
Remember to check the connectors at the slots for continuity to the 74LS138's mentioned above.
Lastly, here's what happens during the INTERRUPT test:

Step 1 Disable all interrupts, mask NMI, enable I.O space, reset ACIA, re set all four slots, and set up the 6522's as they are normally used.
Step 2 Check both 6522 int enable register bits 0-6 to see if they can be set and cleared.
Step 3 Vertify that IRQ and IONMI are clear as they should be.
Step 4 Clear both 6522 interrupt flag registers and vertify that they are indeed clear.
Step 5 Check the 6522 interrupt flags to see if they can be set and cleared when enabled and vertify that they cannot be set when disabled.
Step 6 Repeat once for each slot.
  a. Set slot IRQ by using IO SELECT and vertify by polling slot.
  b. Clear slot IRQ using C02X and vertify by polling slot.
  c. Vertify that the 6522 at B6 caught the IRQ and that it was the correct one and that it can be cleared.
  d. Set slot IONMI using DEVICE SELECT and vertify by polling IONMI.
  e. Clear slot IONMI using C02X and vertify by polling IONMI.
Step 7 Check for shorts between slot IRQ's by setting IRQ on one slot at a time and checking each IRQ on the other slots.

AUDIO troubles are usualy fairly simple to repair. The most common ailments are listed below:
The most common frequent failure is the LM380 which is located at M11, and rarely you may find a problem in its associated circuitry, notably R36, a 1K resistor and C12, a 10uf cap.
The second most frequent, usually noted on the C040 portion of the test, is the 556 located at A7.
Another common ailment is J11, the external speaker jack which is the mini-phone jack at N4. Note that a bad contact in this jack can also prevent you from hearing any internal sound.
Failure of the C030 test can be caused by the 74LS74 at H7.
And last, a failure of the FFE0 test can be caused by either the 6522 at

B5, or RP9 the SIP located at C5.

ACIA problems are also usually fairly simple and usually end up being caused by only a few items:
The most common failure is, of course, the 6551 itself. This is located at B2.
The next items to check, will be the 1488 at J2 and the 1489 at K2.
The third most common failure is J4, the 25 pin D connector at N2.
The less likely things to check, are, the SEL6551 from the 74LS138 at K4-7, and the RC network (or R-pak) at N3.

PADDLE PORT problems frequently coincide with printer port problems. This is because they both share the DB-9 connector N10, (J3). Some causes of paddle port problems are:
The 9708 located at M9. This is the most common cause of failures.
The second most frequent cause of failures is the RC network at N10.
Other things to check that can sometimes cause problems, are the 9334's at locations H6, L12, and L13. These IC's supply some fo the enable neccessary during the paddle port tet, including the disk pahses, and disk side 2/1 signals used to test the switches, as well as the ENSIO and ENSEL signals.
Also check the enables coming from the 74LS138's at K4 and K7.
Finally check the 74Ls251 at L7 and its enables.

RAM FAILURES can be almost as much fun as no reset can be. Some of the things to look for are:
Of course, the most obvious thing to check is the F6E6 test results and see which row, group, chip(s) are causing problems. Also check the two memory board connectors J16 and J17 at this time.
You have about 98% chance of the problem being on sheet 2 of the schematic.
With the highest probability, being the 74LS399 at A9 and the 74S3 74S374 at D13.
Next check the 7643's at locations C10, C11, C12, and C13, and then check the 74S153's at E12, E13, F12, and F13.
It may be a little help to do the following IF and ONLY IF you can get into the monitor routines using a CONTROL-APPLE-RESET:

a. Type the following:
   FFD0: 0/FFDF:IF/FFEF:0 (RETURN)
   You have just set the bank register and zero page to 0 and disabled the screen and IO addresses. (Note that FFEF if the bank register and you may want to try settings other than 0 if this setup doesn't find your problem.
b. Now type:
   0.FFFF/X (RETURN)
   The address bus should now be one big 16-bit counter and therefore easier to trace with an oscilloscope.

PRINTER PORT failures will show up as paddle port failures most of the time. The few exceptions are, that some of the polarities of the enables are reversed, causing the signal direction to also be reversed. (For example, a paddle port INPUT becomes a printer port OUTPUT). Also, be sure to check the connections to slot 1 to insure that the test hardware will function properly. The best way to check this, is to check for continuity from slot 1 to slot 4, (except for pins 1, 30, and 41).

DISK failures will usually prevent the system from booting properly. There are, however, a few things which should be mentioned here.

J1 and J6, the EXTERNAL and INTERNAL drive connectos, respectively, are in parallel, with the exception of pins 14, 21, 22, and 26.

A disk phase of SIDE 2/1 failure will usually also show up as a switch failure in the paddle port test.

The RC filter networks at N13 and M13 are also a good place to check for problems. (See the section below on useflu addresses in order to toggle a particular signal).

KEYBOARD failures are another of those problems that, while they occur frequently, are neverthelesss, failry simple fo correct. Some fo the more common failure modes are:

If the fast repeat or the super fast repeat either fail to work, work all the time, or repeat way too fast, check the 556 located at L10 and also the C16 capacitor.

Another thing to check if there is no fast repeat is diode CR5, located M7.

If the data from the keyboard is wrong, check the keyboard encoder chip at H14, (check its power connections too,) or one of the 74LS257's located at H12 or J12.

If one of the above hasn't led to the problem, check the 74LS05 at H9, or the 74LS132 at H10.

Lastly, if the power light of the keyboard fails to light, check transistor Q9.

ROM failures are almost ALWAYS, (99% of the time), the ROM chip itself located at B9. On rare occassions, it could be that the IC located at F9 is NOT a 341-0055, as it should be.

THERMAL or "HEAT SENSITIVE" failures: (These should be vertified as heat sensitive as described in section 4.4 above).

After vertifying that the unit is actually heat sensitive, you will have to locate the area of the board where the problem is. Do this by looping on the portion of the diagnostic that failed and moving the heat gun over the affected areas. If the unit does not fail within a few minutes, move the heat gun to a different area fo the board and continue the process.

When the test begins to fail, you have found the correct AREA of the board.

You may now want to use, a monitor command of some type with the X (or repeat) command, for your troubleshooting.

The most frequently heat sensitive devices are the ROM located at B9, the 6502-B located at B7, and the 7643 PROMS (with the 342-00xx numbers), scattered throughout the board.

TROUBLESHOOTING INFORMATION

SYSTEM DEATH ERRORS and their meaning:

error code	meaning
$01	bad break (BRK) from SOS
$02	interrupt not found (but received at CPU)
$03	bad zero page allocation
$04	unable to lock NMI
$05	event queue overflow
$06	stack overflow
$07	data manager detected invalid request code

$08	dmgr - too many device handlers (drivers)
$09	memory too small (<64K)
$0A	volume control block not usable
$0B	file control block crashed
$0C	allocation blocks invalid
$0D	directory is not correct
$0E	pathname buffer overflow (too long)
$0F	invalid buffer number
$10	invalid buffer size (=0 or >16K)

^ul

MONITOR AND ESCAPE COMMANDS

MONITOR COMMANDS:

COMMAND	REMARKS
addrl addr2	memory dump, to dump all memory locations from address $30FF you would type, 3000. 30FF and press RETURN.
addrl:byte list	store byte(s) in memory, just like Apple }{, to store data starting at address $3000, you would type, 3000.00 A2 FF 45 9C etc. To store ascii data, you would type, 3000: 'DARRELL' for high bit off, or 3000: "PAYNE" for hihg bit on.
block <addrl.addr2	read block from disk into memory from address 1 to address 2. Block must be in the range $0 to $117 (0-280). For example, 0<2000.20FF would read block 0 of the disk and store the data in memory form $2000 to $20FF. NOTE: 1 block + 512 bytes, and the SOS directory is at block 2.
block <addrl.addr2W	same as above except writes data from address 1 to address 2 onto the disk starting at block.
addr3<addrl.addr2M	move data from memory beginning at location address 1 and ending at address 2 into memory beginning at address 3.
addr3<addrl.addr2V	Vertify that the date in memory from address 1 to address 2 is the same as data in memory beginning at address 3.
byte<addrl.addr2S	search memory for data that matches byte starting at address 1 and continuing search through address 2.
addrG	call subroutine at address. This is the same as a JSR in assembly language, or a CALL in BASIC .
addrJ	jump to address and begin executing code. This is the same as a JMP in assembly language.
U	calls user routine. This actually does a JSR $3F8.
X	repeat entire command line. For example, C0E0/C0E1/X will continue to toggle disk phase 0 on and off.

Note that most of the Monitor commands are the same as they are in the Apple }{, except some have been added and others have been improved.

^UW, 1,2

ESCAPE COMMANDS: These are achieved by pressing the escape key followed by the desired command:

COMMAND	REMARKS
Cntl-K or up arrow	moves cursor up
cntl-J or dn arrow	moves cursor down
cntl-H or left arrow	moves cursor left
cntl-U or rt arrow	moves cursor right
L	clear to end of Line
P	clear ro end of Page
S	clear screen
4	set 40-column display
8	sey 80-column display

using the monitor to cause a particular signal or group of signals to toggle back and forth between high and low levels, can be a valuable troubleshooting tool. Listed below are some commands you can use from the monitor to do this. They are listed as they are found on the Apple /// schematic, by signal name, (all signals on sheet 2 of the schematic are grouped together, page 3 signals likewise, etc.) The signal name is given first, and the next line gives the Monitor commands you must enter to toggle that signal. {C}, means hold down the control key while pressing the next key, and {R} means press the return key. (NOTE: After you have typed a sequence of monitor instructions and used the oscilloscope to look at the signals produced, if you need to look at some different signal, ALWAYS reset the system, and use the CONTROL, APPLE, RESET sequence to re-initialize the system since it could possibly be in an unknown state, caused by either the problem you are trying to isolate, or the last instruction that you typed in).

Page 1 signals are listed on the page where they originate.

Page 2 signals are normally all running. Address lines and bank switch signals are listed on the page where they originate.

Page 3 signals

Address lines:
```
FFD0: 0/FFDF :1F/FFEF" 0{R}
0.FFFF/X{R}
```
Data lines and R/W:
```
3000:A5 5A/3000.3001/X{R}
```
Page 4 signals:

GB outputs, (74LS139)
```
FFC0/FFD0/FFE0/FFF0/X{R}
```
J6 outputs, (74LS138)
```
C000/C100/C200/C300/C400/C500/C600/C700/X{R}
```
K4 OUTPUTS, (74LS138)
```
C080/C090/C0A0/C0B0/C0C0/C0D0/C0E0/C0F0/X{R}
```
K7 outputs, (74LS138)
```
C000/C010/C020/C030/C040/C050/C060/C070/X{R}
```
H6 outputs, (9334)
```
C050.C05F/X{R}
```
6522, Port A, (Environment register)
```
A000.A2 5A A0 A5 8E DF FF 8C DF FF 4C 04 A0{R}
A000G{R}
```
6522, PORT B, (Zero page register)
```
A000: A2 5A A0 A5 8E D0 FF 8C D0 FF 4C 04 A0{R}
A000G{R}
```
Page 5 signals should always be toggling if the screen is enabled, and something is being sent to the screen, (whether or not it actually gets there).

Page 6 signals
L13 outputs, (9334)
C0E0.C0EF/X{R}
L12 OUTPUTS, (9334)
C0D0.C0DF/X{R}
Page 7 signals
BCKSW1-BCKSW4
A000:A2 5A A0 A5 8E EE FF 8C EE FF 4C 04 A0{R}
A000G{R}
L7 outputs (bit 7 only), 74LS251
C060. C06F/X{R}
Sound signals will toggle continuously from sound test ACIA signals
C0F0: 55/C0F0/C0F0:AA/C0F0/X{R}
Page 8 signals
Keyboard A port read
C000/C010/X{R}
Keyboard B port read
C008/C010/X{R}
Page 9 signals should all be running. These are all of the main timing signals for the Apple ///.
Useful addresses to know:
If you wish to know the status of the CPU at the time of a system failure, ($010-$10), you can use CONTROL-APPLE-RESET, to enter the monitor and then examine memory beginning at $19F0, for the information. NOTE, this applies ONLY when the failure occurred while running under control of SOS.
$19F0-19F1............PROGRAM COUNTER
$19F2.................STACK POINTER
$19F3.................ENVIRONMENT REGISTER
$19F4.................ZERO PAGE REGISTER
$19F5.................BANK REGISTER
$19F6.................PROCESSOR STATE REGISTER
$19F7.................ACCUMULATOR (A REGISTER)
$19F8.................INDEX X (X REGISTER) *****
$19F9.................INDEX Y (Y REGISTER)

***** NOTE: If the failure was a $02, (interrrupt not found the index register X should contain one of the following codes:

$00..... IONMI was the interrupt
$01..... ACIA was the interrupt
$02..... CA2 from 6522.E was the interrupt
$03..... CA1 from 6522.E was the interrupt
$04..... shift register from 6522.E was the interrupt
$05..... CB2 from 6522 .E was the interrupt
$06..... CB1 from 6522 .E was the interrupt
$07..... Timer 2 from 6522> e was the interupt
$08..... Timer 1 from 6522. E was the interrupt
$09..... CA2, 6522.D
$0A..... CA1, 6522.D (ANY SLOT but no slot found)
$0B..... Shift register, 6522.D
$0C..... CB2, 6522.D
$0D..... CB1, 6522.D
$0E..... Timer 2, 6522.D
$0F..... Timer 1, 6522.D

$10..... >>>INTERRUPT NOT FOUND <<<
$11..... SLOT 1 was the interrupt
$12..... Slot 2 was the interrupt
$13..... Slot 3 was the interrupt
$14..... Slot 4 was the interrupt

Keyboard:

C000 - "KA" Port

Bit	7	6	5	4	3	2	1	0
	drdy	d6	d5	d4	d3	d2	d1	d0

C008 - "KB" port

7	6	5	4	3	2	1	0
d7	kybd	A2	A1	alk	ctrl	sft	anyky

A2 is solid apple switch
A1 is open apple switch
alk ia alpha-lock
ctrl is control
sft is shift key (either one)
C010 - keyboard reset

Speaker
C030 - toggle speaker (same as Apple }{
C040 - Hardware bell (one beep)
FFE0 - Bit 0 - 5 Apple /// sound (D-A)

Screen Control
C050 - C057 (see sheet 4 of schematic)
C050,C051 - TEXT mode
C052,C053 - MIX mode
C054,C055 - PAGE 2 mode
C056,C057 - HIRES mode

Joysticks, switches, and printer port
C058 - C05F (se sheet 4 of schematic)
C058,C059 - PDL0, Address 0 of A/D
(also disable/enable output handshake)
C05E, C05F - AXC0, Address 1 of A/D
(output handshake line false/true)
C05A,C05B - PDL2, Address 2 of A/D
C05C,C05D - A/D ramp start
(NOTE: To read a particular joystick pot set correct address

as follows:		A3	A2	A1	<---Address lines
joystick #1	(X0)	0	0	1	
"	(Y0)	0	1	0	
joystick #2	(X1)	0	1	1	
"	(Y1)	1	0	0	

Then use C05D to enable the RAMP of the A/D.

Bit 7 of C060 is switch 0
C061 is switch 1
C062 is switch 2
C063 is switch 3
C066 is the joystick timeout (selected above)

C0DC, C0DD is ENSEL (direction of CB1 in 6522. D, SC0)
C0DE, C0DF is ENSIO (serial data R/W in 6522. D, SER)
C064, Bit 7 is IRQ3 and
C065, Bit 7 is IRQ4
C09X is Device select for Slot 1

C0AX is Device select for Slot 2
C0BX is Device select for Slot 3
C0CX is Device select for Slot 4
C1XX is IO select for Slot 1
C2XX is IO select for Slot 2
C3XX is IO select for Slot 3
C4XX is IO select for Slot 4
C0DA disables Character Generator RAM write, and
C0DB enables Character Generator write.
C0D8 disables hire scroll, and
C0D9 enables hires scroll. If enables, then
C0E0, C0E1 is set/clear address VA1
C0E2, C0E3 is set/clear address VB1
C0E4, C0E5 is set/clear address VC1

VC1	VB1	VA1	results in...
0	0	0	no scroll
0	0	1	1 horizontal line wrap
0	1	0	2 horizontal line wrap
0	1	1	3 horizontal line wrap
1	0	0	4 horizontal line wrap
1	0	1	5 horizontal line wrap
1	1	0	6 horizontal line wrap
1	1	1	7 horizontal line wrap

Disk drive Addresses
C0D0, C0D1 clear/set external drive address A0
C0D2, C0D3 clear/set external drive address A1
C0D4, C0D5 enable, external drive power
C0D6, C0D7 Side 1/Side 2 signal. If C0D4 (enable), then

A0	A1	Results in...
0	0	no external drive
0	1	external drive #1
1	0	external dirve #2
1	1	external drive #3

C0E0, C0E1 disk phase 0 set/clear
C0E2, C0E3 disk phase 1 set/clear
C0E4, C0E5 disk phase 3 set/clear
C0E6, C0E7 disk phase 3 set/clear
C0E8, C0E9 drive motor disable/enable (begins time out)
C0EA, C0EB select internal/external drive
RS-232 Port, ACIA, (6551)
C0F0 is received or transmitted data
C0F1 Writing any data causes a programmed reset, while Reading the following:

Bit	7	6	5	4	3	2	1	0
	IRQ	NOT DSR	NOT DCD	TDRO	RDRf1	OVERR	FRMERR	PARERR

C0F2 is the command register:
Bit 7-5 are parity check controls
Bit 4 is ECHO control
Bit 3-2 are transmit controls
Bit 1 is INT
Bit 0 is DTR
C0F3 is the control register:
Bit 7 is STOPB

Bit 6-5 are word length
Bit 4 is NOT XCLOCK
Bit 3-0 are the BAUD rate
VIA 6522 system control registers
FFD0 - Zero Page Register (Z register)
FFDF - Environment register (E register)

Bit	7	6	5	4	3	2	1	0
	1 MHz	IOEN	SCRN	RSTEN	WPROT	PRSTK	ROM 1	ROMEN

FFD2 - data direction register B
FFD3 - Data direction register A
FFD4 - FFD7 Timer 1
FFD8 - FFD9 Timer 2 (used by printer port)
FFDA - Shift register (used by printer port)
CA1 (in) Anyslot IRQ (will not clear)
CA2 (in) printer port input handshake
CB1 (out) Printer port clock
CB2 (out) Printer port serial data
CB2 (out) joystick address 0 set/clear
FFE0 - interrupt flags in / sound out
Bit 7 - IONMI (in)
Bit 6 - IOCT (in)
Bit 5-0 interrupt flags in / bank register (in/out)
Bit 7 - NOT GIRQ
Bit 6 - Not A }{SW
Bit 5 - Not IRQ2
Bit 4 - Not IRQ1
Bits 3-0 - Bank register (B register)
FFE2 - Data direction register B
FFE3 - Data direction register A
FFE4 - FFE7 Timer 1
FFE8 - FFE9 Timer 2 (input to IOCT flag)
FFEA - Shift register (used for VBL)
CA1 (in) clock/calendar IRQ
CA2 (in) keyboard IRQ
CB1, CB2 (out) vertical blanking
List of interrupt flag location:
C000 - Bit 7 = Keyboard
C064 - Bit 7 = Slot 3
C065 - Bit 7 = Slot 4
C070 - = real time clock (function in Z reg)
FFDD - Bit 0 = CA2, printer port input handshake
Bit 1 = CA1, anyslot IRQ
Bit 2 = shift register
Bit 3 = CB2
Bit 4 = CB1
Bit 5 = Timer 2
Bit 6 = Timer 1
Bit 7 = IRQ, any of the above 7 IRQ's
FFE0 - Bit 6 = IOCT
Bit 7 = global IRQ, any IRQ in the system
Bit 5 = Slot 2
Bit 4 = Slot 1
FFED - Bit 0 = CA2, keyboard
Bit 1 = CA1

Bit 2 = Shift register
Bit 3 = CB2, VBL x 8
Bit 4 = CB1, VBL x 1
Bit 5 = timer 2, IOCT (slot)
Bit 6 = Timer 1
Bit 7 = IRQ< any of the above 7 IRQ's

Vertify the problem found. Whenever it is practical always try to replace the problem that you removed to see if the same symptom previously encountered returns. If you have indeed, found the correct problem, the same symptom will return. Otherwise, the probelm probably still exists and further troublshooting is called for.

Vertify the fix. Once you are confident that you have repaired a problem, RETEST the ENTIRE system using ALL of the methods, described above in section 4.0. If no further problems are encountered log and label the board as repaired, making sure that ALL documentation, including SYMPTON, SOLUTION, and METHOD pf fault isolation, (especially if it was a tricky one), are included. If you DO find another problem, then RESTART the diagnostic procedure and attempt to isolate and repair the NEW problem that you ahve encountered. Repeat the entire process as necessary, until ALL problems have been identified and corrected.

APPLE /// COMMON FAILURES (FOR SHOTGUNNING)

SYMPTOM	PROBABLE CAUSE
SELF TEST (F6E6G)	
Self-Test but characters wrong	74S257 (U66 [C12], U69 [C13]) 74LS374 (U4, [M13])
Self-Test with ACIA error message	6551 (U98 [B10])
No-Reset	B8, D13
A/// FINAL TEST: PART A	
No-Boot:	Prom 42 [M14], D3, G13, G11
Video:	
Wrong colors	C5 100 pf
Random Patterns	B8, F10, G11
Sound:	
No sound or weak sound	LM380 (U103 [14])
Sound does't sweep	6522 (U97 [G10])
Serial Port:	
Fails	6551 (U98 [B10])
Paddle Port:	
Switch Fails	74LS251 (U101 [J11])
Paddle Fails	9708 (U105 [L5])
ROM:	
Fails:	341-0031 (U64 [D10])
A/// FINAL TEST: PART B	
Printer Port	6522 (U73 [H10]) 74LS125 (U160 [M4]), 74LS126 (U161 [I7])

This by no means exhaust the possible failures. Try to use your technical ability to find out what's wrong.

Bob Edgington
10-24-80

RAM FAILURE MAP

8	1	1	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1
6	B9	B8	B7	B6	B5	B4	B3	B2
5	B17	B16	B15	B14	B13	B12	B11	B10
4	C17	C16	C15	C14	C13	C12	C11	C10
3	D9	D8	D7	D6	D5	D4	D3	D2
2	D17	D16	D15	D14	D13	D12	D11	D10
1	C9	C8	C7	C6	C5	C4	C3	C2
	1	2	3	4	5	6	7	8

96K

THE RAM FAILURE MAP INDICATES THE PHYSICAL LOCATION (COORDINATES OF THE RAM FAILURE. FOR EXAMPLE, IF WE OBSERVE INVERSED 1'S FOR THE LOWER ROW THIS WOULD CORRESPOND TO A RAM(S) OR RAM ADDRESS FAILURE AT LOCATIONS C9-C10 ON THE MEMORY BOARD.

8	B9	B8	B7	B6	B5	B4	B3	B2
7	B17	B16	B15	B14	B13	B12	B11	B10
6	B9	B8	B7	B6	B5	B4	B3	B2
5	B17	B16	B15	B14	B13	B12	B11	B10
4	C17	C16	C15	C14	C13	C12	C11	C10
3	D9	D8	D7	D6	D5	D4	D3	D2
2	D17	D16	D15	D14	D13	D12	D11	D10
1	C9	C8	C7	C6	C5	C4	C3	C2

128K

RAM FAILURES ARE INDICATED BY INVERSE 1's

RAS OR CAS FAILURES ARE DISPLAYED AS A FAILED ROW (INVER ONE'S

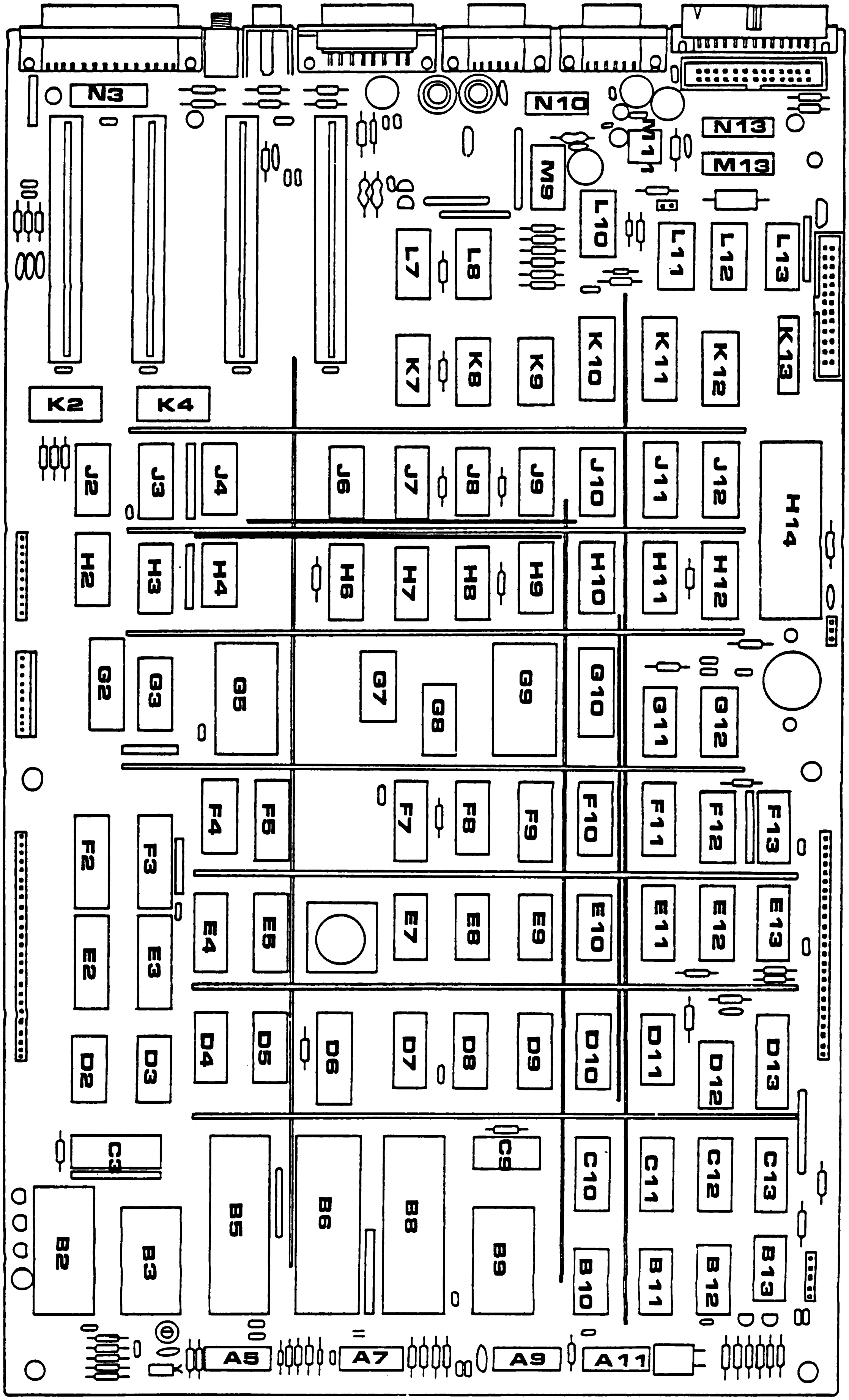
INDIVIDUAL RAM FAILURE (INVERSE 1's) CAN BE DUE TO RAM OR RAM ADDRESSING

APPLE /// IC PARTS BY LOCATION

LOCATION	DESCRIPTION	APPLE PART NUMBER
A05	IC, 556 DUAL TIMER	330-0556
A07	IC, 556 DUAL TIMER	330-0556
A09	IC, 74LS399, QUAD 2 INPUT MUX	306-0399
A11	IC, 74S74, DUAL D-TYPE FLIP-FLOP	308-0074
B02	IC, ACIA 6551A	338-0002
B03	IC,MICROPROCESSOR CLOCK 58167	331-8167
B05	IC, 6522 VERSATILE INTERFACE ADAPTER	338-6522
B06	IC, 6522 VERSATILE INTERFACE ADAPTER	338-6522
B08	IC, MICRO 6502B 3MHZ TEST & BURN-IN	369-6502
B09	IC, ROM BOOT/MONITOR B & T	342-0031
B10	IC, 74LS20, DUAL 4-INPUT NAND	306-0020
B11	IC, 74LS51, AND OR INVERT	306-0051
B12	IC, 74S175, QUAD D-TYPE FLIP FLOP	308-0175
B13	IC, 74S86, QUAD 2 INPUT EXCLUSIVE-OR	308-0086
C03	IC, 8304B 8-BIT TRI-STATE	316-8304
C09	IC, 74LS260, DUAL 5 INPUT NOR	306-0260
C10	IC, PROM 1024 X 4	342-0043
C11	IC, PROM RAS 65,12 VOLT MEMORY BD	341-0044
	IC, PROM RAS65, 5 VOLT MEMORY	342-0061
C12	IC, PROM CASB65 ADDRESSING	342-0056
C13	IC, PROM CAS128, 12 VOLT MEMORY	341-0042
	IC, PROM CASB256, 5 VOLT MEMORY	342-0063
D02	IC, 74S257, QUAD DATA MULTIPLEXER	308-0257
D03	IC, 74S257, QUAD DATA MULTIPLEXER	308-0257
D04	IC, 74LS86,QUAD 2 INPUT EXCLUSIVE OR	306-0086
D05	IC, 74S74, DUAL D-TYPE FLIP-FLOP	308-0074
D06	IC, 74LS244, OCTAL BUFFERS/DRIVERS	306-0244
D07	IC, 74S257, QUAD DATA MULTIPLEXER	308-0257
D08	IC, 74S257, QUAD DATA MULTIPLEXER	308-0257
D09	IC, 74LS02, QUAD 2 INPUT NOR	306-0002
D10	IC, 74S195, 4 BIT PARALLEL SHIFT REG	308-0195
D11	IC, 74S74, DUAL D-TYPE FLIP-FLOP	308-0074
D12	IC, 74LS00, QUAD 2 INPUT NAND	306-0000
D13	IC, 74LS374, OCTAL D-TYPE FLIP-FLOP	306-0374
E02	IC, 74LS374, OCTAL D-TYPE FLIP-FLOP	306-0374
E03	IC, 74LS374, OCTAL D-TYPE FLIP-FLOP	306-0374
E04	IC, 1024 X 4 STATIC RAM 2114	334-0005
E05	IC, 1024 X 4 STATIC RAM 2114	334-0005
E07	IC, 74LS00, QUAD 2 INPUT NAND	306-0000
E08	IC, 74LS08, QUAD 2 INPUT AND	306-0008
E09	IC, 74S10, TRIPLE 3 INPUT NAND	306-0010
E10	IC, 74S86, QUAD 2 INPUT EXCLUSIVE-OR	308-0086
E11	IC, 74LS283, 4 BIT BINARY ADDER	306-0283
E12	IC, 74S153, DUAL 4 TO 1 LINE MUX	308-0153
E13	IC, 74S153, DUAL 4 TO 1 DATA MUX	306-0153
F02	IC, 74S374,OCTAL D-TYPE FLIP-FLOP	308-0374
F03	IC, 74S374, OCTAL D-TYPE FLIP-FLOP	308-0374
F04	IC, 74166,8 BIT SHIFT REGISTER	302-0166
F05	IC, IC PROM 1024 X 4	342-0045
F07	IC, PROM 1024 X 4	342-0046
F08	IC, 74LS08, QUAD 2 INPUT AND	306-0008
F09	IC, PROM, 1024 X 4	342-0055
F10	IC, 74LS161,SYNC BINARY 4 BIT COUNTER	306-0161

APPLE /// IC PARTS BY LOCATION

LOCATION	DESCRIPTION	APPLE PART NUMBER	
F11	IC, 74LS161,SYNC BINARY 4 BIT COUNTER	306-0161	
F12	IC, 74S153, DUAL 4 TO 1 LINE MUX	308-0153	
F13	IC,74S153, DUAL 4 TO 1 MULTIPLEXER	306-0153	
G02	IC, 74S374, OCTAL D-TYPE FLIP-FLOP	308-0374	
G03	IC,74LS157, QUAD 2 TO 1 DATA MUX	306-0157	
G05	IC, VIDEO CONTROL ROM	342-0032	
G07	IC, 74LS133, 13 INPUT NAND	306-0133	
G08	IC, 74LS139, 2 TO 4 LINE DECODERS	306-0139	
G09	IC, ROM, SYNCHROM	342-0030	342-0145A
G10	IC, 74LS374, OCTAL D-TYPE FLIP-FLOP	306-0374	
G11	IC, 74LS161,SYNC BINARY 4 BIT COUNTER	306-0161	
G12	IC, 74LS161,SYNC BINARY 4 BIT COUNTER	306-0161	
H02	IC, 74LS00, QUAD 2 INPUT NAND	306-0000	
H03	IC, 74LS399, QUAD 2 INPUT MUX	306-0399	
H04	IC, 74LS51, AND OR INVERT	306-0051	
H06	IC, 9334, TESTED & BURN-IN	302-9334	
H07	IC, 74LS74, DUAL D FLIP-FLOPS	306-0074	
H08	IC, 74LS04, HEX INVERTERS	306-0004	
H09	IC, 74LS05, OPEN COL HEX INV	306-0005	
H10	IC, 74LS132, QUAD 2 INP NAND SCH TRIGG	306-0132	
H11	IC, 74LS74, DUAL D-TYPE FLIP-FLOP	305-0074	
H12	IC, 74LS257, QUAD DATA MUX	306-0257	
H14	IC, ROM KEYBOARD ENCODER A3	342-0035	
J02	IC, 1488 QUAD LINE DRIVER	360-1488	
J03	IC, 74LS151, 1 OF 8 DATA MUX	308-0151	
J04	IC, 74LS21, DUAL 4 INPUT AND	306-0021	
J06	IC, 74LS138, 3-TO-8 LINE DECODERS	306-0138	
J07	IC, 74LS133, 13 INPUT NAND	306-0133	
J08	IC, 74LS32, QUAD 2 INPUT OR	306-0032	
J09	IC, 74LS125,QUAD TRI-STATE BUFFERS	306-0125	
J10	IC, 74LS126, QUAD TRI-STATE BUFFERS	306-0126	
J11	IC, 74LS139, 2 TO 4 LINE DECODERS	306-0139	
J12	IC, 74LS257,QUAD DATA MUX	306-0257	
K02	IC, 1489 LINE RECEIVER	360-1489	
K04	IC, 74LS138, 3-TO-8 LINE DECODER	306-0138	
K07	IC, 74LS138, 3-TO-8 LINE DECODERS	306-0138	
	IC, 74LS374, OCTAL D-TYPE FLIP-FLOP	306-0374	
K08	IC, 74LS11, TRIPLE 3 INPUT AND	306-0011	
K09	IC, 74LS04, HEX INVERTERS	306-0004	
K10	IC, 74LS323,8 BIT BIDIRECT SHIFT REG	306-0323	
K11	IC, PROM, STATE MACHINE P6A	342-0028	
K12	IC, 74LS174, HEX D-TYPE FLIP-FLOP	306-0174	
K13	RESISTOR ARRAY, 47 OHMS	112-0102	
L07	IC, 74LS251, IC, DATA MULTIPLEXER	306-0251	
L08	IC, 74S153, DUAL 4 TO 1 LINE MUX	308-0153	
L10	IC, 556 DUAL TIMER	330-0556	
L12	IC, 9334,	302-9334	
L13	IC, 9334	302-9334	
M09	IC, 9708, 6 CHANNEL 8 BIT A/D	356-9708	
M11	IC, LM380 AUDIO POWER AMPLIFIER	354-0380	
M13	RESISTOR ARRAY, 47 OHMS	112-0102	
N03	RESISTOR ARRAY, 47 OHMS	112-0102	
N10	RESISTOR ARRAY, 47 OHM	112-0102	
N13	RESISTOR ARRAY 47 OHM	112-0102	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PRINTED 23-Jul-82  13:26                      PERSONAL COMPUTER SYSTEMS                       BIL VERSION 29-Mar-79  PAGE   1

EFFECTIVITY DATE: ALL             I N D E N T E D   B I L L S   O F   M A T E R I A L

  PARENT PART: 610-8156         INACT FG,256K APPLE III           UM: EA   PROD CODE:     ECN: A116   ASSEMBLY QTY:    1
                                ERC: B   SRCE CODE: A   TYPE: *   ABC: A   PLAN CODE: U   DATE: 08-Jul-82

             COMPONENT      E PART DESCRIPTION                       PR S T S A P        EXTENDED   ECN      START              CLOSE
LEVEL        PART NUMBER    R                                        CD C Y P B L UM     QTY PER    CHG    DATE      S/N        DATE     S/N

2            610-8128D      H INACT.DWG ASSY,FINAL 128K A3              D *   * U EA        0       A116 18-Jan-82          08-Jul-82
2            030-0102       E INACT.PACKING LST,A3 SYSTEM BOX        EX X 7 P C P EA        1       A116 18-Jan-82          08-Jul-82
2            030-0103       C INACT.UNPACKING INST A3 SYS BOX        EX X 7 P C P EA        1       A116 18-Jan-82          08-Jul-82
2            030-0104       C SYSTEM REGISTRATION CARD A2/A3         EX P 7 P C P EA        1       A001 18-Jan-82          08-Jul-82
2            590-0003       C CABLE, A.C. POWER CORD                 2M P 1 P B P EA        1       C-10 18-Jan-82          08-Jul-82
2            590-0025       O CABLE, MONITOR                         RC P 1 P C P EA        1       441  18-Jan-82          08-Jul-82
2            610-0006       A INACT.ASSY,FOAM CAP SIDE A RIGHT       EX X 7 P C P EA        1       A116 18-Jan-82          08-Jul-82
 3           944-0062D      O ASSY DWG, FOAM INSIDE/OUTSIDE          EX D 7 S * U EA        0            13-Oct-80
 3           944-0062       A FOAM, ETHER DIE-CUT OUTSIDE            EX X 7 P D P EA        1       473  13-Oct-80
 3           944-0063       O FOAM, ETHER KNOCK-OUT INSIDE           EX X 7 P C P EA        1       473  13-Oct-80
 3           942-0091       A CORRUGATED PANEL, END CAP              EX X 7 P C P EA        1       473  13-Oct-80
2            610-0007       A INACT.ASSY,FOAM CAP SIDE B LEFT        EX X 7 P C P EA        1       A116 18-Jan-82          08-Jul-82
 3           944-0062D      O ASSY DWG, FOAM INSIDE/OUTSIDE          EX D 7 S * U EA        0            13-Oct-80
 3           944-0062       A FOAM, ETHER DIE-CUT OUTSIDE            EX X 7 P D P EA        1       473  13-Oct-80
 3           944-0063       O FOAM, ETHER KNOCK-OUT INSIDE           EX X 7 P C P EA        1       473  13-Oct-80
 3           942-0091       A CORRUGATED PANEL, END CAP              EX X 7 P C P EA        1       473  13-Oct-80
2            610-0008      MA INACT.ASSY,FOAM/CORRUGATED PAD         EX X 7 P C P EA        1       A116 18-Jan-82          08-Jul-82
2            610-6156       D ASSY, CHASSIS 256K A3                     N *   A P EA        1       A035 18-Jan-82          08-Jul-82
 3           610-6128D      N DWG ASSY, CHASSIS 128K A3                 D *   * U EA        0       A024 18-Jan-82
 3           610-5110       A SUBASSY, TESTED, KEYBOARD A3           WS A 1   A P EA        1       948  21-Jan-82
  4          610-0110       A ASSY,UNTST,KEYBOARD A3,ALPS               A *   * P EA        1       948  21-Jan-82
   5         610-0110D      A DWG,UNTST,KEYBOARD A3,ALPS                * *   * * EA        0       948  21-Jan-82
   5         062-0029       C SPECIFICATION, KEYBOARD A3             EX D 7 S * U EA        0       948  21-Jan-82
   5         705-0015       A SWITCH, KBD KCC ALPS                   RP P 1 P C P EA       69       362  21-Jan-82
   5         705-0027       A SWITCH, ALS KCC ALT ACTION                P *   * P EA        1       948  21-Jan-82
   5         705-0026       A SWTCH, ALPS KFF, DOUBLE ACTION            P *   * P EA        4       948  21-Jan-82
   5         710-0003       A LAMP, BI-PIN 5V .115A                  RP P 1 P C P EA        1       362  21-Jan-82
   5         517-0013      MA PIN, LAMP                              RP P 1 P C P EA        2       362  21-Jan-82
   5         805-0103       A PLATE, KEYBOARD A3 ALPS                   P *   * P EA        1       948  21-Jan-82
   5         699-0078       A PCB,MAIN & PIGGYBACK,KBD,A3               P *   * P EA        1       948  21-Jan-82
   5         870-0013       A CRANK, KEYBOARD A3 ALPS                   P *   * P EA        1       948  21-Jan-82
   5         815-0532       A CRANK GUIDE, STRAIGHT, ALPS               P *   * U EA        2       948  21-Jan-82
   5         815-0531       A ADAPTER, STRAIGHT KEYCAP                  P *   * U EA       70       948  21-Jan-82
   5         705-0009       A SWITCH,END ACTUATED PUSH BUTTON        RP P 1 P C P EA        1       P150 21-Jan-82
   5         590-0111       A CABLE ASSY, KEYBOARD A3                   P *   * P EA        1       948  21-Jan-82
   5         815-0184       B PIVOT SPACEBAR CRANK KCC               RM P 1 P C P EA        2       947  21-Jan-82
   5         515-0014       O CONN, 26 PIN HEADER                    RP P 1 P C P EA        1       442  21-Jan-82
   5         403-1606       B SCREW, 6-32 3/8 CRPHD                  EX X 1 S C U EA        5       C086 21-Jan-82
   5         815-0530       A SPACER, RESET SWITCH                      P *   * U EA        1       948  21-Jan-82
   5         610-0197       O SUBASSY, KEYCAPS, COMPLETE SET A3      WS N 1 P B P EA        1       441  21-Jan-82
    6        815-0088D      O SPEC, APPLE III KEYCAPS                EX D 7   * U EA        0       441  05-Jun-80
    6        815-0088       O KEY CAP, APPLE 3, ESCAPE               RM P 1   * P EA        1       441  05-Jun-80
    6        815-0089       O KEY CAP, APPLE 3, ! / 1                RM P 1   * P EA        1       441  05-Jun-80
    6        815-0090       O KEY CAP, APPLE 3, @ / 2                RM P 1   * P EA        1       441  05-Jun-80
    6        815-0091       O KEY CAP, APPLE 3, # / 3                RM P 1   * P EA        1       441  05-Jun-80
    6        815-0092       O KEY CAP, APPLE 3, $ / 4                RM P 1   * P EA        1       441  05-Jun-80
    6        815-0093       O KEY CAP, APPLE 3, % / 5                RM P 1   * P EA        1       441  05-Jun-80
    6        815-0094       O KEY CAP, APPLE 3, ^ / 6                RM P 1   * P EA        1       441  05-Jun-80
    6        815-0095       O KEY CAP, APPLE 3, & / 7                RM P 1   * P EA        1       441  05-Jun-80
    6        815-0096       O KEY CAP, APPLE 3, * / 8                RM P 1   * P EA        1       441  05-Jun-80
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PRINTED 23-Jul-82  13:27                       PERSONAL COMPUTER SYSTEMS                     BIL VERSION 29-Mar-79  PAGE    2

EFFECTIVITY DATE: ALL                   I N D E N T E D   B I L L S   O F   M A T E R I A L

 PARENT PART: 610-8156            INACT.FG.256K APPLE III              UM: EA   PROD CODE:     ECN: A116   ASSEMBLY QTY:     1
                                  ERC: B   SRCE CODE: A   TYPE: *     ABC: A   PLAN CODE: U   DATE: 08-Jul-82

             COMPONENT         E PART DESCRIPTION                 PR S T S A P        EXTENDED   ECN        START               CLOSE
LEVEL        PART NUMBER       R                                  CD C Y P B L UM     QTY PER    CHG    DATE        S/N     DATE       S/N

  6          815-0097          O KEY CAP, APPLE 3, ( / 9          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0098          O KEY CAP, APPLE 3, ) / 0          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0099          O KEY CAP, APPLE 3, _ / -          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0100          O KEY CAP, APPLE 3, + / =          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0101          O KEY CAP, APPLE 3, : / \          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0102          O KEY CAP, APPLE 3, 7              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0103          O KEY CAP, APPLE 3, 8              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0104          O KEY CAP, APPLE 3, 9              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0105          O KEY CAP, APPLE 3, TAB            RM P 1   * P EA        1       441   05-Jun-80
  6          815-0106          O KEY CAP, APPLE 3, Q              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0107          O KEY CAP, APPLE 3, W              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0108          O KEY CAP, APPLE 3, E              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0109          O KEY CAP, APPLE 3, R              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0110          O KEY CAP, APPLE 3, T              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0111          O KEY CAP, APPLE 3, Y              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0112          O KEY CAP, APPLE 3, U              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0113          O KEY CAP, APPLE 3, I              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0114          O KEY CAP, APPLE 3, O              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0115          O KEY CAP, APPLE 3, P              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0116          O KEY CAP, APPLE3, { / [           RM P 1   * P EA        1       441   05-Jun-80
  6          815-0117          O KEY CAP, APPLE 3, } / ]          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0118          O KEY CAP, APPLE 3, ~ / `          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0119          O KEY CAP, APPLE 3, 4              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0120          O KEY CAP, APPLE 3, 5 (W/SENSOR)   RM P 1   * P EA        1       441   05-Jun-80
  6          815-0121          O KEY CAP, APPLE 3, 6              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0122          O KEY CAP, APPLE 3, CONTROL        RM P 1   * P EA        1       441   05-Jun-80
  6          815-0123          O KEY CAP, APPLE 3, A              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0124          O KEY CAP, APPLE 3, S              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0125          O KEY CAP, APPLE 3, D (W SENSOR)   RM P 1   * P EA        1       441   05-Jun-80
  6          815-0126          O KEY CAP, APPLE 3, F              EX P 1   * P EA        1       441   05-Jun-80
  6          815-0127          O KEY CAP, APPLE 3, G              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0128          O KEY CAP, APPLE 3, H              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0129          O KEY CAP, APPLE 3, J              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0130          O KEY CAP, APPLE 3, K (W SENSOR)   RM P 1   * P EA        1       441   05-Jun-80
  6          815-0131          O KEY CAP, APPLE 3, L              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0132          O KEY CAP, APPLE 3, : / ;          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0133          O KEY CAP, APPLE 3, " / '          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0134          O KEY CAP, APPLE 3, RETURN         RM P 1   * P EA        1       441   05-Jun-80
  6          815-0135          O KEY CAP, APPLE 3, 1              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0136          O KEY CAP, APPLE 3, 2              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0137          O KEY CAP, APPLE 3, 3              RM P 1   * P EA        1       SARA  05-Jun-80
  6          815-0138          O KEY CAP, APPLE 3, SHIFT          RM P 1   * P EA        1       441   05-Jun-80
  6          815-0139          O KEY CAP, APPLE 3, Z              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0140          O KEY CAP, APPLE 3, X              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0141          O KEY CAP, APPLE 3, C              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0142          O KEY CAP, APPLE 3, V              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0143          O KEY CAP, APPLE 3, B              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0144          O KEY CAP, APPLE 3, N              RM P 1   * P EA        1       441   05-Jun-80
  6          815-0145          O KEY CAP, APPLE 3, M              RM P 1   * P EA        1       441   05-Jun-80
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EFFECTIVITY DATE: ALL              I N D E N T E D  B I L L S  O F  M A T E R I A L

  PARENT PART: 610-8156      INACT.FG,256K APPLE III            UM: EA   PROD CODE:     ECN: A116   ASSEMBLY QTY:    1
                             ERC: B  SRCE CODE: A  TYPE: *     ABC: A   PLAN CODE: U  DATE: 08-Jul-82

             COMPONENT       E PART DESCRIPTION                 PR S T S A P      EXTENDED  ECN      START              CLOSE
LEVEL        PART NUMBER     R                                  CD C Y P B L UM   QTY PER   CHG   DATE      S/N      DATE      S/N

    6        815-0147        0 KEY CAP, APPLE 3, > / .          RM P 1   * P EA      1      441  05-Jun-80
    6        815-0148        0 KEY CAP, APPLE 3, ? / /          RM P 1   * P EA      1      441  05-Jun-80
    6        815-0149        0 KEY CAP, APPLE 3, SHIFT          RM P 1   * P EA      1      441  05-Jun-80
    6        815-0150        0 KEY CAP, APPLE 3, ARROW UP       RM P 1   * P EA      1      441  05-Jun-80
    6        815-0151        0 KEY CAP, APPLE 3, 0 (ZERO)       RM P 1   * P EA      1      441  05-Jun-80
    6        815-0152        0 KEY CAP, APPLE 3, . (DECIMAL)    RM P 1   * P EA      1      441  05-Jun-80
    6        815-0153        0 KEY CAP, APPLE 3, ALPHA LOCK     RM P 1   * P EA      1      441  05-Jun-80
    6        815-0154        0 KEY CAP, APPLE 3, APPLE 1        RM P 1   * P EA      1      441  05-Jun-80
    6        815-0155        0 KEY CAP, APPLE 3, APPLE 2        RM P 1   * P EA      1      441  05-Jun-80
    6        815-0156        0 KEY CAP, APPLE 3, SPACE BAR      RM P 1   * P EA      1      441  05-Jun-80
    6        815-0157        0 KEY CAP, APPLE 3, ARROW LEFT     RM P 1   * P EA      1      441  05-Jun-80
    6        815-0158        0 KEY CAP, APPLE 3, ARROW RIGHT    RM P 1   * P EA      1      441  05-Jun-80
    6        815-0159        0 KEY CAP, APPLE 3, ARROW DOWN     RM P 1   * P EA      1      441  05-Jun-80
    6        815-0160        0 KEY CAP, APPLE 3, - (MINUS)      RM P 1   * P EA      1      441  05-Jun-80
    6        815-0161        0 KEY CAP, APPLE 3, ENTER          RM P 1   * P EA      1      441  05-Jun-80
    6        815-0163        3 RESET KEY, APPLEIII              RM P 1   * P EA      1      427  05-Jun-80
    6        815-0179        1 SPACER, RESET SWITCH A3          RM P 1 P C P EA      1      427  05-Jun-80
    6        062-0032D       0 DWG, KEY CAP 1 SPACE 17 DEG      EX.D 7 S * U EA      0      441  05-Jun-80
    6        062-0033D       0 DWG, KEY CAP 1 SPACE             EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0034D       0 DWG, KEY CAP 1 SPACE 10 DEG      EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0036D       0 DWG, KEY CAP 1 SPACE W/BUMP      EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0037D       0 DWG, KEY CAP 1 SPACE W/BUMP 5 DEG EX D 7 S * U EA     0      441  05-Jun-80
    6        062-0038D       0 DWG, KEY CAP 1-1/2 SPACE         EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0039D       0 DWG, KEY CAP 1-1/4 SPACE 17 DEG  EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0040D       0 DWG, KEY CAP 1-1/2 SPACE 5 DEG   EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0041D       0 DWG, KEY CAP 1-3/4 SPACE 10 DEG  EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0042D       0 DWG, KEY CAP 2 SPACE 10 DEG      EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0043D       0 DWG, KEY CAP 2 SPACE 17 DEG      EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0044D       0 DWG, KEY CAP 2-1/4 SPACE 17 DEG  EX D 7 S * U EA      0      441  05-Jun-80
    6        062-0049D       0 DWG, KEY CAP 6-1/2 SPACE         EX D 7 S * U EA      0      441  05-Jun-80
   4         063-0079        0 A3, KEYBOARD TEST AND INSPECTION EX D 7 S * U EA      0      M281 21-Jan-82
  3          600-0009        B ASSY, SPEAKER                    RM X 1 P C P EA      1      491  18-Jan-82
   4         731-0001        A SPEAKER, 8 OHM .2W               EX P 7 P B P EA      1      491  15-Apr-82
   4         561-2400        B WIRE, BLACK, 24 AWG, 7 X 32      EX X 1 P C P FT      0.0057 C018 15-Apr-82
   4         520-0100        A HOUSING, CONN SKT, CRIMP, 2 PIN  RP P 1   * P EA      1      491  15-Apr-82
   4         517-0002        B CONNECTOR, CONTACT CRIMP TYPE    RP P 1 P C P EA      2      C-1  15-Apr-82
  3          650-5201        B SBASY, DISK 3, A3 W/ANALOG BD, INT WS P 1 P A P EA    1      816  18-Jan-82
   4         650-4201        0 ASSY,PCB,TST,DISK ANALOG BD A3   TS A 1 P A P EA      1      631  05-Jun-80
    5        650-0201        D ASSY,PCB,UNTST,DISK ANALOG BD A3 UN A 1 P B P EA      1      805  18-Mar-81
    6        050-0031        C SCHEMATIC, DISK ANALOG BD APPLE III EX D 7 P D U EA   0      805
    6        820-0024        C PCB, DISK ANALOG BD APPLE III    RP P 1 P B P EA      1      805  12-May-80
    6        101-2271        0 RES 1/2W 5% 270 OHM              RP P 1 P C P EA      1      426  12-May-80
    6        101-2331        0 RES 1/2W 5% 330 OHM              RP P 1 P C P EA      1      426  12-May-80
    6        101-2561        0 RES 1/2W 5% 560 OHM              RP P 1 P C P EA      1      426  12-May-80
    6        101-4102        A RES 1/4W 5% 1K OHM               RP P 1 P C P EA      6      426  12-May-80
    6        101-4103        A RES 1/4W 5% 10K OHM              RP P 1 P C P EA      5      426  22-Jul-81
    6        101-4104        A RES 1/4W 5% 100K OHM             RP P 1 P C P EA      2      426  12-May-80
    6        101-4153        A RES 1/4W 5% 15K OHM              RP P 1 P C P EA      2      426  22-Jul-81
    6        101-4202        A RES 1/4W 5% 2K OHM               RP P 1 P C P EA      1      426  12-May-80
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PRINTED 23-Jul-82  13:30                  PERSONAL COMPUTER SYSTEMS                          BIL VERSION 29-Mar-79  PAGE    4

EFFECTIVITY DATE: ALL               I N D E N T E D   B I L L S   O F   M A T E R I A L

  PARENT PART: 610-8156          INACT.FG,256K APPLE III              UM: EA   PROD CODE:      ECN: A116   ASSEMBLY QTY:     1
                                 ERC: B   SRCE CODE: A   TYPE: *     ABC: A   PLAN CODE: U   DATE: 08-Jul-82

             COMPONENT         E PART DESCRIPTION                      PR S T S A P      EXTENDED   ECN        START              CLOSE
LEVEL        PART NUMBER       R                                       CD C Y P B L UM   QTY PER    CHG    DATE        S/N     DATE         S/N

   6         101-4302          A RES 1/4W 5% 3K OHM                    RP P 1 P C P EA      2       426   12-May-80
   6         101-4472          A RES 1/4W 5% 4.7K OHM                  RP P 1 P C P EA      1       426   12-May-80
   6         101-4910          A RES 1/4W 5% 91 OHM                    RP P 1 P C P EA      1       426   12-May-80
   6         101-4822          A RES, 1/4W 5% 8.2K OHM                 RP P 1 P C P EA      1       C127  22-Jul-81
   6         108-1372          O RES 1/4W 1% 137 OHM                   RP P 1 P C P EA      2       442   12-May-80
   6         108-5762          O RES 1/4W 1% 576 OHM                   RP P 1 P C P EA      1       442   12-May-80
   6         108-6342          O RES 1/4W 1% 634 OHM                   RP P 1 P C P EA      1       442   12-May-80
   6         108-8872          O RES 1/4W 1% 887 OHM                   RP P 1 P C P EA      2       442   12-May-80
   6         109-0003          O POT, TRIM 10K OHMS 20%                RP P 1 P C P EA      2       442   22-Jul-81
   6         120-0001          A CAP, .22uF 5% 100V                    RP P 1 P C P EA      1       442   12-May-80
   6         125-5101          A CAP, 10uF 16V                         RP P 1 P C P EA      1       433   12-May-80
   6         125-6401          A CAP, 220uF 16V                        RP P 1 P C P EA      1       433   12-May-80
   6         125-6701          A CAP, 470uF 6.3V                       RP P 1 P C P EA      1       433   12-May-80
   6         132-7601          O CAP, 3000pF 10% Z5F 50V               RP P 1 P C P EA      1       426   12-May-80
   6         132-8102          O CAP, .01uF 20% Z5U 50V                RP P 1 P C P EA      2       426   12-May-80
   6         135-9101          A CAP,.1uF +80-20% Z5U/Y5V 50V          RP P 1 P C P EA     11       433   22-Jul-81
   6         137-6101          O CAP, 100pF 5% 200PPM 500VDC           RP P 1 P C P EA      1       442   12-May-80
   6         137-6601          O CAP, 330pF 5% 200PPM 500VDC           RP P 1 P C P EA      2       442   12-May-80
   6         137-6701          O CAP, 510pF 5% 200PPM 500VDC           RP P 1 P C P EA      1       442   12-May-80
   6         151-5801          B CHOKE, 68uH 10%                       RP P 1 P B P EA      1       479   12-May-80
   6         151-6701          O CHOKE, 470uH 10%                      RP P 1 P B P EA      2       442   12-May-80
   6         305-0125          A IC, 74LS125                           RI P 1 P B P EA      1       442   12-May-80
   6         327-2003          O IC,2003A DARLINGTON TRANSIS. ARRAY    RI P 1 P C P EA      1       449   12-May-80
   6         351-3146          O IC, 3146 HI VOLT. TRANSISTOR ARRAY    RP P 1 P C P EA      1       449   12-May-80
   6         355-3470          O IC, MC3470 FLOPPY DISK READ AMPLIF.   RI P 1 P B P EA      1       449   12-May-80
   6         371-4148          A DIODE, 1N4148                         RP P 1 P C P EA      4       731   12-May-80
   6         372-3906          A TRANSISTOR,PNP SW.&AMP. 2N3906        RP P 1 P C P EA      1       C026  12-May-80
   6         376-0001          A TRANSISTOR, MPS-U51                   RP P 1 P C P EA      1       C111  12-May-80
   6         515-0080          O HEADER, 26 PIN RT. ANGLE W/O EARS     RP P 1 P C P EA      2       482   17-Nov-80
   6         511-1801          C SOCKET, IC 18 PIN                     RP P 1 P C P EA      1       799   12-May-80
   6         511-1401          C SOCKET, IC 14 PIN                     RP P 1 P C P EA      4       799   12-May-80
   6         511-1601          C SOCKET, IC 16 PIN                     RP P 1 P C P EA      1       799   12-May-80
   6         515-0005          B PIN, SINGLE                           RP P 1 P C P EA      9       C115  12-May-80
   6         515-0009         ?O PIN CONN, 4 POS. APPLE SPEC.          RP P 1 P C P EA      1       NONE  12-May-80
   6         155-7103          B CHOKE, COIL 28uH                      RP P 1 P B P EA      2       C021  23-Feb-81
   6         371-4003         MA DIODE, 1N4003                         RP P 1 P B P EA      2       C076  12-May-80
   6         305-0074          A IC, 74LS74                            RI P 1 P B P EA      1       442   11-Mar-81
   6         101-4561          A RES 1/4W 5% 560 OHM                   RP P 1 P C P EA      1       426   12-May-80
   6         515-0015          O HEADER, 26 PIN T&B #609-2627          RP P 1 P C P EA      0       SARA  12-May-80              17-Nov-80
   6         155-5602          A INDUCTOR FILTER 27 UH                 RP P 1 P B P EA      2       DC44  12-May-80              23-Feb-81
   6         305-0032          A IC, 74LS32                            RI P 1 P B P EA      1       442   11-Mar-81
   6         108-1274          O RES, 1/8W 1% 12.7K OHM                RP P 1 P C P EA      1       SARA  12-May-80              11-Mar-81
   6         109-0004          O POT, TRIM 20K OHMS 20%                RP P 1 P C P EA      1       442   11-Mar-81              21-Jul-81
  4          699-0032          O ASSY, OEM ALPS DISK DRIVE             VX P 1 P A P EA      1       441   05-Jun-80
  4          815-0162          E DOOR CLIP, DISK APPLEIII              RM X 1 P C P EA      1       657   05-Jun-80
  4          815-0164         ME DOOR, DISK APPLEIII                   RM P 1 P C P EA      1       542   05-Jun-80
  4          815-0165         MH FRONT YOKE, DISK APPLE III            RM P 1 P C P EA      1       499   05-Jun-80
  4          517-0015          B CONNECTOR, BUTT CRIMP                 RP X 1 P C P EA      2       766   05-Jun-80
  4          710-0004         MA LED, RED APPLE III DISKCABLE          RP X 1 P C P EA      1       552   05-Jun-80
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EFFECTIVITY DATE: ALL               I N D E N T E D  B I L L S  O F  M A T E R I A L

 PARENT PART: 610-8156          INACT.FQ,256K APPLE III          UM: EA   PROD CODE:     ECN: A116   ASSEMBLY QTY:    1
                                ERC: B   SRCE CODE: A   TYPE: *  ABC: A   PLAN CODE: U   DATE: 08-Jul-82

            COMPONENT        E PART DESCRIPTION                  PR S T S A P      EXTENDED  ECN      START             CLOSE
LEVEL       PART NUMBER      R                                   CD C Y P B L UM   QTY PER   CHG   DATE       S/N     DATE      S/N

  4         805-0035         Q SHIELD, DRIVE APPLEIII            RM P 1 P C P EA      1      763  05-Jun-80
  4         410-1206         B SCREW, M2.5 X 0.45 X 6MM POZI DR  EX X 1 P C P EA      2      C086 28-Jan-81
  4         825-0084         O LABEL, SERIAL#, INT. DISK A3      EX X 7 P C P EA      1      441  05-Jun-80
  4         914-0028         A CARD, CARRIAGE LOCK                  P *   * P EA      1      816  15-Sep-81
 3          825-0054         C LABEL, APPLE LOGO NAMEPLATE       EX X 7 P C P EA      1      A035 18-Jan-82          09-May-82
 3          590-0017         C CABLE, POWER SUPPLY/MN BD APPLE III RC P 1 P C P EA    1      A044 18-Jan-82
  4         517-0040         A CONN, RECPT 10 PIN                RP P 1   * P EA      2      559  19-Jan-81
  4         561-2209         O WIRE, #22 AWG STRANDED W/PVC INS. EX P 1   * P RL    100           19-Jan-81          17-May-82
  4         550-0107         B TUBING, HEAT SHRINK 3/8 ID WHITE  EX P 7   * P FT      0.8000 C082 19-Jan-81
  4         561-2200         B WIRE, BLACK, 22 AWG, 7 X 30          X *   * P FT      0.0080 C057 17-May-82
  4         561-2211         B WIRE, BROWN, 22 AWG, 7 X 30          P *   * P FT      0.0080 764  17-May-82
  4         561-2222         B WIRE, RED, 22 AWG, 7 X 30            P *   * P FT      0.0080 764  17-May-82
  4         561-2233         B WIRE, ORANGE, 22 AWG, 7 X 30         P *   * P FT      0.0080 764  17-May-82
  4         561-2244         B WIRE, YELLOW, 22 AWG, 7 X 30         P *   * P FT      0.0080 764  17-May-82
  4         561-2255         B WIRE, GREEN, 22 AWG, 7 X 30       EX P 1   * P FT      0.0080 764  17-May-82
  4         561-2266         B WIRE, BLUE, 22 AWG, 7 X 30           * *   * * EA      0.0080 C116 17-May-82
  4         561-2277         B WIRE, VIOLET, 22 AWG, 7 X 30         P *   * P FT      0.0080 764  17-May-82
  4         561-2288         B WIRE, GRAY, 22 AWG, 7 X 30           P *   * P FT      0.0080 764  17-May-82
  4         561-2299         B WIRE, WHITE, 22 AWG, 7 X 30          P *   * P FT      0.0080 764  17-May-82
 3          830-0010         O STUD, 1/4 TURN FASTENER           EX X 1 P C P EA      2      449  18-Jan-82
 3          830-0011         O RETAINER, 1/4 TURN                EX X 1 P C P EA      2      449  18-Jan-82
 3          830-0012         O CLIP-ON RECEPTACLE, 1/4 TURN      EX X 1 P C P EA      2      449  18-Jan-82
 3          805-0057         C CLIP, DISK HOLD DOWN #2 A3        RM X 1 P C P EA      1      749  18-Jan-82
 3          830-0014         O FASTENER, RETAINING CLIP          EX X 7 P C P EA      2      449  18-Jan-82
 3          865-0005        MA FOOT, .52HT, SQ                   EX X 7 P C P EA      6      545  18-Jan-82
 3          946-0000         A TAPE, FOAM, DOUBLE SIDED ADHESIVE EX X 1 P B P RL      0.2300 877  18-Jan-82
 3          810-0364         A CHASSIS, PAINTED A3               RM P 1   A P EA      1      559  18-Jan-82
  4         800-0364         C CHASSIS, MACHINED A3              RM P 1   A P EA      1      983  28-Feb-81
   5        815-0364         B BASE, DIECAST CHASSIS A3          RM P 1   * P EA      1      A012 28-Feb-81
 3          908-0003         1 ADHESIVE, RTV #3145 GRAY          EX X 1 P B P EA      0.0100 352  18-Jan-82
 3          815-0087        MC KEYBOARD COVER, APPLEIII          RM P 1 P C P EA      1      A024 18-Jan-82
 3          825-0163         1 LABEL, POWER ON                   EX X 7 P C P EA      1      427  18-Jan-82
 3          430-1005         C SCREW, TAPPING, 4 X 20 .500          X *   C P EA      5      C086 18-Jan-82
 3          825-0321         C LABEL, A3 SERIAL NO. & UL            X *   C P EA      1      A024 18-Jan-82
 3          825-0057         1 LABEL, REAR CONNECTOR, APPLEIII   EX X 7 P C P EA      1      427  18-Jan-82
 3          410-1206         B SCREW, M2.5 X 0.45 X 6MM POZI DR  EX X 1 P C P EA      2      C086 18-Jan-82
 3          410-1410         B SCREW, M3.5 X .6 X 10MM PHMS      EX X 1   C P EA      7      C086 18-Jan-82
 3          860-0020         O WASHER, FLAT M3.5                 EX X 1 P C P EA      3      441  18-Jan-82
 3          825-0066         C LABEL, MODEL NAMEPLATE A3         EX X 7 P C P EA      1      A035 18-Jan-82          09-May-82
 3          699-0031         E POWER SUPPLY, OEM ASTEC A3 (110V) VX A 1 P A P EA      1      877  18-Jan-82
 3          590-0032         A CABLE ASSY, 15" LG, 26 COND RIBBON RC P 1 P B P EA     2      559  18-Jan-82
  4         517-0030         A CONN, 26P SOCKET INSUL. DISPLACEMNT RP P 1 P C P EA    4      482  19-Jan-81
  4         590-0050         B CABLE, FLAT 26 CONDUCTOR          RC P 1 P * P FT      2.5000 C115 19-Jan-81
 3          420-1006         B SCREW, TAP P.H.C.R M3.5X.6X10        X *   * P EA     19      C086 26-Apr-82
 3          610-0011         A SUBASSY, TOP COVER, A3            RM X 1 P C P EA      1      559  18-Jan-82
  4         815-0086        MM TOP COVER, APPLE III              RM P 1 P C P EA      1      C036 19-Jan-81
  4         805-0031         J COVER, PERIPHERAL CARD, APPLEIII  RM P 1 P C P EA      1      A031 19-Jan-81
 3          610-4106         A ASSY,TST,A3 LOGIC FOR 5V RAM         A *   A P EA      1      923  18-Jan-82          26-Apr-82
  4         610-0106         E ASSY,UNTST,A3 LOGIC FOR 5V RAM       A *   A P EA      1      A091 18-Jan-82
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PRINTED 23-Jul-82  13:32              PERSONAL COMPUTER SYSTEMS                     BIL VERSION 29-Mar-79  PAGE    6

EFFECTIVITY DATE: ALL                 I N D E N T E D   B I L L S   O F   M A T E R I A L

  PARENT PART: 610-8156         INACT.FG,256K APPLE III          UM: EA   PROD CODE:     ECN: A116   ASSEMBLY QTY:    1
                                ERC: B   SRCE CODE: A   TYPE: *  ABC: A   PLAN CODE: U   DATE: 08-Jul-82

          COMPONENT         E PART DESCRIPTION                     PR S T S A P      EXTENDED   ECN     START             CLOSE
LEVEL     PART NUMBER       R                                      CD C Y P B L UM   QTY PER    CHG   DATE      S/N     DATE      S/N

   5      050-0047          A SCHEMATIC,MN LOGIC BD A3/5V RAM         D *     * U EA      0      923   18-Jan-82
   5      112-0102          B RES. ARRAY,47 OHM                    RP P 1 P C P EA      5      611   18-Jan-82
   5      306-0011          A IC, 74LS11, TESTED & BURNED-IN          A *   C P EA      1      807   18-Jan-82
    6     305-0011          A IC, 74LS11                           RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0125          A IC, 74LS125, TESTED & BURNED-IN         A *   C P EA      1      807   18-Jan-82
    6     305-0125          A IC, 74LS125                          RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0000          A IC, 74LS00, TESTED & BURNED-IN          A *   C P EA      2      807   18-Jan-82
    6     305-0000          A IC, 74LS00N                          RI P 1 P B P EA      2      442   15-Jul-81
   5      306-0002          A IC, 74LS02, TESTED & BURNED-IN          A *   C P EA      1      807   18-Jan-82
    6     305-0002          A IC, 74LS02N                          RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0004          A IC, 74LS04, TESTED & BURNED-IN          A *   C P EA      1      807   18-Jan-82
    6     305-0004          A IC, 74LS04                           RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0005          A IC, 74LS05, TESTED & BURNED-IN          A *   C P EA      1      807   18-Jan-82
    6     305-0005          A IC, 74LS05                           RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0008          A IC, 74LS08 TESTED & BURNED-IN           A *   C P EA      2      807   18-Jan-82
    6     305-0008          A IC, 74LS08                           RI P 1 P B P EA      2      442   15-Jul-81
   5      308-0010          A IC, 74S10, TESTED & BURNED-IN           A *   C P EA      1      807   18-Jan-82
    6     307-0010          A IC, 74S10                            RI P 1 P B P EA      1      C063  15-Jul-81
   5      306-0020          A IC, 74LS20, TESTED & BURNED-IN          A *   C P EA      1      807   18-Jan-82
    6     305-0020          A IC, 74LS20                           RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0021          A IC, 74LS21, TESTED & BURNED-IN          A *   C P EA      1      807   18-Jan-82
    6     305-0021          A IC, 74LS21                           RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0032          A IC, 74LS32, TESTED & BURNED-IN          A *   C P EA      1      807   18-Jan-82
    6     305-0032          A IC, 74LS32                           RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0051          A IC, 74LS51, TESTED & BURNED-IN          A *   C P EA      2      807   18-Jan-82
    6     305-0051          A IC, 74LS51                           RI P 1 P B P EA      2      442   15-Jul-81
   5      306-0074          A IC, 74LS74, TESTED & BURNED-IN          A *   C P EA      2      807   18-Jan-82
    6     305-0074          A IC, 74LS74                           RI P 1 P B P EA      2      442   15-Jul-81
   5      306-0086          A IC, 74LS86, TESTED & BURNED-IN          A *   C P EA      1      807   18-Jan-82
    6     305-0086          A IC, 74LS86                           RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0138          A IC, 74LS138, TESTED & BURNED-IN         A *   C P EA      3      807   18-Jan-82
    6     305-0138          A IC, 74LS138                          RI P 1 P B P EA      3      442   15-Jul-81
   5      306-0126          A IC, 74LS126, TESTED & BURNED-IN         A *   C P EA      1      807   18-Jan-82
    6     305-0126          A IC, 74LS126                          RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0153          A IC, 74LS153, TESTED & BURNED-IN         A *   C P EA      1      807   18-Jan-82
    6     305-0153          A IC, 74LS153                          RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0157          A IC, 74LS157, TESTED & BURNED-IN         A *   C P EA      1      807   18-Jan-82
    6     305-0157          A IC, 74LS157                          RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0161          A IC, 74LS161, TESTED & BURNED-IN         A *   C P EA      4      807   18-Jan-82
    6     305-0161          A IC, 74LS161                          RI P 1 P B P EA      4      442   15-Jul-81
   5      306-0174          A IC, 74LS174, TESTED & BURNED-IN         A *   C P EA      1      807   18-Jan-82
    6     305-0174          A IC, 74LS174                          RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0139          A IC, 74LS139, TESTED & BURNED-IN         A *   C P EA      2      807   18-Jan-82
    6     305-0139          A IC, 74LS139                          RI P 1 P B P EA      2      442   15-Jul-81
   5      306-0244          A IC, 74LS244, TESTED & BURNED-IN         A *   C P EA      1      807   18-Jan-82
    6     305-0244          A IC, 74LS244                          RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0251          A IC, 74LS251, TESTED & BURNED-IN         A *   C P EA      1      807   18-Jan-82
    6     305-0251          A IC, 74LS251                          RI P 1 P B P EA      1      442   15-Jul-81
   5      306-0257          A IC, 74LS257, TESTED & BURNED-IN         A *   C P EA      3      807   18-Jan-82
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PRINTED 23-Jul-82  13:32              PERSONAL COMPUTER SYSTEMS                        BIL VERSION 29-Mar-79  PAGE    7

EFFECTIVITY DATE: ALL             I N D E N T E D   B I L L S   O F   M A T E R I A L

  PARENT PART: 610-8156        INACT.FQ,256K APPLE III            UM: EA   PROD CODE:     ECN: A116   ASSEMBLY QTY:    1
                               ERC: B   SRCE CODE: A   TYPE: *   ABC: A   PLAN CODE: U   DATE: 08-Jul-82

          COMPONENT     E PART DESCRIPTION                    PR S T S A P       EXTENDED  ECN      START             CLOSE
LEVEL     PART NUMBER   R                                     CD C Y P B L UM    QTY PER   CHG   DATE      S/N     DATE      S/N

  5       306-0283      A IC, 74LS283, TESTED & BURNED-IN        A *   C P EA       1      807   18-Jan-82
   6      305-0283      A IC, 74LS283                         RI P 1 P B P EA       1      442   15-Jul-81
  5       306-0323      A IC, 74LS323, TESTED & BURNED-IN        A *   C P EA       1      807   18-Jan-82
   6      305-0323      A IC, 74LS323                         RI P 1 P B P EA       1      442   15-Jul-81
  5       306-0374      A IC, 74LS374, TESTED & BURNED-IN        A *   C P EA       6      807   18-Jan-82
   6      305-0374      A IC, 74LS374                         RI P 1 P B P EA       6      442   15-Jul-81
  5       306-0399      A IC, 74LS399, TESTED & BURNED-IN        A *   C P EA       2      807   18-Jan-82
   6      305-0399      A IC, 74LS399                         RI P 1 P B P EA       2      442   15-Jul-81
  5       308-0074      A IC, 74S74, TESTED & BURNED-IN          A *   C P EA       3      807   18-Jan-82
   6      307-0074      A IC, 74S74                           RI P 1 P B P EA       3      C063  15-Jul-81
  5       308-0086      A IC, 74S86, TESTED & BURNED-IN          A *   C P EA       2      807   18-Jan-82
   6      307-0086      A IC, 74S86                           RI P 1 P B P EA       2      C063  15-Jul-81
  5       308-0151      A IC, 74S151, TESTED & BURNED-IN         A *   C P EA       1      807   18-Jan-82
   6      307-0151      A IC, 74S151                          RI P 1 P B P EA       1      C063  15-Jul-81
  5       308-0153      A IC, 74S153, TESTED & BURNED-IN         A *   C P EA       4      807   18-Jan-82
   6      307-0153      A IC, 74S153                          RI P 1 P B P EA       4      C063  15-Jul-81
  5       308-0175      A IC, 74S175, TESTED & BURNED-IN         A *   C P EA       1      807   18-Jan-82
   6      307-0175      A IC, 74S175                          RI P 1 P B P EA       1      C063  15-Jul-81
  5       308-0195      A IC, 74S195, TESTED & BURNED-IN         A *   C P EA       1      807   18-Jan-82
   6      307-0195      A IC, 74S195 OR 93S00                 RI P 1 P B P EA       1      C063  15-Jul-81
  5       308-0257      A IC, 74S257, TESTED & BURNED-IN         A *   C P EA       4      807   18-Jan-82
   6      307-0257      A IC, 74S257                          RI P 1 P B P EA       4      C063  15-Jul-81
  5       342-0032      A IC VIDEO CONTROL TST & BRN IN          A *   C P EA       1      831   18-Jan-82
   6      341-0032      O ROM, VIDEO CONTROL                  RL P 1 P C P EA       1      449   10-Aug-81
  5       302-0166      A IC, 74166, TESTED & BURNED-IN          A *   C P EA       1      807   18-Jan-82
   6      301-0166      A IC, 74166                           RI P 1 P B P EA       1      C063  15-Jul-81
  5       369-6502      B IC MICRO 6502B 3MHZ TEST&BURN-IN       A *   C P EA       1      A098  18-Jan-82
   6      368-6502     ?0 IC/MICROPROCESSOR 6502B 3MHz        RI P 1 P C P EA       1      458   31-Aug-81
  5       354-0380      A IC LM380 AUDIO PWR AMP TST & BRN IN    A *   C P EA       1      831   18-Jan-82
   6      353-0380      O IC, LM380 AUDIO POWER AMPLIFIER     RI P 1 P C P EA       1      449   10-Aug-81
  5       342-0030     MA IC ROM SYNCHROM WITH BURN-IN           A *   C P EA       1      831   18-Jan-82
   6      341-0030      O ROM, SYNCHROM                       RL P 1 P C P EA       1      449   10-Aug-81
  5       342-0031     MA IC. ROM BOOT WITH BURN-IN              A *   C P EA       1      831   18-Jan-82
   6      341-0031      1 ROM, BOOT                           RL P 1 P C P EA       1      532   10-Aug-81
  5       338-6522      A IC 6522 I/F ADAPTER TEST&BURN-IN       A *   C P EA       2      877   18-Jan-82
   6      337-6522     MO IC, 6522 VERSATILE I/F ADAPTER      RL P 1 P B P EA       2      449   31-Aug-81
  5       338-0002      A ASYN COMM INT 6551A TST & BRN IN       A *   C P EA       1      877   18-Jan-82
   6      337-0002      A IC,6551A ASYNC.COMM.I/F ADAP.  SELE.   P *   C P EA       1      736   31-Aug-81
  5       316-8304      A IC 8304B 8-BIT TRI-ST. TST&BRN IN      A *   C P EA       1      831   18-Jan-82
   6      315-8304      O IC, 8304B 8-BIT TRI-STATE           RI P 1 P B P EA       1      449   10-Aug-81
  5       330-0556      A IC 556 DUAL TIMER TEST&BURN-IN         A *   C P EA       3      831   18-Jan-82
   6      329-0556      O IC, 556 DUAL TIMER                  RI P 1 P C P EA       3      449   10-Aug-81
  5       302-9334      B IC, 9334, TESTED & BURNED-IN           A *   C P EA       3      802   18-Jan-82
   6      301-9334      A IC, 9334                            RI P 1 P B P EA       3      C063  20-Jul-81
   6      301-0259      A IC, 74259                           EX P 7 P B P EA       0      C063  20-Jul-81
  5       360-1488      A IC 1488 QUAD LINE DRIVER TST&BRN-IN    A *   C P EA       1      831   18-Jan-82
   6      359-1488      O IC, 1488 QUAD LINE DRIVER           RI P 1 P C P EA       1      449   10-Aug-81
  5       356-9708      A IC 9708 6-CH 8-BIT TESTED & BRN IN     A *   C P EA       1      831   18-Jan-82
   6      355-9708      O IC, 9708 6-CH. 8-BIT A TO D         RI P 1 P B P EA       1      449   10-Aug-81
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PRINTED 23-Jul-82  13:33             PERSONAL COMPUTER SYSTEMS                         BIL VERSION 29-Mar-79  PAGE    8

EFFECTIVITY DATE: ALL              I N D E N T E D  B I L L S  O F  M A T E R I A L

 PARENT PART: 610-8156           INACT.FG,256K APPLE III           UM: EA   PROD CODE:      ECN: A116   ASSEMBLY QTY:     1
                                 ERC: B   SRCE CODE: A   TYPE: *   ABC: A   PLAN CODE: U    DATE: 08-Jul-82

             COMPONENT        E PART DESCRIPTION                  PR S T S A P      EXTENDED  ECN     START          CLOSE
LEVEL        PART NUMBER      R                                   CD C Y P B L UM   QTY PER   CHG  DATE      S/N   DATE     S/N

    6        359-1489         O IC, 1489 LINE RECEIVER            RI P 1 P C P EA      1      449  10-Aug-81
   5         372-3904         A TRANSISTOR,NPN SW.&AMP. 2N3904    RP P 1 P C P EA      4      C026 18-Jan-82
   5         111-0003         O RES ARRAY D/A CONVERTER 7 RES 8 PIN RP P 1 P C P EA    1      426  18-Jan-82
   5         111-0025         A RESISTOR ARRAY, SIP 7 RES, SPECIAL   P *   * P EA      1      923  18-Jan-82
   5         135-9101         A CAP,.1uF +80-20% Z5U/Y5V 50V      RP P 1 P C P EA     41      433  18-Jan-82
   5         151-5501         B CHOKE, 27uH 10%                   RP P 1 P B P EA      1      479  18-Jan-82
   5         342-0028         A IC.PROM,STATE MACH.P6A W/BURN-IN     A *   C P EA      1      831  18-Jan-82
    6        341-0028         1 IC, PROM, STATE MACHINE, P6A      RL A 1 P C P EA      1      454  10-Aug-81
     7       335-0471         A PROM,74S471                       RL P 1 P B P EA      1
   5         334-0005         A IC 1024 X 4 STATIC RAM TST & BRN IN  A *   C P EA      2      877  18-Jan-82
    6        334-2114         O IC, 1024 X 4 STATIC RAM 2114      RL P 1 P C P EA      2      449  31-Aug-81
   5         306-0133         A IC, 74LS133, TESTED & BURNED-IN      A *   C P EA      2      807  18-Jan-82
    6        305-0133         A IC, 74LS133                       RI P 1 P B P EA      2      442  15-Jul-81
   5         820-0043         O PCB, MAIN LOGIC BD #2 A3          RP P 7 P A P EA      1      503  18-Jan-82
   5         101-4112         A RES, 1/4W 5% 1.1K OHM             RP P 1 P C P EA      2      426  18-Jan-82
   5         101-4104         A RES 1/4W 5% 100K OHM              RP P 1 P C P EA      3      426  18-Jan-82
   5         126-5102         O CAP, 10uF 16V                     RP P 1 P C P EA      2      426  18-Jan-82
   5         197-0001         B CRYSTAL, 14.318630 MHz            RI P 1 P C P EA      1      487  18-Jan-82
   5         101-4102         A RES 1/4W 5% 1K OHM                RP P 1 P C P EA     15      426  18-Jan-82
   5         126-4102         O CAP, 1uF 50V                      RP P 1 P C P EA      3      426  18-Jan-82
   5         101-4225         A RES 1/4W 5% 2.2 MEG OHM           RP P 1 P C P EA      1      426  18-Jan-82
   5         131-5401         O CAP, 20pF 5% NPO 50V              RP P 1 P C P EA      1      426  18-Jan-82
   5         372-4258         A TRANSISTOR, PNP HIGH SPD.SW. 2N4258 RP P 1 P C P EA    2      C026 18-Jan-82
   5         101-4335         A RES 1/4W 5% 3.3 MEG OHM           RP P 1 P C P EA      2      426  18-Jan-82
   5         197-0004         O CRYSTAL, TUNING FORK 32.768 KHz   RI P 1 P C P EA      1      449  18-Jan-82
   5         101-4302         A RES 1/4W 5% 3K OHM                RP P 1 P C P EA      5      426  18-Jan-82
   5         101-4470         A RES 1/4W 5% 47 OHM                RP P 1 P C P EA      3      426  18-Jan-82
   5         101-4474         A RES 1/4W 5% 470K OHM              RP P 1 P C P EA      1      426  18-Jan-82
   5         101-4473         A RES 1/4W 5% 47K OHM               RP P 1 P C P EA      2      426  18-Jan-82
   5         515-0053        MB CONN, STRAIGHT HEADER 2 PIN       RP P 1 P C P EA      1      532  18-Jan-82
   5         371-4148         A DIODE, 1N4148                     RP P 1 P C P EA      5      731  18-Jan-82
   5         519-0011         O CONNECTOR, 9 PIN D                RC P 1 P C P EA      2      467  18-Jan-82
   5         519-0038         A CONN. 15 PIN D RT ANGLE PC MOUNT  RC P 1   C P EA      1      725  18-Jan-82
   5         515-0001         A JACK, PHONO RT ANG (MON) NTT 333-15 RP P 1 P C P EA    1      784  18-Jan-82
   5         515-0002         O JACK, PHONE                       RP P 1 P C P EA      1      467  18-Jan-82
   5         519-0014         O CONNECTOR,  HEADER 25 PIN         RC P 1 P C P EA      2      467  18-Jan-82
   5         519-0016         A CONN, 26 PIN HEADER W/O MTG EARS  RC P 1 P C P EA      2      523  18-Jan-82
   5         519-0017         A CONN, 26 PIN HEADER W/MTG EARS    RC P 1 P C P EA      1      523  18-Jan-82
   5         155-5102         A COIL, 10UH RADIAL                    P *   B P EA      2      DC44 18-Jan-82
   5         519-0018         O CONNECTOR, 25 PIN D               RC P 1 P C P EA      1      467  18-Jan-82
   5         378-0001         B LED, RED                          RP P 1 P C P EA      1      DC53 18-Jan-82
   5         511-1401         C SOCKET, IC 14 PIN                 RP P 1 P C P EA     30      799  18-Jan-82
   5         511-1601         C SOCKET, IC 16 PIN                 RP P 1 P C P EA     36      799  18-Jan-82
   5         511-1801         C SOCKET, IC 18 PIN                 RP P 1 P C P EA      9      799  18-Jan-82
   5         511-2001         C SOCKET, IC 20 PIN                 RP P 1 P C P EA     11      799  18-Jan-82
   5         511-2401         C SOCKET, IC 24 PIN                 RP P 1 P C P EA      4      799  18-Jan-82
   5         511-2801         C SOCKET, IC 28 PIN                 RP P 1 P C P EA      1      799  18-Jan-82
   5         511-4001         C SOCKET, IC 40 PIN                 RP P 1 P C P EA      4      799  18-Jan-82
   5         342-0056         A IC. PROM,CASB65.1 WITH BURN-IN       A *   C P EA      1      831  18-Jan-82
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PRINTED 23-Jul-82  13:34                  PERSONAL COMPUTER SYSTEMS                          BIL VERSION 29-Mar-79  PAGE    9

EFFECTIVITY DATE: ALL            I N D E N T E D   B I L L S   O F   M A T E R I A L

  PARENT PART: 610-8156          INACT.FG,256K APPLE III              UM: EA   PROD CODE:      ECN: A116   ASSEMBLY QTY:     1
                                 ERC: B   SRCE CODE: A   TYPE: *      ABC: A   PLAN CODE: U    DATE: 08-Jul-82

                COMPONENT       E PART DESCRIPTION                    PR S T S A P         EXTENDED   ECN      START               CLOSE
LEVEL           PART NUMBER     R                                     CD C Y P B L UM      QTY PER    CHG    DATE        S/N       DATE        S/N

      7         335-0003        O PROM, 1024 X 4 UNPROGRAMMED         RL P 1 P B P EA         1       SARA 27-Oct-80
    5           342-0043        A IC PROM U174 WITH BURN-IN              A *   C P EA         1       831  18-Jan-82
     6          341-0043        O PROM, 1024 X 4 U174                 RL A 1 P C P EA         1       449  10-Aug-81
      7         335-0003        O PROM, 1024 X 4 UNPROGRAMMED         RL P 1 P B P EA         1       SARA
    5           342-0045        A IC.PROM,U176.2 WITH BURN-IN            A *   C P EA         1       831  18-Jan-82
     6          341-0045        O PROM, 1024 X 4 U176.2               RL A 1 P C P EA         1       449  10-Aug-81
      7         335-0003        O PROM, 1024 X 4 UNPROGRAMMED         RL P 1 P B P EA         1       SARA
    5           342-0046        A IC.PROM, U180 WITH BURN-IN             A *   C P EA         1       831  18-Jan-82
     6          341-0046        O PROM, 1024 X 4 U180                 RL A 1 P B P EA         1       449  10-Aug-81
      7         335-0003        O PROM, 1024 X 4 UNPROGRAMMED         RL P 1 P B P EA         1       SARA
    5           342-0055       MA IC. PROM, U175-65 WITH BURN-IN         A *   C P EA         1       831  18-Jan-82
     6          341-0055        A IC, PROM U175-65                    RL A 1 P C P EA         1       503  10-Aug-81
      7         335-0003        O PROM, 1024 X 4 UNPROGRAMMED         RL P 1 P B P EA         1       SARA 27-Oct-80
    5           513-5002        D CONNECTOR, EDGE 25/50 PIN (NO TABS) RP P 1 P C P EA         4       760  18-Jan-82
    5           515-0103        A HEADER, RIGHT ANGLE 10 PINS            P *   C P EA         1       877  18-Jan-82
    5           306-0260        A IC, 74LS260, TESTED & BURNED-IN        A *   C P EA         1       807  18-Jan-82
     6          305-0260        A IC, 74LS260                         RI P 1 P B P EA         1       442  15-Jul-81
    5           131-5101        O CAP, 10pF 10% NPO 50V               RP P 1 P C P EA         1       426  18-Jan-82
    5           126-6404        A CAP, 220UF 16V                         * *   * * EA         4       C103 24-May-82
    5           151-5101        O CHOKE, 10uH 10%                     RP P 1 P B P EA         2       442  18-Jan-82
    5           132-6401        O CAP, 220pF 10% Z5F 50V              RP P 1 P C P EA         4       426  18-Jan-82
    5           372-3906        A TRANSISTOR,PNP SW.&AMP. 2N3906      RP P 1 P C P EA         1       C026 18-Jan-82
    5           101-4750        A RES 1/4W 5% 75 OHM                  RP P 1 P C P EA         3       426  18-Jan-82
    5           101-4152        A RES 1/4W 5% 1.5K OHM                RP P 1 P C P EA         2       426  18-Jan-82
    5           101-4682        A RS 1/4W 5% 6.8K OHM                 RP P 1 P C P EA         2       426  18-Jan-82
    5           519-0032        O CONN, 10 PIN FRICTION LOCK          RC P 1 P C P EA         1       442  18-Jan-82
    5           306-0132        A IC, 74LS132, TESTED & BURNED-IN        A *   C P EA         1       807  18-Jan-82
     6          305-0132        A IC, 74LS132                         RI P 1 P B P EA         1       442  15-Jul-81
    5           375-0005        O DIODE, 1N5712 SCHOTTKY BARRIER      RP P 1 P C P EA         1       449  18-Jan-82
    5           111-0018        O RES ARRAY 7 X 330 OHM               RP P 1 P C P EA         1       426  18-Jan-82
    5           111-0017        O RES ARRAY 9 X 3.3K OHM              RP P 1 P C P EA         2       426  18-Jan-82
    5           101-4330        A RES 1/4W 5% 33 OHM                  RP P 1 P C P EA         4       426  18-Jan-82
    5           101-4101        A RES 1/4W 5% 100 OHM                 RP P 1 P C P EA         2       426  18-Jan-82
    5           111-0014        O RES ARRAY 9 X 1K OHM                RP P 1 P C P EA         2       426  18-Jan-82
    5           101-4472        A RES 1/4W 5% 4.7K OHM                RP P 1 P C P EA         1       426  18-Jan-82
    5           101-4153        A RES 1/4W 5% 15K OHM                 RP P 1 P C P EA         4       426  18-Jan-82
    5           101-4241        A RES 1/4W 5% 240 OHM                 RP P 1 P C P EA         1       426  18-Jan-82
    5           101-4105        A RES, 1/4W 5% 1M OHM                 RP P 1 P C P EA         2       426  18-Jan-82
    5           101-4301        A RES, 1/4W 5% 300 OHM                RP P 1 P C P EA         3       426  18-Jan-82
    5           101-4471        A RES 1/4W 5% 470 OHM                 RP P 1 P C P EA         3       426  18-Jan-82
    5           125-5401        A CAP, 22uF 16V                       RP P 1 P C P EA         1       433  18-Jan-82
    5           511-0801        C SOCKET, IC 8 PIN                    RP P 1 P C P EA         1       799  18-Jan-82
    5           132-6101        O CAP, 100pF 20% Z5F 50V              RP P 1 P C P EA         3       426  18-Jan-82
    5           101-4181        A RES, 1/4W 5% 180 OHM                RP P 1 P C P EA         1       426  18-Jan-82
    5           119-2101       MA CAP, .01uF 10% 100V                 RP P 1 P C P EA         1       449  18-Jan-82
    5           101-4125        A RES 1/4W 5% 1.2 MEG OHM             RP P 1 P C P EA         1       426  18-Jan-82
    5           133-2401        B CAP, .022uF 20% Y5P 25V             RP P 1 P C P EA         2       433  18-Jan-82
    5           138-0002       MO CAP,VAR  CERAMIC TRIMMER 3.8/4.0F   RP P 1 P C P EA         1       449  18-Jan-82
    5           111-0019        O RES ARRAY 5 X 1K OHM                RP P 1 P C P EA         3       426  18-Jan-82
    5                                                                    A       P EA         1
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PRINTED 23-Jul-82  13:34                      PERSONAL COMPUTER SYSTEMS                     BIL VERSION 29-Mar-79  PAGE  10

EFFECTIVITY DATE: ALL              I N D E N T E D   B I L L S   O F   M A T E R I A L

 PARENT PART: 610-8156       INACT.FQ,256K APPLE III            UM: EA   PROD CODE:      ECN: A116   ASSEMBLY QTY:   1
                             ERC: B   SRCE CODE: A   TYPE: *    ABC: A   PLAN CODE: U    DATE: 08-Jul-82

        COMPONENT     E PART DESCRIPTION                       PR S T S A P       EXTENDED   ECN      START                CLOSE
LEVEL   PART NUMBER   R                                        CD C Y P B L UM    QTY PER    CHG   DATE       S/N     DATE       S/N

    6   307-0374      A IC, 74S374                             RI P 1 P B P EA         1     C063 15-Jul-81
   5    308-0000      A IC, 74S00, TESTED & BURNED-IN             A *   C P EA         1     807  18-Jan-82
    6   307-0000      A IC, 74S00 QUAD NAND GATE               RI P 5 P B P EA         1     C063 15-Jul-81
   5    342-0035     MA IC ROM KYBD ENC. A3 BRN-IN & TST          A *   C P EA         1     886  18-Jan-82
    6   341-0035      B ROM, KEYBOARD ENCODER                  RL P 1 P C P EA         1     683  21-Sep-81
   5    111-0001      O RES ARRAY 7 X 1K OHMS                  RP P 1 P C P EA         3     426  18-Jan-82
   5    131-5701      O CAP, 47pF 5% N470 50V                  RP P 1 P C P EA         1     426  18-Jan-82
   5    112-0001      B RES,INDIV. NTWRK. 68 OHM/5RES/10PIN    RP P 1 P C P EA         1     609  18-Jan-82
   5    376-0001      A TRANSISTOR, MPS-U51                    RP P 1 P C P EA         1     C111 18-Jan-82
   5    119-2701      A CAP, .047uF 10% 100V                   RP P 1 P C P EA         1     DC3  18-Jan-82
   5    101-4103      A RES 1/4W 5% 10K OHM                    RP P 1 P C P EA         2     426  18-Jan-82
   5    101-4270      A RES 1/4W 5% 27 OHM                     RP P 1 P C P EA         3     426  18-Jan-82
   5    101-4121      A RES 1/4W 5% 120 OHMS                   RP P 1 P C P EA         4     426  18-Jan-82
   5    750-0006      B BUS BAR, CAPACITIVE .2uF               RP P 1 P C P EA         7     503  18-Jan-82
   5    562-2405      A WIRE, #24 KYNAR GREEN SOLID            EX X 7 P C P FT         4     503  18-Jan-82
   5    101-4432      A RES 1/4W 5% 4.3K OHM                   RP P 1 P C P EA         1     426  18-Jan-82
   5    111-0006      O RES,ARRAY SPECIAL 8R, 9P               RP P 1 P C P EA         1     426  18-Jan-82
   5    831-0100      A RIVET, PLASTIC .125                       X *   C P EA         8     778  18-Jan-82
   5    306-0014      A IC, 74LS14, TESTED & BURNED-IN            A *   C P EA         1     807  18-Jan-82
    6   305-0014      A IC, 74LS14                             RI P 1 P B P EA         1     442  15-Jul-81
   5    136-3101     MC CAP, .1UF 10% XR7 50V                     P *   C P EA         6     C082 18-Jan-82
   5    342-0061      A I.C. PROM RAS65 WITH BURN-IN              A *   C P EA         1     867  18-Jan-82
    6   341-0061      A IC/PROM, RAS65                         RL P 1   C P EA         1     665  24-Aug-81
   5    342-0063      A IC. PROM CASB256 WITH BURN-IN             A *   C P EA         1     867  18-Jan-82
    6   341-0063      A IC/PROM, CASB256                       RL P 1   C P EA         1     665  24-Aug-81
   5    825-0233      A LABEL, PCB SERIALIZATION                  P *   * U EA         1     923  18-Jan-82
   5    942-0197      A BAG, POLY 12X18 ANTI-STAT                 P *   * P EA         1     A024 26-Apr-82
   5    875-0005      A CONTACT PROTECTOR                         * *   * * EA         2     C132 26-Jul-82
   5    126-6402      O CAP, 220uF 16V                         RP P 1 P C P EA         4     426  18-Jan-82              23-May-82
 3      610-4256      A ASSY, PCB, TST, 5V MEMORY 256K A3         A *   A P EA         1     714  18-Jan-82              26-Apr-82
 3      805-0099      B BOTTOM COVER,MAIN BOARD 2 A3              P *   C P EA         1     972  18-Jan-82              26-Apr-82
  4     860-0018      A STANDOFF M3.5X0.6 BLD THD .200" LG     EX X 1 P C P EA         6     559  07-Nov-81
 3      865-0007      A BUMPER, HEMISPHERE .2" HIGH            EX X 7   C P EA        11     661  18-Jan-82              26-Apr-82
 3      830-0018      O CLAMP, C-TYPE, FLAT CABLE              EX X 7 P C P EA         1     445  18-Jan-82
 3      000-0001      A NOT USED THIS ASSEMBLY                    D *   D U EA         0     NONE 18-Jan-82
 3      865-0006      A BUMPER,SQ. .23"                        EX X 7   C P EA         2     661  18-Jan-82
 3      825-0207      A LABEL, FCC NON COMPLIANCE APPLE 3      EX X 7 P C P EA         1     559  18-Jan-82
 3      825-0312      A LABEL, WARNING SLOT A3                    X *   C P EA         1     793  18-Jan-82
 3      610-5103      C INACTIVE,SUBASSY,KEYBOARD APPLE III    WS A 1 P A P EA         1     948  18-Jan-82              20-Jan-82
  4     610-4103      O INACTIVE,ASSY,PCB,TST KEYBOARD A3      VX A 1 P A P EA         1     948  05-Jun-80              21-Jan-82
   5    610-0103        INACTIVE,ASSY,PCB,UNTST,KBD A3         UN A 1 P A P EA         1     948                         21-Jan-82
    6   820-0025        PCB, KEYBOARD (SARA)                   RP P 1 P A P EA         1     SARA                        21-Jan-82
    6   710-0001      O LAMP 02-1876-01                        EX P 7 P C P EA         1     352                         21-Jan-82
    6   705-0009      A SWITCH,END ACTUATED PUSH BUTTON        RP P 1 P C P EA         1     P150                        21-Jan-82
    6   515-0014      O CONN, 26 PIN HEADER                    RP P 1 P C P EA         1     442                         21-Jan-82
    6   705-0011        SWITCH, DC51 ALT ACTION (SARA)         RP P 1 P C P EA         1     SARA                        21-Jan-82
    6   705-0012        SWITCH, DC51 DUAL ACTION (SARA)        RP P 1 P C P EA         4     SARA                        21-Jan-82
    6   705-0004      O SWITCH DC51-31                         RP P 1 P C P EA        69     352                         21-Jan-82
  4     610-0197      O SUBASSY, KEYCAPS, COMPLETE SET A3      WS N 1 P B P EA         1     441  05-Jun-80              21-Jan-82
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PRINTED 23-Jul-82  13:35               PERSONAL COMPUTER SYSTEMS                        BIL VERSION 29-Mar-79  PAGE   11

EFFECTIVITY DATE: ALL              I N D E N T E D   B I L L S   O F   M A T E R I A L

 PARENT PART: 610-8156          INACT.FG,256K APPLE III         UM: EA   PROD CODE:      ECN: A116   ASSEMBLY QTY:    1
                                ERC: B   SRCE CODE: A   TYPE: *  ABC: A   PLAN CODE: U   DATE: 08-Jul-82

           COMPONENT      E PART DESCRIPTION                 PR S T S A P      EXTENDED   ECN      START             CLOSE
 LEVEL     PART NUMBER    R                                  CD C Y P B L UM   QTY PER    CHG   DATE       S/N    DATE      S/N

   5       815-0088       O KEY CAP, APPLE 3, ESCAPE         RM P 1   * P EA      1       441   05-Jun-80
   5       815-0089       O KEY CAP, APPLE 3, ! / 1          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0090       O KEY CAP, APPLE 3, @ / 2          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0091       O KEY CAP, APPLE 3, # / 3          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0092       O KEY CAP, APPLE 3, $ / 4          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0093       O KEY CAP, APPLE 3, % / 5          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0094       O KEY CAP, APPLE 3, ^ / 6          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0095       O KEY CAP, APPLE 3, & / 7          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0096       O KEY CAP, APPLE 3, * / 8          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0097       O KEY CAP, APPLE 3, ( / 9          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0098       O KEY CAP, APPLE 3, ) / 0          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0099       O KEY CAP, APPLE 3, _ / -          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0100       O KEY CAP, APPLE 3, + / =          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0101       O KEY CAP, APPLE 3, : / \          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0102       O KEY CAP, APPLE 3, 7              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0103       O KEY CAP, APPLE 3, 8              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0104       O KEY CAP, APPLE 3, 9              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0105       O KEY CAP, APPLE 3, TAB            RM P 1   * P EA      1       441   05-Jun-80
   5       815-0106       O KEY CAP, APPLE 3, Q              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0107       O KEY CAP, APPLE 3, W              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0108       O KEY CAP, APPLE 3, E              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0109       O KEY CAP, APPLE 3, R              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0110       O KEY CAP, APPLE 3, T              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0111       O KEY CAP, APPLE 3, Y              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0112       O KEY CAP, APPLE 3, U              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0113       O KEY CAP, APPLE 3, I              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0114       O KEY CAP, APPLE 3, O              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0115       O KEY CAP, APPLE 3, P              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0116       O KEY CAP, APPLE3, { / [           RM P 1   * P EA      1       441   05-Jun-80
   5       815-0117       O KEY CAP, APPLE 3, } / ]          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0118       O KEY CAP, APPLE 3, ~ / `          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0119       O KEY CAP, APPLE 3, 4              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0120       O KEY CAP, APPLE 3, 5 (W/SENSOR)   RM P 1   * P EA      1       441   05-Jun-80
   5       815-0121       O KEY CAP, APPLE 3, 6              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0122       O KEY CAP, APPLE 3, CONTROL        RM P 1   * P EA      1       441   05-Jun-80
   5       815-0123       O KEY CAP, APPLE 3, A              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0124       O KEY CAP, APPLE 3, S              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0125       O KEY CAP, APPLE 3, D (W SENSOR)   RM P 1   * P EA      1       441   05-Jun-80
   5       815-0126       O KEY CAP, APPLE 3, F              EX P 1   * P EA      1       441   05-Jun-80
   5       815-0127       O KEY CAP, APPLE 3, G              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0128       O KEY CAP, APPLE 3, H              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0129       O KEY CAP, APPLE 3, J              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0130       O KEY CAP, APPLE 3, K (W SENSOR)   RM P 1   * P EA      1       441   05-Jun-80
   5       815-0131       O KEY CAP, APPLE 3, L              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0132       O KEY CAP, APPLE 3, : / ;          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0133       O KEY CAP, APPLE 3, " / '          RM P 1   * P EA      1       441   05-Jun-80
   5       815-0134       O KEY CAP, APPLE 3, RETURN         RM P 1   * P EA      1       441   05-Jun-80
   5       815-0135       O KEY CAP, APPLE 3, 1              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0136       O KEY CAP, APPLE 3, 2              RM P 1   * P EA      1       441   05-Jun-80
   5       815-0137       O KEY CAP, APPLE 3, 3              RM P 1     P EA      1
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EFFECTIVITY DATE: ALL                    I N D E N T E D  B I L L S  O F  M A T E R I A L

 PARENT PART: 610-8156           INACT.FQ.256K APPLE III             UM: EA   PROD CODE:      ECN: A116   ASSEMBLY QTY:     1
                                 ERC: B    SRCE CODE: A   TYPE: *    ABC: A   PLAN CODE: U    DATE: 08-Jul-82

             COMPONENT       E PART DESCRIPTION                    PR S T S A P       EXTENDED  ECN      START             CLOSE
LEVEL        PART NUMBER     R                                     CD C Y P B L UM    QTY PER   CHG    DATE       S/N    DATE      S/N

   5         815-0138        0 KEY CAP, APPLE 3, SHIFT             RM P 1   * P EA       1      441  05-Jun-80
   5         815-0139        0 KEY CAP, APPLE 3, Z                 RM P 1   * P EA       1      441  05-Jun-80
   5         815-0140        0 KEY CAP, APPLE 3, X                 RM P 1   * P EA       1      441  05-Jun-80
   5         815-0141        0 KEY CAP, APPLE 3, C                 RM P 1   * P EA       1      441  05-Jun-80
   5         815-0142        0 KEY CAP, APPLE 3, V                 RM P 1   * P EA       1      441  05-Jun-80
   5         815-0143        0 KEY CAP, APPLE 3, B                 RM P 1   * P EA       1      441  05-Jun-80
   5         815-0144        0 KEY CAP, APPLE 3, N                 RM P 1   * P EA       1      441  05-Jun-80
   5         815-0145        0 KEY CAP, APPLE 3, M                 RM P 1   * P EA       1      441  05-Jun-80
   5         815-0146        0 KEY CAP, APPLE 3, < / ,             RM P 1   * P EA       1      441  05-Jun-80
   5         815-0147        0 KEY CAP, APPLE 3, > / .             RM P 1   * P EA       1      441  05-Jun-80
   5         815-0148        0 KEY CAP, APPLE 3, ? / /             RM P 1   * P EA       1      441  05-Jun-80
   5         815-0149        0 KEY CAP, APPLE 3, SHIFT             RM P 1   * P EA       1      441  05-Jun-80
   5         815-0150        0 KEY CAP, APPLE 3, ARROW UP          RM P 1   * P EA       1      441  05-Jun-80
   5         815-0151        0 KEY CAP, APPLE 3, 0 (ZERO)          RM P 1   * P EA       1      441  05-Jun-80
   5         815-0152        0 KEY CAP, APPLE 3, . (DECIMAL)       RM P 1   * P EA       1      441  05-Jun-80
   5         815-0153        0 KEY CAP, APPLE 3, ALPHA LOCK        RM P 1   * P EA       1      441  05-Jun-80
   5         815-0154        0 KEY CAP, APPLE 3, APPLE 1           RM P 1   * P EA       1      441  05-Jun-80
   5         815-0155        0 KEY CAP, APPLE 3, APPLE 2           RM P 1   * P EA       1      441  05-Jun-80
   5         815-0156        0 KEY CAP, APPLE 3, SPACE BAR         RM P 1   * P EA       1      441  05-Jun-80
   5         815-0157        0 KEY CAP, APPLE 3, ARROW LEFT        RM P 1   * P EA       1      441  05-Jun-80
   5         815-0158        0 KEY CAP, APPLE 3, ARROW RIGHT       RM P 1   * P EA       1      441  05-Jun-80
   5         815-0159        0 KEY CAP, APPLE 3, ARROW DOWN        RM P 1   * P EA       1      441  05-Jun-80
   5         815-0160        0 KEY CAP, APPLE 3, - (MINUS)         RM P 1   * P EA       1      441  05-Jun-80
   5         815-0161        0 KEY CAP, APPLE 3, ENTER             RM P 1   * P EA       1      441  05-Jun-80
   5         815-0163        3 RESET KEY, APPLEIII                 RM P 1   * P EA       1      427  05-Jun-80
   5         815-0179        1 SPACER, RESET SWITCH A3             RM P 1 P C P EA       1      427  05-Jun-80
   5         062-0032D       0 DWG, KEY CAP 1 SPACE 17 DEG         EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0033D       0 DWG, KEY CAP 1 SPACE                EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0034D       0 DWG, KEY CAP 1 SPACE 10 DEG         EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0036D       0 DWG, KEY CAP 1 SPACE W/BUMP         EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0037D       0 DWG, KEY CAP 1 SPACE W/BUMP 5 DEG   EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0038D       0 DWG, KEY CAP 1-1/2 SPACE            EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0039D       0 DWG, KEY CAP 1-1/4 SPACE 17 DEG     EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0040D       0 DWG, KEY CAP 1-1/2 SPACE 5 DEG      EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0041D       0 DWG, KEY CAP 1-3/4 SPACE 10 DEG     EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0042D       0 DWG, KEY CAP 2 SPACE 10 DEG         EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0043D       0 DWG, KEY CAP 2 SPACE 17 DEG         EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0044D       0 DWG, KEY CAP 2-1/4 SPACE 17 DEG     EX D 7 S * U EA       0      441  05-Jun-80
   5         062-0049D       0 DWG, KEY CAP 6-1/2 SPACE            EX D 7 S * U EA       0      441  05-Jun-80
  3          000-0003        A NOT USED THIS ASSEMBLY                 D *   * U EA       0      NONE 26-Apr-82
  3          000-0004        A NOT USED THIS ASSEMBLY                 D *   * U EA       0      NONE 26-Apr-82
  3          000-0005        A NOT USED THIS ASSEMBLY                 D *   * U EA       0      NONE 26-Apr-82
  3          000-0006        A NOT USED THIS ASSEMBLY                 * *   * U EA       0      NONE 26-Apr-82
  3          000-0007        A NOT USED THIS ASSEMBLY                 * *   * U EA       0      NONE 26-Apr-82
  3          825-0354        A LABEL, NOMEX PAPER                     P *   * U EA       1      A024 26-Apr-82
  3          914-0028        A CARD, CARRIAGE LOCK                    P *   * P EA       1      816  26-Apr-82
  3          825-0357        A LABEL, 256K                            X *   * P EA       1      A024 26-Apr-82
  3          610-5156        A SUBASSY,A3 PAN,LOGIC & MEM BD 256K     A *   A P EA       1      A024 26-Apr-82
   4         610-5129D       A DWG,SUBASSY A3 PAN,LOGIC & MEM BD.     * *   * * EA       0      A024 26-Apr-82
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EFFECTIVITY DATE: ALL                 I N D E N T E D   B I L L S   O F   M A T E R I A L

  PARENT PART:  610-8156        INACT.FG,256K APPLE III           UM:  EA    PROD CODE:      ECN:  A116   ASSEMBLY QTY:     1
                                ERC:  B   SRCE CODE:  A   TYPE:  *   ABC:  A    PLAN CODE:  U   DATE:  08-Jul-82

           COMPONENT      E PART DESCRIPTION                     PR S T S A P       EXTENDED   ECN      START                CLOSE
LEVEL      PART NUMBER    R                                      CD C Y P B L UM     QTY PER   CHG   DATE        S/N      DATE        S/N

   5       610-0106       E ASSY,UNTST,A3 LOGIC FOR 5V RAM          A *   A P EA         1     A091 18-Jan-82
    6      610-0106D      E DWG,ASSY,UNT.A3 LOGIC FOR 5V RAM        * *   * * EA         0     A091 26-Jul-82
    6      050-0047       A SCHEMATIC,MN LOGIC BD A3/5V RAM         D *     * U EA       0     923  18-Jan-82
    6      112-0102       B RES. ARRAY,47 OHM                    RP P 1 P C P EA         5     611  18-Jan-82
    6      306-0011       A IC, 74LS11, TESTED & BURNED-IN          A *   C P EA         1     807  18-Jan-82
     7     305-0011       A IC, 74LS11                           RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0125       A IC, 74LS125, TESTED & BURNED-IN         A *   C P EA         1     807  18-Jan-82
     7     305-0125       A IC, 74LS125                          RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0000       A IC, 74LS00, TESTED & BURNED-IN          A *   C P EA         2     807  18-Jan-82
     7     305-0000       A IC, 74LS00N                          RI P 1 P B P EA         2     442  15-Jul-81
    6      306-0002       A IC, 74LS02, TESTED & BURNED-IN          A *   C P EA         1     807  18-Jan-82
     7     305-0002       A IC, 74LS02N                          RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0004       A IC, 74LS04, TESTED & BURNED-IN          A *   C P EA         1     807  18-Jan-82
     7     305-0004       A IC, 74LS04                           RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0005       A IC, 74LS05, TESTED & BURNED-IN          A *   C P EA         1     807  18-Jan-82
     7     305-0005       A IC, 74LS05                           RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0008       A IC, 74LS08 TESTED & BURNED-IN           A *   C P EA         2     807  18-Jan-82
     7     305-0008       A IC, 74LS08                           RI P 1 P B P EA         2     442  15-Jul-81
    6      308-0010       A IC, 74S10, TESTED & BURNED-IN           A *   C P EA         1     807  18-Jan-82
     7     307-0010       A IC, 74S10                            RI P 1 P B P EA         1     C063 15-Jul-81
    6      306-0020       A IC, 74LS20, TESTED & BURNED-IN          A *   C P EA         1     807  18-Jan-82
     7     305-0020       A IC, 74LS20                           RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0021       A IC, 74LS21, TESTED & BURNED-IN          A *   C P EA         1     807  18-Jan-82
     7     305-0021       A IC, 74LS21                           RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0032       A IC, 74LS32, TESTED & BURNED-IN          A *   C P EA         1     807  18-Jan-82
     7     305-0032       A IC, 74LS32                           RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0051       A IC, 74LS51, TESTED & BURNED-IN          A *   C P EA         2     807  18-Jan-82
     7     305-0051       A IC, 74LS51                           RI P 1 P B P EA         2     442  15-Jul-81
    6      306-0074       A IC, 74LS74, TESTED & BURNED-IN          A *   C P EA         2     807  18-Jan-82
     7     305-0074       A IC, 74LS74                           RI P 1 P B P EA         2     442  15-Jul-81
    6      306-0086       A IC, 74LS86, TESTED & BURNED-IN          A *   C P EA         1     807  18-Jan-82
     7     305-0086       A IC, 74LS86                           RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0138       A IC, 74LS138, TESTED & BURNED-IN         A *   C P EA         3     807  18-Jan-82
     7     305-0138       A IC, 74LS138                          RI P 1 P B P EA         3     442  15-Jul-81
    6      306-0126       A IC, 74LS126, TESTED & BURNED-IN         A *   C P EA         1     807  18-Jan-82
     7     305-0126       A IC, 74LS126                          RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0153       A IC, 74LS153, TESTED & BURNED-IN         A *   C P EA         1     807  18-Jan-82
     7     305-0153       A IC, 74LS153                          RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0157       A IC, 74LS157, TESTED & BURNED-IN         A *   C P EA         1     807  18-Jan-82
     7     305-0157       A IC, 74LS157                          RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0161       A IC, 74LS161, TESTED & BURNED-IN         A *   C P EA         4     807  18-Jan-82
     7     305-0161       A IC, 74LS161                          RI P 1 P B P EA         4     442  15-Jul-81
    6      306-0174       A IC, 74LS174, TESTED & BURNED-IN         A *   C P EA         1     807  18-Jan-82
     7     305-0174       A IC, 74LS174                          RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0139       A IC, 74LS139, TESTED & BURNED-IN         A *   C P EA         2     807  18-Jan-82
     7     305-0139       A IC, 74LS139                          RI P 1 P B P EA         2     442  15-Jul-81
    6      306-0244       A IC, 74LS244, TESTED & BURNED-IN         A *   C P EA         1     807  18-Jan-82
     7     305-0244       A IC, 74LS244                          RI P 1 P B P EA         1     442  15-Jul-81
    6      306-0251       A IC, 74LS251, TESTED & BURNED-IN         A *   C P EA         1     807  18-Jan-82
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PRINTED 23-Jul-82  13:38                    PERSONAL COMPUTER SYSTEMS                       BIL VERSION 29-Mar-79  PAGE   14

EFFECTIVITY DATE: ALL                  I N D E N T E D  B I L L S  O F  M A T E R I A L

 PARENT PART: 610-8156            INACT.FG,256K APPLE III                UM: EA   PROD CODE:     ECN:  A116   ASSEMBLY QTY:    1
                                  ERC: B   SRCE CODE: A    TYPE: *      ABC: A   PLAN CODE: U   DATE: 08-Jul-82

          COMPONENT       E PART DESCRIPTION                PR S T S A P         EXTENDED  ECN      START               CLOSE
LEVEL     PART NUMBER     R                                 CD C Y P B L UM      QTY PER   CHG   DATE       S/N      DATE      S/N

   6      306-0257        A IC, 74LS257, TESTED & BURNED-IN      A *   C P EA       3      807   18-Jan-82
    7     305-0257        A IC, 74LS257                     RI P 1 P B P EA       3      442   15-Jul-81
   6      306-0283        A IC, 74LS283, TESTED & BURNED-IN      A *   C P EA       1      807   18-Jan-82
    7     305-0283        A IC, 74LS283                     RI P 1 P B P EA       1      442   15-Jul-81
   6      306-0323        A IC, 74LS323, TESTED & BURNED-IN      A *   C P EA       1      807   18-Jan-82
    7     305-0323        A IC, 74LS323                     RI P 1 P B P EA       1      442   15-Jul-81
   6      306-0374        A IC, 74LS374, TESTED & BURNED-IN      A *   C P EA       6      807   18-Jan-82
    7     305-0374        A IC, 74LS374                     RI P 1 P B P EA       6      442   15-Jul-81
   6      306-0399        A IC, 74LS399, TESTED & BURNED-IN      A *   C P EA       2      807   18-Jan-82
    7     305-0399        A IC, 74LS399                     RI P 1 P B P EA       2      442   15-Jul-81
   6      308-0074        A IC, 74S74, TESTED & BURNED-IN        A *   C P EA       3      807   18-Jan-82
    7     307-0074        A IC, 74S74                       RI P 1 P B P EA       3      C063  15-Jul-81
   6      308-0086        A IC, 74S86, TESTED & BURNED-IN        A *   C P EA       2      807   18-Jan-82
    7     307-0086        A IC, 74S86                       RI P 1 P B P EA       2      C063  15-Jul-81
   6      308-0151        A IC, 74S151, TESTED & BURNED-IN       A *   C P EA       1      807   18-Jan-82
    7     307-0151        A IC, 74S151                      RI P 1 P B P EA       1      C063  15-Jul-81
   6      308-0153        A IC, 74S153, TESTED & BURNED-IN       A *   C P EA       4      807   18-Jan-82
    7     307-0153        A IC, 74S153                      RI P 1 P B P EA       4      C063  15-Jul-81
   6      308-0175        A IC, 74S175, TESTED & BURNED-IN       A *   C P EA       1      807   18-Jan-82
    7     307-0175        A IC, 74S175                      RI P 1 P B P EA       1      C063  15-Jul-81
   6      308-0195        A IC, 74S195, TESTED & BURNED-IN       A *   C P EA       1      807   18-Jan-82
    7     307-0195        A IC, 74S195 OR 93S00             RI P 1 P B P EA       1      C063  15-Jul-81
   6      308-0257        A IC, 74S257, TESTED & BURNED-IN       A *   C P EA       4      807   18-Jan-82
    7     307-0257        A IC, 74S257                      RI P 1 P B P EA       4      C063  15-Jul-81
   6      342-0032        A IC VIDEO CONTROL TST & BRN IN        A *   C P EA       1      831   18-Jan-82
    7     341-0032        O ROM, VIDEO CONTROL              RL P 1 P C P EA       1      449   10-Aug-81
   6      302-0166        A IC, 74166, TESTED & BURNED-IN        A *   C P EA       1      807   18-Jan-82
    7     301-0166        A IC, 74166                       RI P 1 P B P EA       1      C063  15-Jul-81
   6      369-6502        B IC MICRO 6502B 3MHZ TEST&BURN-IN     A *   C P EA       1      A098  18-Jan-82
    7     368-6502       ?O IC/MICROPROCESSOR 6502B 3MHz    RI P 1 P C P EA       1      458   31-Aug-81
   6      354-0380        A IC LM380 AUDIO PWR AMP TST & BRN IN  A *   C P EA       1      831   18-Jan-82
    7     353-0380        O IC, LM380 AUDIO POWER AMPLIFIER RI P 1 P C P EA       1      449   10-Aug-81
   6      342-0030       MA IC ROM SYNCHROM WITH BURN-IN         A *   C P EA       1      831   18-Jan-82
    7     341-0030        O ROM, SYNCHROM                   RL P 1 P C P EA       1      449   10-Aug-81
   6      342-0031       MA IC. ROM BOOT WITH BURN-IN            A *   C P EA       1      831   18-Jan-82
    7     341-0031        1 ROM, BOOT                       RL P 1 P C P EA       1      532   10-Aug-81
   6      338-6522        A IC 6522 I/F ADAPTER TEST&BURN-IN     A *   C P EA       2      877   18-Jan-82
    7     337-6522       MO IC, 6522 VERSATILE I/F ADAPTER  RL P 1 P B P EA       2      449   31-Aug-81
   6      338-0002        A ASYN COMM INT 6551A TST & BRN IN     A *   C P EA       1      877   18-Jan-82
    7     337-0002        A IC,6551A ASYNC,COMM.I/F ADAP. SELE.  P *   C P EA       1      736   31-Aug-81
   6      316-8304        A IC 8304B 8-BIT TRI-ST. TST&BRN IN    A *   C P EA       1      831   18-Jan-82
    7     315-8304        O IC, 8304B 8-BIT TRI-STATE       RI P 1 P B P EA       1      449   10-Aug-81
   6      330-0556        A IC 556 DUAL TIMER TEST&BURN-IN       A *   C P EA       3      831   18-Jan-82
    7     329-0556        O IC, 556 DUAL TIMER              RI P 1 P C P EA       3      449   10-Aug-81
   6      302-9334        B IC, 9334, TESTED & BURNED-IN         A *   C P EA       3      802   18-Jan-82
    7     301-9334        A IC, 9334                        RI P 1 P B P EA       3      C063  20-Jul-81
    7     301-0259        A IC, 74259                       EX P 7 P B P EA       0      C063  20-Jul-81
   6      360-1488        A IC 1488 QUAD LINE DRIVER TST&BRN-IN  A *   C P EA       1      831   18-Jan-82
    7     359-1488        O IC, 1488 QUAD LINE DRIVER       RI P 1 P C P EA       1      449   10-Aug-81
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EFFECTIVITY DATE: ALL                  I N D E N T E D   B I L L S   O F   M A T E R I A L

  PARENT PART: 610-8156          INACT.FQ,256K APPLE III                UM: EA    PROD CODE:      ECN: A116    ASSEMBLY QTY:     1
                                 ERC: B   SRCE CODE: A   TYPE: *       ABC: A    PLAN CODE: U   DATE: 08-Jul-82

             COMPONENT        E PART DESCRIPTION                        PR S T S A P         EXTENDED   ECN      START            CLOSE
LEVEL        PART NUMBER      R                                         CD C Y P B L UM     -QTY PER    CHG   DATE      S/N     DATE      S/N

     7       355-9708         O IC, 9708 6-CH. 8-BIT A TO D             RI P 1 P B P EA          1      449  10-Aug-81
    6        360-1489         A IC 1489 LINE REC. TEST&BURN-IN             A *   C P EA          1      831  18-Jan-82
     7       359-1489         O IC, 1489 LINE RECEIVER                  RI P 1 P C P EA          1      449  10-Aug-81
    6        372-3904         A TRANSISTOR,NPN SW.&AMP. 2N3904          RP P 1 P C P EA          4      C026 18-Jan-82
    6        111-0003         O RES ARRAY D/A CONVERTER 7 RES 8 PIN RP P 1 P C P EA              1      426  18-Jan-82
    6        111-0025         A RESISTOR ARRAY, SIP 7 RES, SPECIAL         P *   * P EA          1      923  18-Jan-82
    6        135-9101         A CAP,.1uF +80-20% Z5U/Y5V 50V            RP P 1 P C P EA         41      433  18-Jan-82
    6        151-5501         B CHOKE, 27uH 10%                         RP P 1 P B P EA          1      479  18-Jan-82
    6        342-0028         A IC.PROM,STATE MACH.P6A W/BURN-IN           A *   C P EA          1      831  18-Jan-82
     7       341-0028         1 IC, PROM, STATE MACHINE, P6A            RL A 1 P C P EA          1      454  10-Aug-81
      8      335-0471         A PROM,74S471                             RL P 1 P B P EA          1
    6        334-0005         A IC 1024 X 4 STATIC RAM TST & BRN IN        A *   C P EA          2      877  18-Jan-82
     7       334-2114         O IC, 1024 X 4 STATIC RAM 2114            RL P 1 P C P EA          2      449  31-Aug-81
    6        306-0133         A IC, 74LS133, TESTED & BURNED-IN            A *   C P EA          2      807  18-Jan-82
     7       305-0133         A IC, 74LS133                             RI P 1 P B P EA          2      442  15-Jul-81
    6        820-0043         O PCB, MAIN LOGIC BD #2 A3                RP P 7 P A P EA          1      503  18-Jan-82
    6        101-4112         A RES, 1/4W 5% 1.1K OHM                   RP P 1 P C P EA          2      426  18-Jan-82
    6        101-4104         A RES 1/4W 5% 100K OHM                    RP P 1 P C P EA          3      426  18-Jan-82
    6        126-5102         O CAP, 10uF 16V                           RP P 1 P C P EA          2      426  18-Jan-82
    6        197-0001         B CRYSTAL, 14.318630 MHz                  RI P 1 P C P EA          1      487  18-Jan-82
    6        101-4102         A RES 1/4W 5% 1K OHM                      RP P 1 P C P EA         15      426  18-Jan-82
    6        126-4102         O CAP, 1uF 50V                            RP P 1 P C P EA          3      426  18-Jan-82
    6        101-4225         A RES 1/4W 5% 2.2 MEG OHM                 RP P 1 P C P EA          1      426  18-Jan-82
    6        131-5401         O CAP, 20pF 5% NPO 50V                    RP P 1 P C P EA          1      426  18-Jan-82
    6        372-4258         A TRANSISTOR, PNP HIGH SPD.SW. 2N4258 RP P 1 P C P EA              2      C026 18-Jan-82
    6        101-4335         A RES 1/4W 5% 3.3 MEG OHM                 RP P 1 P C P EA          2      426  18-Jan-82
    6        197-0004         O CRYSTAL, TUNING FORK 32.768 KHz         RI P 1 P C P EA          1      449  18-Jan-82
    6        101-4302         A RES 1/4W 5% 3K OHM                      RP P 1 P C P EA          5      426  18-Jan-82
    6        101-4470         A RES 1/4W 5% 47 OHM                      RP P 1 P C P EA          3      426  18-Jan-82
    6        101-4474         A RES 1/4W 5% 470K OHM                    RP P 1 P C P EA          1      426  18-Jan-82
    6        101-4473         A RES 1/4W 5% 47K OHM                     RP P 1 P C P EA          2      426  18-Jan-82
    6        515-0053        MB CONN, STRAIGHT HEADER 2 PIN             RP P 1 P C P EA          1      532  18-Jan-82
    6        371-4148         A DIODE, 1N4148                           RP P 1 P C P EA          5      731  18-Jan-82
    6        519-0011         O CONNECTOR, 9 PIN D                      RC P 1 P C P EA          2      467  18-Jan-82
    6        519-0038         A CONN. 15 PIN D RT ANGLE PC MOUNT        RC P 1   C P EA          1      725  18-Jan-82
    6        515-0001         A JACK, PHONO RT ANG (MON) NTT 333-15 RP P 1 P C P EA              1      784  18-Jan-82
    6        515-0002         O JACK, PHONE                             RP P 1 P C P EA          1      467  18-Jan-82
    6        519-0014         O CONNECTOR,  HEADER 25 PIN               RC P 1 P C P EA          2      467  18-Jan-82
    6        519-0016         A CONN, 26 PIN HEADER W/O MTG EARS        RC P 1 P C P EA          2      523  18-Jan-82
    6        519-0017         A CONN, 26 PIN HEADER W/MTG EARS          RC P 1 P C P EA          1      523  18-Jan-82
    6        155-5102         A COIL, 10UH RADIAL                          P *   B P EA          2      DC44 18-Jan-82
    6        519-0018         O CONNECTOR, 25 PIN D                     RC P 1 P C P EA          1      467  18-Jan-82
    6        378-0001         B LED, RED                                RP P 1 P C P EA          1      DC53 18-Jan-82
    6        511-1401         C SOCKET, IC 14 PIN                       RP P 1 P C P EA         30      799  18-Jan-82
    6        511-1601         C SOCKET, IC 16 PIN                       RP P 1 P C P EA         36      799  18-Jan-82
    6        511-1801         C SOCKET, IC 18 PIN                       RP P 1 P C P EA          9      799  18-Jan-82
    6        511-2001         C SOCKET, IC 20 PIN                       RP P 1 P C P EA         11      799  18-Jan-82
    6        511-2401         C SOCKET, IC 24 PIN                       RP P 1 P C P EA          4      799  18-Jan-82
    6        511-2801         C SOCKET, IC 28 PIN                       RP P 1 P C P EA          1      799  18-Jan-82
    6        511-4001         C SOCKET, IC 40 PIN                       RP P 1 P C P EA          4      799  18-Jan-82
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PRINTED 23-Jul-82  13:39                     PERSONAL COMPUTER SYSTEMS                          BIL VERSION 29-Mar-79  PAGE   16

EFFECTIVITY DATE: ALL                  I N D E N T E D   B I L L S   O F   M A T E R I A L

  PARENT PART: 610-8156           INACT.FQ,256K APPLE III              UM: EA   PROD CODE:      ECN: A116   ASSEMBLY QTY:     1
                                  ERC: B   SRCE CODE: A   TYPE: *     ABC: A   PLAN CODE: U   DATE: 08-Jul-82

           COMPONENT         E PART DESCRIPTION                  PR S T S A P         EXTENDED  ECN       START                CLOSE
LEVEL      PART NUMBER       R                                   CD C Y P B L UM      QTY PER   CHG    DATE        S/N      DATE      S/N

    6      342-0056          A IC. PROM,CASB65.1 WITH BURN-IN       A *   C P EA         1      831  18-Jan-82
     7     341-0056          O IC, PROM CASB65.1                 RL A 1 P C P EA         1      503  10-Aug-81
      8    335-0003          O PROM, 1024 X 4 UNPROGRAMMED       RL P 1 P B P EA         1      SARA 27-Oct-80
    6      342-0043          A IC PROM U174 WITH BURN-IN            A *   C P EA         1      831  18-Jan-82
     7     341-0043          O PROM, 1024 X 4 U174               RL A 1 P C P EA         1      449  10-Aug-81
      8    335-0003          O PROM, 1024 X 4 UNPROGRAMMED       RL P 1 P B P EA         1      SARA
    6      342-0045          A IC.PROM,U176.2 WITH BURN-IN          A *   C P EA         1      831  18-Jan-82
     7     341-0045          O PROM, 1024 X 4 U176.2             RL A 1 P C P EA         1      449  10-Aug-81
      8    335-0003          O PROM, 1024 X 4 UNPROGRAMMED       RL P 1 P B P EA         1      SARA
    6      342-0046          A IC.PROM, U180 WITH BURN-IN           A *   C P EA         1      831  18-Jan-82
     7     341-0046          O PROM, 1024 X 4 U180               RL A 1 P B P EA         1      449  10-Aug-81
      8    335-0003          O PROM, 1024 X 4 UNPROGRAMMED       RL P 1 P B P EA         1      SARA
    6      342-0055         MA IC. PROM, U175-65 WITH BURN-IN       A *   C P EA         1      831  18-Jan-82
     7     341-0055          A IC, PROM U175-65                  RL A 1 P C P EA         1      503  10-Aug-81
      8    335-0003          O PROM, 1024 X 4 UNPROGRAMMED       RL P 1 P B P EA         1      SARA 27-Oct-80
    6      513-5002          D CONNECTOR, EDGE 25/50 PIN (NO TABS) RP P 1 P C P EA       4      760  18-Jan-82
    6      515-0103          A HEADER, RIGHT ANGLE 10 PINS          P *   C P EA         1      877  18-Jan-82
    6      306-0260          A IC, 74LS260, TESTED & BURNED-IN      A *   C P EA         1      807  18-Jan-82
     7     305-0260          A IC, 74LS260                       RI P 1 P B P EA         1      442  15-Jul-81
    6      131-5101          O CAP, 10pF 10% NPO 50V             RP P 1 P C P EA         1      426  18-Jan-82
    6      126-6404          A CAP, 220UF 16V                       * *   * * EA         4      C103 24-May-82
    6      151-5101          O CHOKE, 10uH 10%                   RP P 1 P B P EA         2      442  18-Jan-82
    6      132-6401          O CAP, 220pF 10% Z5F 50V            RP P 1 P C P EA         4      426  18-Jan-82
    6      372-3906          A TRANSISTOR,PNP SW.&AMP. 2N3906    RP P 1 P C P EA         1      C026 18-Jan-82
    6      101-4750          A RES 1/4W 5% 75 OHM                RP P 1 P C P EA         3      426  18-Jan-82
    6      101-4152          A RES 1/4W 5% 1.5K OHM              RP P 1 P C P EA         2      426  18-Jan-82
    6      101-4682          A RS 1/4W 5% 6.8K OHM               RP P 1 P C P EA         2      426  18-Jan-82
    6      519-0032          O CONN, 10 PIN FRICTION LOCK        RC P 1 P C P EA         1      442  18-Jan-82
    6      306-0132          A IC, 74LS132, TESTED & BURNED-IN      A *   C P EA         1      807  18-Jan-82
     7     305-0132          A IC, 74LS132                       RI P 1 P B P EA         1      442  15-Jul-81
    6      375-0005          O DIODE, 1N5712 SCHOTTKY BARRIER    RP P 1 P C P EA         1      449  18-Jan-82
    6      111-0018          O RES ARRAY 7 X 330 OHM             RP P 1 P C P EA         1      426  18-Jan-82
    6      111-0017          O RES ARRAY 9 X 3.3K OHM            RP P 1 P C P EA         2      426  18-Jan-82
    6      101-4330          A RES 1/4W 5% 33 OHM                RP P 1 P C P EA         4      426  18-Jan-82
    6      101-4101          A RES 1/4W 5% 100 OHM               RP P 1 P C P EA         2      426  18-Jan-82
    6      111-0014          O RES ARRAY 9 X 1K OHM              RP P 1 P C P EA         2      426  18-Jan-82
    6      101-4472          A RES 1/4W 5% 4.7K OHM              RP P 1 P C P EA         1      426  18-Jan-82
    6      101-4153          A RES 1/4W 5% 15K OHM               RP P 1 P C P EA         4      426  18-Jan-82
    6      101-4241          A RES 1/4W 5% 240 OHM               RP P 1 P C P EA         1      426  18-Jan-82
    6      101-4105          A RES, 1/4W 5% 1M OHM               RP P 1 P C P EA         2      426  18-Jan-82
    6      101-4301          A RES, 1/4W 5% 300 OHM              RP P 1 P C P EA         3      426  18-Jan-82
    6      101-4471          A RES 1/4W 5% 470 OHM               RP P 1 P C P EA         3      426  18-Jan-82
    6      125-5401          A CAP, 22uF 16V                     RP P 1 P C P EA         1      433  18-Jan-82
    6      511-0801          C SOCKET, IC 8 PIN                  RP P 1 P C P EA         1      799  18-Jan-82
    6      132-6101          O CAP, 100pF 20% Z5F 50V            RP P 1 P C P EA         3      426  18-Jan-82
    6      101-4181          A RES, 1/4W 5% 180 OHM              RP P 1 P C P EA         1      426  18-Jan-82
    6      119-2101         MA CAP, .01uF 10% 100V               RP P 1 P C P EA         1      449  18-Jan-82
    6      101-4125          A RES 1/4W 5% 1.2 MEG OHM           RP P 1 P C P EA         1      426  18-Jan-82
    6      133-2401          B CAP,  022uF 20% Y5P 25V           RP P 1 P C P EA         2      433  18-Jan-82
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PRINTED 23-Jul-82  13:39          PERSONAL COMPUTER SYSTEMS                        BIL VERSION 29-Mar-79  PAGE   17
EFFECTIVITY DATE: ALL             I N D E N T E D  B I L L S  O F  M A T E R I A L

  PARENT PART: 610-8156       INACT.FQ,256K APPLE III          UM: EA   PROD CODE:     ECN: A116   ASSEMBLY QTY:    1
                              ERC: B   SRCE CODE: A   TYPE: *  ABC: A   PLAN CODE: U   DATE: 08-Jul-82

           COMPONENT      E PART DESCRIPTION                   PR S T S A P       EXTENDED   ECN      START              CLOSE
LEVEL      PART NUMBER    R                                    CD C Y P B L UM    QTY PER    CHG   DATE       S/N     DATE       S/N

    6      111-0019       O RES ARRAY 5 X 1K OHM               RP P 1 P C P EA       3       426   18-Jan-82
    6      308-0374       A IC, 74S374, TESTED & BURNED-IN        A *   C P EA       1       807   18-Jan-82
     7     307-0374       A IC, 74S374                         RI P 1 P B P EA       1       C063  15-Jul-81
    6      308-0000       A IC, 74S00, TESTED & BURNED-IN         A *   C P EA       1       807   18-Jan-82
     7     307-0000       A IC, 74S00 QUAD NAND GATE           RI P 5 P B P EA       1       C063  15-Jul-81
    6      342-0035      MA IC ROM KYBD ENC. A3 BRN-IN & TST      A *   C P EA       1       886   18-Jan-82
     7     341-0035       B ROM, KEYBOARD ENCODER              RL P 1 P C P EA       1       683   21-Sep-81
    6      111-0001       O RES ARRAY 7 X 1K OHMS              RP P 1 P C P EA       3       426   18-Jan-82
    6      131-5701       O CAP, 47pF 5% N470 50V              RP P 1 P C P EA       1       426   18-Jan-82
    6      112-0001       B RES,INDIV. NTWRK. 68 OHM/5RES/10PIN RP P 1 P C P EA      1       609   18-Jan-82
    6      376-0001       A TRANSISTOR, MPS-U51                RP P 1 P C P EA       1       C111  18-Jan-82
    6      119-2701       A CAP, .047uF 10% 100V               RP P 1 P C P EA       1       DC3   18-Jan-82
    6      101-4103       A RES 1/4W 5% 10K OHM                RP P 1 P C P EA       2       426   18-Jan-82
    6      101-4270       A RES 1/4W 5% 27 OHM                 RP P 1 P C P EA       3       426   18-Jan-82
    6      101-4121       A RES 1/4W 5% 120 OHMS               RP P 1 P C P EA       4       426   18-Jan-82
    6      750-0006       B BUS BAR, CAPACITIVE .2uF           RP P 1 P C P EA       7       503   18-Jan-82
    6      562-2405       A WIRE, #24 KYNAR GREEN SOLID        EX X 7 P C P FT       4       503   18-Jan-82
    6      101-4432       A RES 1/4W 5% 4.3K OHM               RP P 1 P C P EA       1       426   18-Jan-82
    6      111-0006       O RES,ARRAY SPECIAL 8R, 9P           RP P 1 P C P EA       1       426   18-Jan-82
    6      831-0100       A RIVET, PLASTIC .125                   X *   C P EA       8       778   18-Jan-82
    6      306-0014       A IC, 74LS14, TESTED & BURNED-IN        A *   C P EA       1       807   18-Jan-82
     7     305-0014       A IC, 74LS14                         RI P 1 P B P EA       1       442   15-Jul-81
    6      136-3101      MC CAP, .1UF 10% XR7 50V                 P *   C P EA       6       C082  18-Jan-82
    6      342-0061       A I.C. PROM RAS65 WITH BURN-IN          A *   C P EA       1       867   18-Jan-82
     7     341-0061       A IC/PROM, RAS65,                    RL P 1   C P EA       1       665   24-Aug-81
    6      342-0063       A IC. PROM CASB256 WITH BURN-IN         A *   C P EA       1       867   18-Jan-82
     7     341-0063       A IC/PROM, CASB256                   RL P 1   C P EA       1       665   24-Aug-81
    6      825-0233       A LABEL, PCB SERIALIZATION              P *   * U EA       1       923   18-Jan-82
    6      942-0197       A BAG, POLY 12X18 ANTI-STAT             P *   * P EA       1       A024  26-Apr-82
    6      875-0005       A CONTACT PROTECTOR                     * *   * * EA       2       C132  26-Jul-82
    6      126-6402       O CAP, 220uF 16V                     RP P 1 P C P EA       4       426   18-Jan-82          23-May-82
   4       610-4256       A ASSY, PCB, TST, 5V MEMORY 256K A3     A *   A P EA       1       714   26-Apr-82
   4       865-0007       A BUMPER, HEMISPHERE .2" HIGH        EX X 7   C P EA      11       661   26-Apr-82
   4       805-0099       B BOTTOM COVER,MAIN BOARD 2 A3          P *   C P EA       1       972   26-Apr-82
    5      860-0018       A STANDOFF M3.5X0.6 BLD THD .200" LG EX X 1 P C P EA       6       559   07-Nov-81
   4       410-1410       B SCREW, M3.5 X .6 X 10MM PHMS       EX X 1   C P EA       6       C086  26-Apr-82
   4       860-0102       B SPACER,NYLON.125LX.140I.D.X.310O.D.   P *   * P EA       6       C095  26-Apr-82
  3        830-0031       A TIE WRAP, 3.800LG WHITE            EX X 7   C P EA       1       701   26-Apr-82
  3        420-1001       B SCREW, M3.5X6X10                   EX X 1 P C P EA      18       C086  18-Jan-82          26-Apr-82
  3        610-5197       A SUB ASSY, LOGO/NAMEPLATE A3           * *   * * EA       1       A035  10-May-82
   4       825-0054       C LABEL, APPLE LOGO NAMEPLATE        EX X 7 P C P EA       1       A035  10-May-82
   4       825-0066       C LABEL, MODEL NAMEPLATE A3          EX X 7 P C P EA       1       A035  10-May-82
 2         590-0029       O CABLE, MODEM ELIMINATOR            RC P 1 P B P EA       1       526   18-Jan-82          10-May-82
  3        520-0020       A HOUSING, CONN D-TYPE RECPT 25 PIN  EX P 7 P D P EA       1       482   12-Dec-80
  3        515-0023       A CONTACT, SOCKET (D-TYPE)           RP P 1 P D P EA       9       482   12-Dec-80
  3        590-0070       A CABLE, ROUND 8 CONDUCTOR           RC P 1 P D P FT       1       526   12-Dec-80
  3        515-0022       A CONTACT, PIN (D-TYPE)              RP P 1 P D P EA       9       482   12-Dec-80
  3        520-0030       A HOUSING, CONN D-TYPE 25 PIN        EX P 7 P D P EA       1       DC53  12-Dec-80
 2         942-0047       B BAG, PLASTIC 8" X 12"              EX X 1 P C P EA       1       C137  18-Jan-82          08-Jul-82
 2         942-0078       O INACT ENVELOPE VINYL ADHESIVE BACKED EX X 7 P C P EA     1       A116  18-Jan-82          08-Jul-82
```

```
PRINTED 23-Jul-82  13:40                   PERSONAL COMPUTER SYSTEMS                         BIL VERSION 29-Mar-79  PAGE   18
EFFECTIVITY DATE: ALL                     I N D E N T E D  B I L L S  O F  M A T E R I A L

  PARENT PART: 610-8156          INACT.FG,256K APPLE III               UM: EA   PROD CODE:      ECN: A116   ASSEMBLY QTY:    1
                                 ERC: B   SRCE CODE: A   TYPE: *      ABC: A   PLAN CODE: U   DATE: 08-Jul-82

              COMPONENT         E PART DESCRIPTION                   PR S T S A P       EXTENDED  ECN      START            CLOSE
LEVEL         PART NUMBER       R                                    CD C Y P B L UM    QTY PER   CHG   DATE      S/N    DATE       S/N

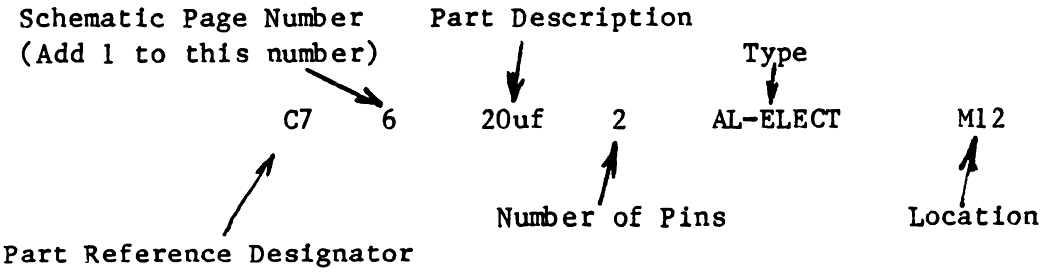
2             942-0079          B INACT.BOX,FG APPLE III SYSTEM      EX X 7 P C P EA       1      A116 18-Jan-82        08-Jul-82
2             946-0008          A TAPE, SEALING GLASS WEB #341 A3    EX X 7 P B P RL     0.0100  474  18-Jan-82        08-Jul-82
2             946-0005          A TAPE, 3M #218 3/4" WIDE            EX X 1 P C P RL     0.0050  C145 18-Jan-82        08-Jul-82
2             030-0241          A CUSTOMER LETTER, A3 CLOCK CHIP        X * P * P EA       1           18-Jan-82        26-Apr-82
2             944-0059          0 BAG, POLY, ANTI-STATIC, 24X36      EX X 7 P C P EA       1      442  26-Apr-82        08-Jul-82

           END OF REPORT
```

THE APPLE /// WIRE LIST

The following list is to be used for finding circuit components which are connected to each other.

INTEPRETING WIRE LIST NOMENCLATURE



Note: This wire list has schematic page numbers for the old Apple /// Schematic. Please add 1 to the schematic page number for the correct page.

A/// WIRE LIST

PART REFERENCE DESIGNATOR

SCHEMATIC SHEET #3

PART DESCRIPTION.

PINS, LEADS

TYPE

LOCATION

```
B1 2 BRIDGE 2
     1            PCAS0,3*
                 P1-9  U3-12  B1-1
     2            RAS0.3*
                 J17-12  R58-2  B1-2

C1 4 10U 2 AL-ELECT B1
     1           Q2-1  C1-1  R4-2
     2           GND

C2 4 .1U 2 MON A3
     1            PWRDN*
                 U72-23  Q3-3  C2-1  R6-2
     2           GND

C3 4 3-30P 3 A3
     1           GND
     2           GND
     3           Y2-1  U72-10  C3-3

C4 4 20P 2 CER A3
     1           C4-1  U72-11  Y2-2
     2           GND

C5 5 47P 2 CER N9
     1           P3-9  R55-2  C5-1  L1-1
     2           GND

C7 6 22U 2 AL-ELECT M12
     1           +5V
     2            DT1M
                 R31-1  U164-10  C7-2  U96-2  U96-6

C9 7 .022U 2 CER M10
     1           U105-6  R39-2  C9-1
     2           GNDF

C10 7 1U 2 ELECT
     1            SUMSND
                 R35-2  P9-1  C10-1  R78-2
     2            PEXTSPK
                 U172-19  C10-2

C12 7 10U 2 AL-ELECT
     1           +12V
     2           GND

C13 7 1U 2 ELECT N10
     1           C13-1  U103-8
     2           GND

C15 7 .01U 2 MYLAR M11
```

```
     1           TCAP
                 C15-1  U105-4
     2           GND

C16 8 47P 2 CER H14
     1           C16-1  U107-1
     2           U107-2  C16-2  R47-2

C17 8 .1U 2 MON M7
     1           U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
                 X3-1  C75-1
     2           U164-6  C17-2  X5-2  C75-2

C18 8 .05U 2 CER M8
     1           U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
                 X3-1  C75-1
     2           GND

C20 8 .1U 2 MON
     1            UPRST*
                 C20-1  U113-6  U113-2  R44-2  X4-2  X6-1
     2           GND

C21 8 .1U 2 MON A5
     1           U113-8  R46-2  U113-12  C21-1
     2           GND

C22 8 .1U 2 MON G12
     1           U107-31  C22-1
     2           GND

C23 9 .1U 2 MON B14
     1           Q10-2  R90-2  R91-1  C23-1  R49-1
     2           GND

C25 1 .1U 2 MON M7
     1           +5FV
     2           GNDF

C26 1 .1U 2 MON
     1           -5FV
     2           GNDF

C27 1 .1U 2 MON N11
     1           +12FV
     2           GNDF

C28 1 .1U 2 MON M10
     1           -12FV
     2           GNDF

C29 1 .1U 2 MON J2
```

```
     1          +12V
     2          GND

C30 1 .1U 2 MON J2
     1          +5V
     2          GND

C31 1 .1U 2 MON K1
     1          +12V
     2          GND

C32 1 .1U 2 MON K2
     1          +12V
     2          GND

C33 1 .1U 2 MON K4
     1          +12V
     2          GND

C34 1 .1U 2 MON K6
     1          +12V
     2          GND

C35 1 .1U 2 MON M1
     1          -12V
     2          GND

C36 1 .1U 2 MON M1
     1          -5V
     2          GND

C37 1 .1U 2 MON A2
     1          +5V
     2          GND

C38 1 .1U 2 MON K8
     1          +5V
     2          GND

C39 1 .1U 2 MON K10
     1          +5V
     2          GND

C40 1 .1U 2 MON K12
     1          +5V
     2          GND

C41 1 .1U 2 MON M6
     1          -12V
     2          GND

C42 1 .1U 2 MON G4
```

```
     1              +5V
     2              GND

C43 1 .1U 2 MON G12
     1              +5V
     2              GND

C44 1 .1U 2 MON G12
     1              +5V
     2              GND

C45 1 .1U 2 MON F7
     1              +5V
     2              GND

C46 1 .1U 2 MON A12
     1              +5V
     2              GND

C47 1 .1U 2 MON E14
     1              +5V
     2              GND

C48 1 .1U 2 MON M6
     1              -5V
     2              GND

C50 1 .1U 2 MON D7
     1              +5V
     2              GND

C51 1 .1U 2 MON B8
     1              +5V
     2              GND

C52 1 .1U 2 MON A6
     1              +5V
     2              GND

C53 1 .1U 2 MON E4
     1              +5V
     2              GND

C54 1 .1U 2 MON D4
     1              +5V
     2              GND

C55 1 .1U 2 MON C2
     1              +5V
     2              GND

C56 1 .1U 2 MON B10
```

```
     1           +5V
     2           GND

C57 1 .1U 2 MON B12
     1           +5V
     2           GND

C58 1 .1U 2 MON A10
     1           +5V
     2           GND

C59 9 10P 2 CER A8
     1            CS6522
                 R68-2  U73-24  C59-1  U97-24
     2           GND

C60 1 220U 2 AL-ELECT N11
     1           +5FV
     2           GNDF

C61 1 220U 2 AL-ELECT N7
     1           GNDF
     2           -5FV

C62 1 220U 2 AL-ELECT N12
     1           +12FV
     2           GNDF

C63 1 220U 2 AL-ELECT M10
     1           GNDF
     2           -12FV

C64 1 .1U 2 MON F14
     1           +5V
     2           GND

C65 1 .1U 2 MON A4
     1           +5V
     2           GND

C66 1 220P 2 CER M5
     1           R96-2  C66-1
     2           GND

C67 1 220P 2 CER L1
     1           R93-2  C67-1
     2           GND

C68 1 220P 2 CER L1
     1           R94-2  C68-1
     2           GND
```

```
C69 7 .1U 2 MON A8
     1          +5V
     2          C69-2  R75-2  U181-1  U181-2

C70 7 .1U 2 MON A8
     1          R77-2  U181-8  U181-12  C70-1
     2          GND

C71 8 1U 2 ELECT M14
     1           KRESET*
                U139-12  R80-1  C71-1  U179-15  J7-15
     2          GNDF

C73 9 .1U 2 MON B14
     1          +12V
     2          GND

C74 2 100P 2 CER D12
     1          R100-2  C74-1  U4-11
     2          GND

C75 8 .1U 2 MON M6
     1          U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
                X3-1  C75-1
     2          U164-6  C17-2  X5-2  C75-2

C76 7 .1U 2 MON M8
     1          U105-8  R37-2  R38-1  C76-1
     2          GND

C77 1 220P 2 CER L1
     1          R95-2  C77-1
     2          GND

C78 7 100P 2 CER
     1          C78-1  U103-2  R34-2  R36-1
     2          GND

C79 1 .1U 2 MON
     1          +5V
     2          GND

C80 1 .1U 2 MON
     1          +5V
     2          GND

J1 1 26PIN 26 RIBBON
     1          GNDF
     2           DPH0
                J6-2  U166-9  J1-2
     3          GNDF
     4           DPH1
```

```
               J6-4  U167-9  J1-4
     5         GNDF
     6          DPH2
               J6-6  U166-8  J1-6
     7         GNDF
     8          DPH3
               J6-8  U167-8  J1-8
     9         -12FV
     10         WRREQ
               J6-10  U166-7  J1-10
     11        +5FV
     12        +5FV
     13        +12FV
     14         ENBL1.E*
               J1-14  U166-5
     15        +12FV
     16         RDDATA
               J6-16  U166-4  J1-16
     17        +12FV
     18         WRDATA
               J6-18  U166-3  J1-18
     19        +12FV
     20         WRPROT
               J6-20  U167-4  J1-20
     21         ENBL3.E*
               J1-21  U166-2
     22         ENBL2.E*
               J1-22  U167-6
     23         AII*
               U167-5  J1-23  J6-23
     24         SIDE2/1
               J6-24  U167-7  J1-24
     25        NO CONNECTION
     26         EXT*
               J1-26  U167-2

J2 1 9PIN 9 9D
     1         GNDF
     2         +5FV
     3         GNDF
     4          X0
               U169-9  J2-4
     5          SW2
               U169-7  J2-5
     6         +12FV
     7         GNDF
     8          Y0
               U169-6  J2-8
     9          SW0
               U169-8  J2-9

J3 1 9PIN 9 9D
```

```
     1          GNDF
     2          +5FV
     3          GNDF
     4           X1/SER
                J3-4  U169-3
     5           SW1/MGNSW
                J3-5  U169-2
     6          +12FV
     7          GNDF
     8           Y1/XCO
                J3-8  U169-4
     9           SW3/SCO
                J3-9  U169-5

J4 1 25PIN 25 25D
     1          GNDF
     2           TXD
                J4-2  U172-9
     3           DATA IN
                J4-3  U172-8
     4           RTS
                J4-4  U172-7
     5           CTS
                J4-5  U172-6
     6           DSR
                J4-6  U172-5
     7          GNDF
     8           DCD
                J4-8  U172-3
     9          NO CONNECTION
     10         NO CONNECTION
     11         NO CONNECTION
     12         NO CONNECTION
     13         NO CONNECTION
     14         NO CONNECTION
     15         NO CONNECTION
     16         NO CONNECTION
     17         NO CONNECTION
     18         NO CONNECTION
     19         NO CONNECTION
     20          DTR
                J4-20  U172-4
     21         NO CONNECTION
     22         NO CONNECTION
     23         NO CONNECTION
     24         NO CONNECTION
     25         NO CONNECTION

J5 1 15PIN 15 15D
     1          GNDF
     2           XRGB4
                J5-2  P17-3  P18-3
     3          XSYNC
               J5-3  P17-9  P18-6
     4          PDINT*
               J5-4  U72-14
     5          XRGB1
               J5-5  P17-7  P18-5
     6         GNDF
     7         -5FV
     8         +12FV
     9          XRGB2
               J5-9  P17-5  P18-4
     10         XRGB8
               J5-10  P17-1  P18-2
     11         B&WVID
               J5-11  R15-2  J10-1  P18-7
     12         NTSC
               J5-12  R12-2  P18-8
     13        GNDF
     14        -12FV
     15        +5FV

J6 1 26PIN 26 RIBBON
     1         GNDF
     2          DPH0
               J6-2  U166-9  J1-2
     3         GNDF
     4          DPH1
               J6-4  U167-9  J1-4
     5         GNDF
     6          DPH2
               J6-6  U166-8  J1-6
     7         GNDF
     8          DPH3
               J6-8  U167-8  J1-8
     9         -12FV
     10         WRREQ
               J6-10  U166-7  J1-10
     11        +5FV
     12        +5FV
     13        +12FV
     14         ENBL1.I*
               J6-14  U166-6
     15        +12FV
     16         RDDATA
               J6-16  U166-4  J1-16
     17        +12FV
     18         WRDATA
               J6-18  U166-3  J1-18
     19        +12FV
     20         WRPROT
               J6-20  U167-4  J1-20
     21        NO CONNECTION
     22          NO CONNECTION
     23           AII*
                 U167-5  J1-23  J6-23
     24           SIDE2/1
                 J6-24  U167-7  J1-24
     25          NO CONNECTION
     26           INT*
                 J6-26  U167-3

J7 1 26PIN 26 RIBBON
     1            KY0
                 J7-1  U107-17
     2            KY1
                 J7-2  U107-18
     3            KVCC
                 J7-3  Q9-2
     4            KY2
                 J7-4  U107-19
     5            APPLEII*
                 J7-5  P11-5  U106-12  U164-5
     6            KY3
                 J7-6  U107-20
     7            APPLE1*
                 J7-7  P11-4  U111-3
     8            KY4
                 J7-8  U107-21
     9            CAPLCK*
                 J7-9  P11-3  U109-13
     10           KY5
                 J7-10  U107-22
     11           CONTROL*
                 J7-11  U179-13  U107-28  U109-10  P11-2
     12           KY8
                 J7-12  U107-25
     13          GNDF
     14           KX0
                 J7-14  U171-9
     15           KRESET*
                 U139-12  R80-1  C71-1  U179-15  J7-15
     16           KX2
                 J7-16  U171-8
     17           KX7
                 J7-17  U171-7
     18           KX1
                 J7-18  U171-6
     19           KX5
                 J7-19  U171-5
     20           KX3
                 J7-20  U171-4
     21           KX4
                 J7-21  U171-3
     22           KY9
```

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                 J7-22  U107-26
     23           KY6
                 J7-23  U107-23
     24           SHIFT*
                 J7-24  P11-6  U107-29
     25           KY7
                 J7-25  U107-24
     26           KX6
                 J7-26  U171-2

J8 1 10PIN 10 PWR G1
     1           -12V
     2           GND
     3           GND
     4           GND
     5           GND
     6           -5V
     7           +5V
     8           +5V
     9           +12V
     10          +12V

J9 1 2PIN 2 MOLEX M11
     1            AUDIO
                 J9-1  R69-1
     2           +5V

J10 1 2PIN 3 RCA
     1            B&WVID
                 J5-11  R15-2  J10-1  P18-7
     2           GNDF
     3           GNDF

J11 1 3PIN 3 MINPHONE
     1            EXTSPK1
                 J11-1  R34-1
     2            EXTSPK2
                 J11-2  U172-2
     3           GNDF

J12 1 50PIN 50 EDG
     1            IOSEL1*
                 U74-14  J12-1
     2            A0
                 J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
                 U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
     3            A1
                 J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
                 U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     4            A2
                 J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
                 U177-2  U94-2  U75-2  U73-36  U63-14
```

5	A3	J15-5 J14-5 J13-5 J12-5 U5-10 U109-1 U111-1 U97-35 U177-3 U94-3 U75-3 U73-35 U63-12
6	A4	J15-6 J14-6 J13-6 J12-6 U9-6 U77-1 U76-1 U112-2 U63-9
7	A5	J15-7 J14-7 J13-7 J12-7 U9-10 U76-2 U77-2 U112-3 U63-7
8	A6	J15-8 J14-8 J13-8 J12-8 U2-4 U77-3 U76-3 U71-10 U63-5 U71-11
9	A7	J15-9 J14-9 J13-9 J12-9 U13-10 U77-4 U76-6 U71-7 U63-3
10	A8	J15-10 J14-10 J13-10 J12-10 U67-4 U74-1 U71-6 U2-12 U13-6 U13-4
11	A9	J15-11 J14-11 J13-11 J12-11 U5-4 U74-2 U71-5 U67-7
12	A10	J15-12 J14-12 J13-12 J12-12 U128-1 U74-3 U71-4 U67-9
13	A11	J15-13 J14-13 J13-13 J12-13 U128-12 U6-6 U71-3 U150-13 U74-5 U67-12 U3-5 U174-5
14	A12	J15-14 J14-14 J13-14 J12-14 U9-12 U155-11 U165-14 U70-4 U71-2 U174-6
15	A13	J15-15 J14-15 J13-15 J12-15 U128-4 U155-12 U165-15 U71-1 U70-7 U6-5 U3-6 U174-7
16	A14	J15-16 J14-16 J13-16 J12-16 U3-7 U147-4 U70-9 U6-16 U174-4
17	A15	J15-17 J14-17 J13-17 J12-17 U3-4 U147-3 U70-12 U174-16 U6-7
18	R/W*	J15-18 J14-18 J13-18 J12-18 U3-3 U136-9 U180-17 U176-6 U165-11 U160-11
19	PHO	J15-19 U136-11 J14-19 J13-19 J12-19 U124-5 U65-37 R96-1
20	IOSTRB*	J15-20 U150-12 J14-20 J13-20 J12-20
21	RDY	J15-21 U164-8 J14-21 J13-21 J12-21 P14-4 U65-2
22	TSADB*	J15-22 J12-22 J14-22 J13-22 U163-3 P14-3
23	SPARE2	

J15-23 J12-23 J14-23 J13-23
24 SPARE1
J15-24 J12-24 J14-24 J13-24
25 +5V
26 GND
27 DMAOK
U144-8 J12-27 J15-27 J14-27 J13-27
28 DMAI*
U176-2 J12-28 J15-28 J14-28 J13-28 U163-5 P14-2
U153-9
29 IONMI*
J15-29 U97-17 J14-29 J13-29 U139-13 J12-29
30 IRQ1*
U101-14 J12-30 P2-7 U148-1
31 IORESET*
J12-31 J13-31 J14-31 J15-31 P14-6 U164-2 U164-4
U96-4 U94-15
32 INH*
J15-32 J14-32 J13-32 J12-32 U176-4 U165-13 P14-5
33 -12V
34 -5V
35 SYNC
U65-7 U136-1 J15-35 U174-3 J14-35 J13-35 J12-35
36 C7M
J15-36 J14-36 J13-36 J12-36 U141-9 U119-2 U146-12
U90-14
37 Q3
J14-37 U85-3 J15-37 J13-37 J12-37 U117-12 R93-1
U154-2
38 PRE1M*
J12-38 J13-38 J14-38 J15-38 U123-6 R95-1
39 C02X*
J15-39 U77-13 J14-39 J13-39 J12-39
40 PRE1M
J12-40 J13-40 J14-40 J15-40 U119-12 U73-25 U123-5
U97-25 U139-10 R94-1
41 DEVSEL1*
J12-41 U76-14
42 D7
J15-42 J14-42 J13-42 J12-42 U68-12 J16-24 U111-12
U101-5 U91-7 U69-12 P15-9
43 D6
J15-43 J14-43 J13-43 J12-43 U68-13 J16-23 U111-9
U91-13 U69-9 P15-8
44 D5
J15-44 J14-44 J13-44 J12-44 U68-14 J16-22 U111-7
U91-6 U69-7 P15-7
45 D4
J15-45 J14-45 J13-45 J12-45 U68-15 J16-21 U111-4
U91-14 U69-4 P15-6
46 D3
J15-46 J14-46 J13-46 J12-46 U68-16 J16-20 U109-12

```
              U91-5  U66-12  P15-5
     47        D2
              J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
              U91-15  U66-9  P15-4
     48        D1
              J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
              U91-4  U66-7  P15-3
     49        D0
              J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
              U91-16  U66-4  P15-2
     50       +12V

J13 1 50PIN 50 EDG
     1         IOSEL2*
              U74-13  J13-1
     2         A0
              J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
              U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
     3         A1
              J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
              U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     4         A2
              J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
              U177-2  U94-2  U75-2  U73-36  U63-14
     5         A3
              J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
              U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     6         A4
              J15-6  J14-6  J13-6  J12-6  U9-6  U77-1  U76-1
              U112-2  U63-9
     7         A5
              J15-7  J14-7  J13-7  J12-7  U9-10  U76-2  U77-2
              U112-3  U63-7
     8         A6
              J15-8  J14-8  J13-8  J12-8  U2-4  U77-3  U76-3
              U71-10  U63-5  U71-11
     9         A7
              J15-9  J14-9  J13-9  J12-9  U13-10  U77-4  U76-6
              U71-7  U63-3
     10        A8
              J15-10  J14-10  J13-10  J12-10  U67-4  U74-1  U71-6
              U2-12  U13-6  U13-4
     11        A9
              J15-11  J14-11  J13-11  J12-11  U5-4  U74-2  U71-5
              U67-7
     12        A10
              J15-12  J14-12  J13-12  J12-12  U128-1  U74-3  U71-4
              U67-9
     13        A11
              J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
              U150-13  U74-5  U67-12  U3-5  U174-5
     14        A12
```

J15-14 J14-14 J13-14 J12-14 U9-12 U155-11 U165-14
U70-4 U71-2 U174-6

15 A13
J15-15 J14-15 J13-15 J12-15 U128-4 U155-12 U165-15
U71-1 U70-7 U6-5 U3-6 U174-7

16 A14
J15-16 J14-16 J13-16 J12-16 U3-7 U147-4 U70-9
U6-16 U174-4

17 A15
J15-17 J14-17 J13-17 J12-17 U3-4 U147-3 U70-12
U174-16 U6-7

18 R/W*
J15-18 J14-18 J13-18 J12-18 U3-3 U136-9 U180-17
U176-6 U165-11 U160-11

19 PHO
J15-19 U136-11 J14-19 J13-19 J12-19 U124-5 U65-37
R96-1

20 IOSTRB*
J15-20 U150-12 J14-20 J13-20 J12-20

21 RDY
J15-21 U164-8 J14-21 J13-21 J12-21 P14-4 U65-2

22 TSADB*
J15-22 J12-22 J14-22 J13-22 U163-3 P14-3

23 SPARE2
J15-23 J12-23 J14-23 J13-23

24 SPARE1
J15-24 J12-24 J14-24 J13-24

25 +5V

26 GND

27 DMAOK
U144-8 J12-27 J15-27 J14-27 J13-27

28 DMAI*
U176-2 J12-28 J15-28 J14-28 J13-28 U163-5 P14-2
U153-9

29 IONMI*
J15-29 U97-17 J14-29 J13-29 U139-13 J12-29

30 IRQ2*
U101-15 J13-30 P2-6 U148-2

31 IORESET*
J12-31 J13-31 J14-31 J15-31 P14-6 U164-2 U164-4
U96-4 U94-15

32 INH*
J15-32 J14-32 J13-32 J12-32 U176-4 U165-13 P14-5

33 -12V

34 -5V

35 SYNC
U65-7 U136-1 J15-35 U174-3 J14-35 J13-35 J12-35

36 C7M
J15-36 J14-36 J13-36 J12-36 U141-9 U119-2 U146-12
U90-14

37 Q3
J14-37 U85-3 J15-37 J13-37 J12-37 U117-12 R93-1

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               U154-2
    38          PRE1M*
               J12-38  J13-38  J14-38  J15-38  U123-6  R95-1
    39          C02X*
               J15-39  U77-13  J14-39  J13-39  J12-39
    40          PRE1M
               J12-40  J13-40  J14-40  J15-40  U119-12  U73-25  U123-5
               U97-25  U139-10  R94-1
    41          DEVSEL2*
               J13-41  U76-13
    42          D7
               J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
               U101-5  U91-7  U69-12  P15-9
    43          D6
               J15-43  J14-43  J13-43  J12-43  U68-13  J16-23  U111-9
               U91-13  U69-9  P15-8
    44          D5
               J15-44  J14-44  J13-44  J12-44  U68-14  J16-22  U111-7
               U91-6  U69-7  P15-7
    45          D4
               J15-45  J14-45  J13-45  J12-45  U68-15  J16-21  U111-4
               U91-14  U69-4  P15-6
    46          D3
               J15-46  J14-46  J13-46  J12-46  U68-16  J16-20  U109-12
               U91-5  U66-12  P15-5
    47          D2
               J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
               U91-15  U66-9  P15-4
    48          D1
               J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
               U91-4  U66-7  P15-3
    49          D0
               J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
               U91-16  U66-4  P15-2
    50         +12V

J14 1 50PIN 50 EDG
    1           IOSEL3*
               U74-12  J14-1
    2           A0
               J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
               U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
    3           A1
               J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
               U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
    4           A2
               J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
               U177-2  U94-2  U75-2  U73-36  U63-14
    5           A3
               J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
               U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
    6           A4
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		J15-6 J14-6 J13-6 J12-6 U9-6 U77-1 U76-1 U112-2 U63-9
7	A5	J15-7 J14-7 J13-7 J12-7 U9-10 U76-2 U77-2 U112-3 U63-7
8	A6	J15-8 J14-8 J13-8 J12-8 U2-4 U77-3 U76-3 U71-10 U63-5 U71-11
9	A7	J15-9 J14-9 J13-9 J12-9 U13-10 U77-4 U76-6 U71-7 U63-3
10	A8	J15-10 J14-10 J13-10 J12-10 U67-4 U74-1 U71-6 U2-12 U13-6 U13-4
11	A9	J15-11 J14-11 J13-11 J12-11 U5-4 U74-2 U71-5 U67-7
12	A10	J15-12 J14-12 J13-12 J12-12 U128-1 U74-3 U71-4 U67-9
13	A11	J15-13 J14-13 J13-13 J12-13 U128-12 U6-6 U71-3 U150-13 U74-5 U67-12 U3-5 U174-5
14	A12	J15-14 J14-14 J13-14 J12-14 U9-12 U155-11 U165-14 U70-4 U71-2 U174-6
15	A13	J15-15 J14-15 J13-15 J12-15 U128-4 U155-12 U165-15 U71-1 U70-7 U6-5 U3-6 U174-7
16	A14	J15-16 J14-16 J13-16 J12-16 U3-7 U147-4 U70-9 U6-16 U174-4
17	A15	J15-17 J14-17 J13-17 J12-17 U3-4 U147-3 U70-12 U174-16 U6-7
18	R/W*	J15-18 J14-18 J13-18 J12-18 U3-3 U136-9 U180-17 U176-6 U165-11 U160-11
19	PHO	J15-19 U136-11 J14-19 J13-19 J12-19 U124-5 U65-37 R96-1
20	IOSTRB*	J15-20 U150-12 J14-20 J13-20 J12-20
21	RDY	J15-21 U164-8 J14-21 J13-21 J12-21 P14-4 U65-2
22	TSADB*	J15-22 J12-22 J14-22 J13-22 U163-3 P14-3
23	SPARE2	J15-23 J12-23 J14-23 J13-23
24	SPARE1	J15-24 J12-24 J14-24 J13-24
25	+5V	

26 GND

27 DMAOK
U144-8 J12-27 J15-27 J14-27 J13-27

28 DMAI*
U176-2 J12-28 J15-28 J14-28 J13-28 U163-5 P14-2
U153-9

29 IONMI*
J15-29 U97-17 J14-29 J13-29 U139-13 J12-29

30 IRQ3*
U97-7 J14-30 P2-4 U148-4

31 IORESET*
J12-31 J13-31 J14-31 J15-31 P14-6 U164-2 U164-4
U96-4 U94-15

32 INH*
J15-32 J14-32 J13-32 J12-32 U176-4 U165-13 P14-5

33 -12V

34 -5V

35 SYNC
U65-7 U136-1 J15-35 U174-3 J14-35 J13-35 J12-35

36 C7M
J15-36 J14-36 J13-36 J12-36 U141-9 U119-2 U146-12
U90-14

37 Q3
J14-37 U85-3 J15-37 J13-37 J12-37 U117-12 R93-1
U154-2

38 PRE1M*
J12-38 J13-38 J14-38 J15-38 U123-6 R95-1

39 C02X*
J15-39 U77-13 J14-39 J13-39 J12-39

40 PRE1M
J12-40 J13-40 J14-40 J15-40 U119-12 U73-25 U123-5
U97-25 U139-10 R94-1

41 DEVSEL3*
J14-41 U76-12

42 D7
J15-42 J14-42 J13-42 J12-42 U68-12 J16-24 U111-12
U101-5 U91-7 U69-12 P15-9

43 D6
J15-43 J14-43 J13-43 J12-43 U68-13 J16-23 U111-9
U91-13 U69-9 P15-8

44 D5
J15-44 J14-44 J13-44 J12-44 U68-14 J16-22 U111-7
U91-6 U69-7 P15-7

45 D4
J15-45 J14-45 J13-45 J12-45 U68-15 J16-21 U111-4
U91-14 U69-4 P15-6

46 D3
J15-46 J14-46 J13-46 J12-46 U68-16 J16-20 U109-12
U91-5 U66-12 P15-5

47 D2
J15-47 J14-47 J13-47 J12-47 U68-17 J16-19 U109-9
U91-15 U66-9 P15-4

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     48           D1
                 J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
                 U91-4  U66-7  P15-3
     49           D0
                 J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
                 U91-16  U66-4  P15-2
     50           +12V

J15 1 50PIN 50 EDG
     1            IOSEL4*
                 U74-11  J15-1
     2            A0
                 J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
                 U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
     3            A1
                 J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
                 U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     4            A2
                 J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
                 U177-2  U94-2  U75-2  U73-36  U63-14
     5            A3
                 J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
                 U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     6            A4
                 J15-6  J14-6  J13-6  J12-6  U9-6  U77-1  U76-1
                 U112-2  U63-9
     7            A5
                 J15-7  J14-7  J13-7  J12-7  U9-10  U76-2  U77-2
                 U112-3  U63-7
     8            A6
                 J15-8  J14-8  J13-8  J12-8  U2-4  U77-3  U76-3
                 U71-10  U63-5  U71-11
     9            A7
                 J15-9  J14-9  J13-9  J12-9  U13-10  U77-4  U76-6
                 U71-7  U63-3
     10           A8
                 J15-10  J14-10  J13-10  J12-10  U67-4  U74-1  U71-6
                 U2-12  U13-6  U13-4
     11           A9
                 J15-11  J14-11  J13-11  J12-11  U5-4  U74-2  U71-5
                 U67-7
     12           A10
                 J15-12  J14-12  J13-12  J12-12  U128-1  U74-3  U71-4
                 U67-9
     13           A11
                 J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
                 U150-13  U74-5  U67-12  U3-5  U174-5
     14           A12
                 J15-14  J14-14  J13-14  J12-14  U9-12  U155-11  U165-14
                 U70-4  U71-2  U174-6
     15           A13
                 J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
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U71-1 U70-7 U6-5 U3-6 U174-7
16 A14
J15-16 J14-16 J13-16 J12-16 U3-7 U147-4 U70-9
U6-16 U174-4
17 A15
J15-17 J14-17 J13-17 J12-17 U3-4 U147-3 U70-12
U174-16 U6-7
18 R/W*
J15-18 J14-18 J13-18 J12-18 U3-3 U136-9 U180-17
U176-6 U165-11 U160-11
19 PHO
J15-19 U136-11 J14-19 J13-19 J12-19 U124-5 U65-37
R96-1
20 IOSTRB*
J15-20 U150-12 J14-20 J13-20 J12-20
21 RDY
J15-21 U164-8 J14-21 J13-21 J12-21 P14-4 U65-2
22 TSADB*
J15-22 J12-22 J14-22 J13-22 U163-3 P14-3
23 SPARE2
J15-23 J12-23 J14-23 J13-23
24 SPARE1
J15-24 J12-24 J14-24 J13-24
25 +5V
26 GND
27 DMAOK
U144-8 J12-27 J15-27 J14-27 J13-27
28 DMAI*
U176-2 J12-28 J15-28 J14-28 J13-28 U163-5 P14-2
U153-9
29 IONMI*
J15-29 U97-17 J14-29 J13-29 U139-13 J12-29
30 IRQ4*
U97-6 J15-30 P2-3 U148-5
31 IORESET*
J12-31 J13-31 J14-31 J15-31 P14-6 U164-2 U164-4
U96-4 U94-15
32 INH*
J15-32 J14-32 J13-32 J12-32 U176-4 U165-13 P14-5
33 -12V
34 -5V
35 SYNC
U65-7 U136-1 J15-35 U174-3 J14-35 J13-35 J12-35
36 C7M
J15-36 J14-36 J13-36 J12-36 U141-9 U119-2 U146-12
U90-14
37 Q3
J14-37 U85-3 J15-37 J13-37 J12-37 U117-12 R93-1
U154-2
38 PRE1M*
J12-38 J13-38 J14-38 J15-38 U123-6 R95-1
39 CO2X*

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               J15-39  U77-13  J14-39  J13-39  J12-39
    40          PRE1M
               J12-40  J13-40  J14-40  J15-40  U119-12  U73-25  U123-5
               U97-25  U139-10  R94-1
    41          DEVSEL4*
               J15-41  U76-11
    42          D7
               J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
               U101-5  U91-7  U69-12  P15-9
    43          D6
               J15-43  J14-43  J13-43  J12-43  U68-13  J16-23  U111-9
               U91-13  U69-9  P15-8
    44          D5
               J15-44  J14-44  J13-44  J12-44  U68-14  J16-22  U111-7
               U91-6  U69-7  P15-7
    45          D4
               J15-45  J14-45  J13-45  J12-45  U68-15  J16-21  U111-4
               U91-14  U69-4  P15-6
    46          D3
               J15-46  J14-46  J13-46  J12-46  U68-16  J16-20  U109-12
               U91-5  U66-12  P15-5
    47          D2
               J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
               U91-15  U66-9  P15-4
    48          D1
               J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
               U91-4  U66-7  P15-3
    49          D0
               J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
               U91-16  U66-4  P15-2
    50         +12V

J16 1 25PIN 25 LNGMOLEX
    1           DB0
               J16-1  U66-3  U80-13
    2           DB1
               J16-2  U66-6  U80-8
    3           DB2
               J16-3  U66-10  U80-14
    4           DB3
               J16-4  U66-13  U80-7
    5           DB4
               J16-5  U69-3  U80-17
    6           DB5
               J16-6  U69-6  U80-4
    7           DB6
               J16-7  U69-10  U80-18
    8           DB7
               J16-8  U69-13  U80-3
    9           DA0
               J16-9  U10-4  U84-13  U66-2
    10          DA1
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              J16-10  U10-5  U84-8  U66-5
     11        DA2
              J16-11  U10-12  U84-14  U66-11
     12        DA3
              J16-12  U66-14  U84-7
     13        DA4
              J16-13  U69-2  U84-17
     14        DA5
              J16-14  U69-5  U84-4
     15        DA6
              J16-15  U69-11  U84-18
     16        DA7
              J16-16  U153-5  U84-3  U69-14
     17        D0
              J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
              U91-16  U66-4  P15-2
     18        D1
              J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
              U91-4  U66-7  P15-3
     19        D2
              J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
              U91-15  U66-9  P15-4
     20        D3
              J15-46  J14-46  J13-46  J12-46  U68-16  J16-20  U109-12
              U91-5  U66-12  P15-5
     21        D4
              J15-45  J14-45  J13-45  J12-45  U68-15  J16-21  U111-4
              U91-14  U69-4  P15-6
     22        D5
              J15-44  J14-44  J13-44  J12-44  U68-14  J16-22  U111-7
              U91-6  U69-7  P15-7
     23        D6
              J15-43  J14-43  J13-43  J12-43  U68-13  J16-23  U111-9
              U91-13  U69-9  P15-8
     24        D7
              J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
              U101-5  U91-7  U69-12  P15-9
     25       GND

J17 1 25PIN 25 LNGMOLEX
     1        GND
     2        +5V
     3        +12V
     4         AR6
              J17-4  U13-9  P16-5
     5         AR5
              R99-2  J17-5
     6         AR4
              J17-6  U9-7  P16-6
     7         AR3
              J17-7  U5-9  P16-3
     8         AR2
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                J17-8  U5-7  P16-2
    9            AR1
                R98-2  J17-9
    10           AR0
                R97-2  J17-10
    11           RAMR/W*
                J17-11  U150-8
    12           RAS0.3*
                J17-12  R58-2  B1-2
    13           RAS1.2*
                J17-13  R59-2
    14           RAS4.5*
                J17-14  R60-2
    15           RAS6.7*
                J17-15  R61-2
    16          -5V
    17           CAS0*
                J17-17  U4-2
    18           CAS1*
                J17-18  U4-5
    19           CAS2*
                J17-19  U4-6
    20           CAS3*
     .          J17-20  U4-9
    21           CAS4,6*
                J17-21  U4-12
    22           CAS5,7*
                U4-15  J17-22
    23           AX*
                U124-8  U2-2  U13-2  U9-2  U5-2  J17-23
    24           AR7
                U13-7  J17-24
    25          GND

J19 1 3PIN 3 MOLEX H14
    1            UUTSUNK*
                J19-1  U118-9  U162-8  U120-9
    2            FIELDOUT
                U126-19  J19-2
    3            FIELDIN
                J19-3  U121-18  R63-1

J20 1 10PIN 10 MOLEX H1
    1            SYNCH
                J20-1  P17-10  U126-5  P3-2  P4-6
    2            RGB2
                J20-2  P17-6  P4-3  P3-4  P10-6  U90-5  U90-13
                U89-10
    3            C3.5M
                U132-10  U141-10  U146-13  U119-7  J20-3
    4            RGB4
                P4-4  P17-4  P3-5  P10-7  U90-4  U90-10  U89-7
```

```
               J20-4
     5          RGB8
               J20-5  P4-5  P17-2  P3-6  P10-3  U90-11  U90-3
               U89-2
     6          RGB1
               U89-15  P17-8  P4-2  P3-3  J20-6  P10-4  U90-6
               U90-12
     7          FORCPAGE
               U87-6  P10-2  J20-7
     8          COLRGATE
               J20-8  U147-2  U126-6
     9          COLORKILL*
               U147-13  U87-11  J20-9
     10        GND

J21 1 5PIN 5 MOLEX B14
     1          HPEDIS
               U135-2  J21-1  R54-1
     2          C14M*
               U141-13  U146-8  U124-11  J21-2
     3          UUTRST*
               U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
               U120-1  U118-1  U117-1
     4          UUTUPRST
               R92-2  U162-11  J21-4  U164-3
     5         GND

L1 5 27U 2 L1 M10
     1         P3-9  R55-2  C5-1  L1-1
     2         GNDF

L2 1 30U 2 FIL1 M7
     1         +5V
     2         +5FV

L3 1 10U 2 FIL2 L7
     1         -5V
     2         -5FV

L4 1 30U 2 FIL1 M7
     1         +12V
     2         +12FV

L5 1 10U 2 FIL2 L7
     1         -12V
     2         -12FV

Q1 4 3904 3 TR1 C1
     1         U72-24  Q1-1  X1-2
     2         Q1-2  R5-2
     3         +5V
```

```
Q2 4 3906 3 TR1 C1
     1          Q2-1  C1-1  R4-2
     2          +5V
     3          Q3-2  Q2-3  R101-1

Q3 4 3904 3 TR1 B1
     1          GND
     2          Q3-2  Q2-3  R101-1
     3           PWRDN*
                U72-23  Q3-3  C2-1  R6-2

Q4 5 3904 3 TR1 M7
     1          R15-1  Q4-1  R16-1
     2          P4-1  Q4-2
     3          +5V

Q9 8 MPSU51 3 TR1 L14
     1          +5FV
     2           KVCC
                J7-3  Q9-2
     3          Q9-3  R43-1  U111-10

Q10 9 4258 3 TR1 B13
     1          Q11-1  R48-2  Q10-1
     2          Q10-2  R90-2  R91-1  C23-1  R49-1
     3          R52-1  Q10-3  Y1-1

Q11 9 4258 3 TR1 B13
     1          Q11-1  R48-2  Q10-1
     2
                Y1-2  Q11-2  R49-2
     3
                Q11-3  R51-1  U146-10  U146-5  U146-2

Q12 5 3904 3 TR1 L7
     1          R12-1  R13-1  Q12-1
     2          P3-1  Q12-2
     3          +5V

P1 2 1K 10 SIP10 C14
     1          +5V
     2           PCAS4,6*
                U4-13  U6-14  P1-2
     3           PCAS1*
                P1-3  U4-4  U6-12  U128-10
     4           PCAS2*
                P1-4  U4-7  U6-11
     5           PCAS5,7*
                U4-14  P1-5  U6-13
     6           PCAS3*
                U128-2  U128-13  P1-6  U3-11  U4-8
     7           PCAS0*
```

```
               P1-7  U4-3  U3-14
     8          PUSELB
               U4-17  P1-8  U3-13
     9          PCAS0,3*
               P1-9  U3-12  B1-1
     10        NO CONNECTION

P2 4 1K 8 SIP8 J4
     1         +5V
     2         NO CONNECTION
     3          IRQ4*
               U97-6  J15-30  P2-3  U148-5
     4          IRQ3*
               U97-7  J14-30  P2-4  U148-4
     5         NO CONNECTION
     6          IRQ2*
               U101-15  J13-30  P2-6  U148-2
     7          IRQ1*
               U101-14  J12-30  P2-7  U148-1
     8         NO CONNECTION

P3 5 SP3 10 SIP10 L9
     1         P3-1  Q12-2
     2          SYNCH
               J20-1  P17-10  U126-5  P3-2  P4-6
     3          RGB1
               U89-15  P17-8  P4-2  P3-3  J20-6  P10-4  U90-6
               U90-12
     4          RGB2
               J20-2  P17-6  P4-3  P3-4  P10-6  U90-5  U90-13
               U89-10
     5          RGB4
               P4-4  P17-4  P3-5  P10-7  U90-4  U90-10  U89-7
               J20-4
     6          RGB8
               J20-5  P4-5  P17-2  P3-6  P10-3  U90-11  U90-3
               U89-2
     7          NTSCA
               P3-7  U90-7
     8          NTSCB
               P3-8  U163-8
     9         P3-9  R55-2  C5-1  L1-1
     10        NO CONNECTION

P4 5 SP4 8 SIP8 M8
     1         P4-1  Q4-2
     2          RGB1
               U89-15  P17-8  P4-2  P3-3  J20-6  P10-4  U90-6
               U90-12
     3          RGB2
               J20-2  P17-6  P4-3  P3-4  P10-6  U90-5  U90-13
               U89-10
```

```
    4        RGB4
             P4-4  P17-4  P3-5  P10-7  U90-4  U90-10  U89-7
             J20-4
    5        RGB8
             J20-5  P4-5  P17-2  P3-6  P10-3  U90-11  U90-3
             U89-2
    6        SYNCH
             J20-1  P17-10  U126-5  P3-2  P4-6
    7        NO CONNECTION
    8        +5V

P8 5 1K 6 SIP6 F4
    1        +5V
    2        NO CONNECTION
    3        DX5
             U89-12  U86-5  P8-3
    4        DX4
             U89-13  U86-16  P8-4
    5        DX6
             U89-5  U86-19  P8-5
    6        DX7
             U89-4  U86-2  P8-6

P9 7 SP9 8 SIP8 C5
    1        SUMSND
             R35-2  P9-1  C10-1  R78-2
    2        SND5
             P9-2  U97-15
    3        SND4
             P9-3  U97-14
    4        SND3
             P9-4  U97-13
    5        SND2
             P9-5  U97-12
    6        SND1
             P9-6  U97-11
    7        SND0
             P9-7  U97-10
    8        +5V

P10 5 1K 8 SIP8 G4
    1        +5V
    2        FORCPAGE
             U87-6  P10-2  J20-7
    3        RGB8
             J20-5  P4-5  P17-2  P3-6  P10-3  U90-11  U90-3
             U89-2
    4        RGB1
             U89-15  P17-8  P4-2  P3-3  J20-6  P10-4  U90-6
             U90-12
    5        NO CONNECTION
    6        RGB2
```

```
                J20-2  P17-6  P4-3  P3-4  P10-6  U90-5  U90-13
                U89-10
     7           RGB4
                P4-4  P17-4  P3-5  P10-7  U90-4  U90-10  U89-7
                J20-4
     8          NO CONNECTION

P11 8 1K 8 SIP8 L14
     1          +5FV
     2           CONTROL*
                J7-11  U179-13  U107-28  U109-10  P11-2
     3           CAPLCK*
                J7-9  P11-3  U109-13
     4           APPLE1*
                J7-7  P11-4  U111-3
     5           APPLEII*
                J7-5  P11-5  U106-12  U164-5
     6           SHIFT*
                J7-24  P11-6  U107-29
     7          NO CONNECTION
     8          NO CONNECTION

P13 5 1K 6 SIP6 G3
     1          GND
     2           DX0
                U88-14  U86-12  P13-2
     3           DX2
                U88-5  U86-15  P13-3
     4           DX3
                U88-2  U86-6  P13-4
     5           DX1
                U88-11  U86-9  P13-5
     6          NO CONNECTION

P14 3-4-8 1K 6 SIP6 M1
     1          +5V
     2           DMAI*
                U176-2  J12-28  J15-28  J14-28  J13-28  U163-5  P14-2
                U153-9
     3           TSADB*
                J15-22  J12-22  J14-22  J13-22  U163-3  P14-3
     4           RDY
                J15-21  U164-8  J14-21  J13-21  J12-21  P14-4  U65-2
     5           INH*
                J15-32  J14-32  J13-32  J12-32  U176-4  U165-13  P14-5
     6           IORESET*
                J12-31  J13-31  J14-31  J15-31  P14-6  U164-2  U164-4
                U96-4  U94-15

P15 3 3.3K 10 SIP10 C3
     1          +5V
     2           D0
```

```
             J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
             U91-16  U66-4  P15-2
    3         D1
             J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
             U91-4  U66-7  P15-3
    4         D2
             J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
             U91-15  U66-9  P15-4
    5         D3
             J15-46  J14-46  J13-46  J12-46  U68-16  J16-20  U109-12
             U91-5  U66-12  P15-5
    6         D4
             J15-45  J14-45  J13-45  J12-45  U68-15  J16-21  U111-4
             U91-14  U69-4  P15-6
    7         D5
             J15-44  J14-44  J13-44  J12-44  U68-14  J16-22  U111-7
             U91-6  U69-7  P15-7
    8         D6
             J15-43  J14-43  J13-43  J12-43  U68-13  J16-23  U111-9
             U91-13  U69-9  P15-8
    9         D7
             J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
             U101-5  U91-7  U69-12  P15-9
    10       NO CONNECTION

P16 2 330 8 SIP8 F13
    1        +5V
    2         AR2
             J17-8  U5-7  P16-2
    3         AR3
             J17-7  U5-9  P16-3
    4         AR0
             P16-4  R97-1  U2-7
    5         AR6
             J17-4  U13-9  P16-5
    6         AR4
             J17-6  U9-7  P16-6
    7         AR5
             R99-1  U9-9  P16-7
    8         AR1
             P16-8  R98-1  U2-9

P17 5 75 10 SIP10 M9
    1         XRGB8
             J5-10  P17-1  P18-2
    2         RGB8
             J20-5  P4-5  P17-2  P3-6  P10-3  U90-11  U90-3
             U89-2
    3         XRGB4
             J5-2  P17-3  P18-3
    4         RGB4
             P4-4  P17-4  P3-5  P10-7  U90-4  U90-10  U89-7
```

```
              J20-4
    5           XRGB2
              J5-9  P17-5  P18-4
    6           RGB2
              J20-2  P17-6  P4-3  P3-4  P10-6  U90-5  U90-13
              U89-10
    7           XRGB1
              J5-5  P17-7  P18-5
    8           RGB1
              U89-15  P17-8  P4-2  P3-3  J20-6  P10-4  U90-6
              U90-12
    9           XSYNC
              J5-3  P17-9  P18-6
    10          SYNCH
              J20-1  P17-10  U126-5  P3-2  P4-6

P18 5 220P 8 SIP8 M9
    1         GNDF
    2           XRGB8
              J5-10  P17-1  P18-2
    3           XRGB4
              J5-2  P17-3  P18-3
    4           XRGB2
              J5-9  P17-5  P18-4
    5           XRGB1
              J5-5  P17-7  P18-5
    6           XSYNC
              J5-3  P17-9  P18-6
    7           B&WVID
              J5-11  R15-2  J10-1  P18-7
    8           NTSC
              J5-12  R12-2  P18-8

P19 4 3.3K 10 SIP10 B6
    1         +5V
    2           SEL1M
              U180-15  U174-2  U150-3  U73-9  P19-2
    3           IOEN
              U73-8  P19-3  U147-10
    4           SCRN
              U154-13  U73-7  P19-4
    5           RESETLK*
              U179-14  U73-6  P19-5  U139-5
    6           RWPR
              U73-5  P19-6  U180-16
    7           PRIMSTK
              U73-4  P19-7  U158-9
    8           ROMSEL2
              U73-3  U64-21  P19-8
    9           ROMSEL1
              U165-10  U73-2  P19-9
    10          PH2M
```

```
                P19-10  U141-5  U65-39  U176-17

R4 4 100K 2 QW A2
   1            +5V
   2            Q2-1  C1-1  R4-2

R5 4 47K 2 QW C2
   1            +12V
   2            Q1-2  R5-2

R6 4 470K 2 QW A2
   1            +5V
   2             PWRDN*
                U72-23  Q3-3  C2-1  R6-2

R9 4 3.3M 2 QW A2
   1            R9-1  T1-1  X1-1  U105-10
   2            GND

R12 5 47 2 QW N6
   1            R12-1  R13-1  Q12-1
   2             NTSC
                J5-12  R12-2  P18-8

R13 5 75 2 QW N6
   1            R12-1  R13-1  Q12-1
   2            GND

R15 5 47 2 QW M6
   1            R15-1  Q4-1  R16-1
   2             B&WVID
                J5-11  R15-2  J10-1  P18-7

R16 5 75 2·QW N5
   1            R15-1  Q4-1  R16-1
   2            GND

R31 6 47K 2 QW N14
   1             DT1M
                R31-1  U164-10  C7-2  U96-2  U96-6
   2            +5V

R34 7 3K 2 QW N5
   1             EXTSPK1
                J11-1  R34-1
   2            C78-1  U103-2  R34-2  R36-1

R35 7 4.7K 2 QW G6
   1             AIISPKR
                R35-1  U173-9
   2             SUMSND
                R35-2  P9-1  C10-1  R78-2
```

```
R36 7 1K 2 QW M12
     1          C78-1  U103-2  R34-2  R36-1
     2          GND

R37 7 4.3K 2 QW L9
     1          +12V
     2          U105-8  R37-2  R38-1  C76-1

R38 7 1.1K 2 QW L9
     1          U105-8  R37-2  R38-1  C76-1
     2          GND

R39 7 1.2M 2 QW L9
     1          +12V
     2          U105-6  R39-2  C9-1

R40 8 1M 2 QW L11
     1           ANYKEY
                U107-4  R40-1  X2-2  U106-11  U109-3
     2          U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
                X3-1  C75-1

R43 8 1K 2 QW G13
     1          Q9-3  R43-1  U111-10
     2          GND

R44 8 2.2M 2 QW A6
     1          +5V
     2           UPRST*
                C20-1  U113-6  U113-2  R44-2  X4-2  X6-1

R45 8 15K 2 QW A5
     1          +5V
     2          U113-13  R45-2  R46-1

R46 8 3.3M 2 QW A5
     1          U113-13  R45-2  R46-1
     2          U113-8  R46-2  U113-12  C21-1

R47 8 100K 2 QW H14
     1          U107-3  R47-1
     2          U107-2  C16-2  R47-2

R48 9 180 2 QW A13
     1          +12V
     2          Q11-1  R48-2  Q10-1

R49 9 47 2 QW A13
     1          Q10-2  R90-2  R91-1  C23-1  R49-1
     2

                Y1-2  Q11-2  R49-2
```

```
R51 9 75 2 QW A13
    1
             Q11-3  R51-1  U146-10  U146-5  U146-2
    2        GND

R52 9 47 2 QW A12
    1        R52-1  Q10-3  Y1-1
    2        NO CONNECTION

R53 9 1K 2 QW C14
    1        +5V
    2         UUTRST*
             U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
             U120-1  U118-1  U117-1

R54 9 1K 2 QW C9
    1         HPEDIS
             U135-2  J21-1  R54-1
    2        GND

R55 5 1K 2 QW K8
    1         COLORBURST
             R55-1  U147-12
    2        P3-9  R55-2  C5-1  L1-1

R57 7 10K 2 QW L8
    1        +5V
    2         PDLOT*
             U101-13  U105-7  R57-2

R58 2 27 2 QW C14
    1         RRAS0.3*
             R58-1  U12-3
    2         RAS0.3*
             J17-12  R58-2  B1-2

R59 2 27 2 QW C14
    1         RRAS1.2*
             R59-1  U12-6
    2         RAS1.2*
             J17-13  R59-2

R60 2 27 2 QW E12
    1         RRAS4.5*
             R60-1  U12-8
    2         RAS4.5*
             J17-14  R60-2

R61 2 27 2 QW D12
    1         RRAS6.7*
             R61-1  U12-11
```

```
     2          RAS6.7*
               J17-15  R61-2

R63 9 3K 2 QW G11
     1          FIELDIN
               J19-3  U121-18  R63-1
     2         GND

R65 6 1K 2 QW H9
     1         +5V
     2          MOTON*
               U179-1  U92-15  U178-15  R65-2  U164-12  U92-16

R66 6 1K 2 QW L11
     1         U92-9  U91-9  R66-1
     2         GND

R67 6 1K 2 QW L9
     1         +5V
     2         U161-11  U92-5  R67-2

R68 9 3K 2 QW F7
     1          PCS6522
               R68-1  U180-14
     2          CS6522
               R68-2  U73-24  C59-1  U97-24

R69 7 33 2 QW M11
     1          AUDIO
               J9-1  R69-1
     2         R69-2  U103-6

R75 7 1MEG 2 QW A8
     1         +5V
     2         C69-2  R75-2  U181-1  U181-2

R76 7 1.5K 2 QW A8
     1         +5V
     2         R76-2  R77-1  U181-13

R77 7 6.8K 2 QW A8
     1         R76-2  R77-1  U181-13
     2         R77-2  U181-8  U181-12  C70-1

R78 7 6.8K 2 QW A7
     1         U181-9  R78-1
     2          SUMSND
               R35-2  P9-1  C10-1  R78-2

R79 4 3K 2 QW A4
     1         +5V
     2          CKIRQ*
```

```
               U72-13  R79-2  U97-40

R80 8 10K 2 QW M14
     1          KRESET*
               U139-12  R80-1  C71-1  U179-15  J7-15
     2         +5V

R81 1 240 2 QW N4
     1         X7-2  R81-1
     2         GND

R85 7 3K 2 QW N4
     1         +5V
     2          SW1/MGNSWUF
               R85-2  U169-19  U73-39  U101-3

R86 7 1.1K 2 QW J9
     1         R86-1  U160-6  U161-2
     2         GND

R87 7 15K 2 QW J1
     1         +12V
     2          PCTS
               R87-2  U172-15  U100-4

R88 7 15K 2 QW J1
     1         +12V
     2          PDSR
               R88-2  U172-16  U100-10

R89 7 15K 2 QW J2
     1         +12V
     2          PDCD
               R89-2  U172-18  U100-13

R90 9 1.5K 2 QW A13
     1         +12V
     2         Q10-2  R90-2  R91-1  C23-1  R49-1

R91 9 1.1K 2 QW A12
     1         Q10-2  R90-2  R91-1  C23-1  R49-1
     2         GND

R92 8 1K 2 QW A4
     1          TRESET
               U113-5  R92-1
     2          UUTUPRST
               R92-2  U162-11  J21-4  U164-3

R93 1 120 2 QW L1
     1          Q3
               J14-37  U85-3  J15-37  J13-37  J12-37  U117-12  R93-1
```

```
                  U154-2
     2            R93-2  C67-1

R94 1 120 2 QW L1
     1             PRE1M
                  J12-40  J13-40  J14-40  J15-40  U119-12  U73-25  U123-5
                  U97-25  U139-10  R94-1
     2            R94-2  C68-1

R95 1 120 2 QW L1
     1             PRE1M*
                  J12-38  J13-38  J14-38  J15-38  U123-6  R95-1
     2            R95-2  C77-1

R96 1 120 2 QW M5
     1             PH0
                  J15-19  U136-11  J14-19  J13-19  J12-19  U124-5  U65-37
                  R96-1
     2            R96-2  C66-1

R97 2 33 2 QW E13
     1             AR0
                  P16-4  R97-1  U2-7
     2             AR0
                  R97-2  J17-10

R98 2 33 2 QW E13
     1             AR1
                  P16-8  R98-1  U2-9
     2             AR1
                  R98-2  J17-9

R99 2 33 2 QW F12
     1             AR5
                  R99-1  U9-9  P16-7
     2             AR5
                  R99-2  J17-5

R100 2 100 2 QW D12
     1             C14M
                  U146-6  R100-1  U117-10  U119-9  U79-7  U85-11
     2            R100-2  C74-1  U4-11

R101 4 100K 2 QW A2
     1            Q3-2  Q2-3  R101-1
     2            GND

R102 6 470 2 QW L9
     1            +5V
     2             Q3*
                  U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                  U131-5  R102-2  R103-1  U146-1
```

```
R103 6 300 2 QW L9
     1          Q3*
                U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                U131-5  R102-2  R103-1  U146-1
     2          GND

R106 1 1K 2 QW J8
     1          +5V
     2           S5A
                R106-2  U165-2  U165-3  U165-4  U165-5  U173-4  U173-13
                U173-10

R107 1 1K 2 QW H12
     1          +5V
     2           S5B
                R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                U114-7  U116-5

R108 1 1K 2 QW D5
     1          +5V
     2           S5C
                R108-2  U140-1  U140-4  U140-10  U140-13

R109 1 1K 2 QW A10
     1          +5V
     2           S5D
                R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
                U123-10  U123-13  U117-4  U117-5  U117-6  U117-7

T1 4 4V 2 BAT G14
     1          R9-1  T1-1  X1-1  U105-10
     2          GND

U1 2 LS283 16 E11
     1           SUM2
                U1-1  U9-5
     2           V4
                U87-19  U1-2  U154-4  U120-12  U1-11
     3           H4
                U121-5  U1-3  U116-14
     4           SUM1
                U1-4  U5-11
     5           H3
                U114-11  U1-5  U121-6
     6           V3
                U120-13  U1-15  U154-5  U1-6
     7          GND
     8          GND
     9          NO CONNECTION
     10          SUM4
                U1-10  U2-3
```

11 V4
U87-19 U1-2 U154-4 U120-12 U1-11
12 GND
13 SUM3
U1-13 U9-11
14 H5
U121-4 U1-14 U116-13
15 V3
U120-13 U1-15 U154-5 U1-6
16 +5V

U2 2 S153 16 F13
1 GND
2 AX*
U124-8 U2-2 U13-2 U9-2 U5-2 J17-23
3 SUM4
U1-10 U2-3
4 A6
J15-8 J14-8 J13-8 J12-8 U2-4 U77-3 U76-3
U71-10 U63-5 U71-11
5 H0
U114-14 U2-5
6 A0
J15-2 J14-2 J13-2 J12-2 U2-6 U97-38 U98-13
U101-11 U94-13 U73-38 U75-13 U63-18 U177-13
7 AR0
P16-4 R97-1 U2-7
8 GND
9 AR1
P16-8 R98-1 U2-9
10 A1
J15-3 J14-3 J13-3 J12-3 U2-10 U97-37 U98-14
U101-10 U177-1 U94-1 U73-37 U75-1 U63-16
11 H1
U114-13 U2-11 U155-9
12 A8
J15-10 J14-10 J13-10 J12-10 U67-4 U74-1 U71-6
U2-12 U13-6 U13-4
13 V1
U121-22 U2-13 U118-11 U13-5 U13-3
14 AY*
U13-14 U11-3 U9-14 U5-14 U2-14 U153-3 U6-15
U3-1
15 GND
16 +5V

U3 2 7643 18 341-~~0056~~ 0041 C12
1 AY*
U13-14 U11-3 U9-14 U5-14 U2-14 U153-3 U6-15
U3-1
2 RDHIRES
U175-1 U11-17 U3-2 U6-3 U126-9

```
     3          R/W*
               J15-18  J14-18  J13-18  J12-18  U3-3  U136-9  U180-17
               U176-6  U165-11  U160-11
     4          A15
               J15-17  J14-17  J13-17  J12-17  U3-4  U147-3  U70-12
               U174-16  U6-7
     5          A11
               J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
               U150-13  U74-5  U67-12  U3-5  U174-5
     6          A13
               J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
               U71-1  U70-7  U6-5  U3-6  U174-7
     7          A14
               J15-16  J14-16  J13-16  J12-16  U3-7  U147-4  U70-9
               U6-16  U174-4
     8          Q1
               U6-8  U131-4  U3-8  U124-12  U117-14
     9         GND
     10        GND
     11         PCAS3*
               U128-2  U128-13  P1-6  U3-11  U4-8
     12         PCAS0,3*
               P1-9  U3-12  B1-1
     13         PUSELB
               U4-17  P1-8  U3-13
     14         PCAS0*
               P1-7  U4-3  U3-14
     15         PRAS0.3
               U128-5  U11-14  U12-1  U3-15  U6-4
     16         PRAS1.2
               U12-4  U11-13  U3-16
     17         ABK2
               U6-1  U11-6  U10-7  U3-17
     18        +5V

U4 2 S374 20 D13
     1         GND
     2          CAS0*
               J17-17  U4-2
     3          PCAS0*
               P1-7  U4-3  U3-14
     4          PCAS1*
               P1-3  U4-4  U6-12  U128-10
     5          CAS1*
               J17-18  U4-5
     6          CAS2*
               J17-19  U4-6
     7          PCAS2*
               P1-4  U4-7  U6-11
     8          PCAS3*
               U128-2  U128-13  P1-6  U3-11  U4-8
     9          CAS3*
```

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                J17-20  U4-9
    10          GND
    11          R100-2  C74-1  U4-11
    12           CAS4,6*
                J17-21  U4-12
    13           PCAS4,6*
                U4-13  U6-14  P1-2
    14           PCAS5,7*
                U4-14  P1-5  U6-13
    15           CAS5,7*
                U4-15  J17-22
    16           USELB
                U4-16  U66-1  U69-1
    17           PUSELB
                U4-17  P1-8  U3-13
    18          NO CONNECTION
    19          NO CONNECTION
    20          +5V

U5 2 S153 16 E12
    1           GND
    2            AX*
                U124-8  U2-2  U13-2  U9-2  U5-2  J17-23
    3            V2*V5
                U121-8  U154-8  U5-3
    4            A9
                J15-11  J14-11  J13-11  J12-11  U5-4  U74-2  U71-5
                U67-7
    5            H2
                U121-7  U5-5  U114-12  U85-8
    6            A2
                J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
                U177-2  U94-2  U75-2  U73-36  U63-14
    7            AR2
                J17-8  U5-7  P16-2
    8           GND
    9            AR3
                J17-7  U5-9  P16-3
    10           A3
                J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
                U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
    11           SUM1
                U1-4  U5-11
    12          U5-12  U128-3
    13           MUX1
                U101-12  U175-14  U5-13
    14           AY*
                U13-14  U11-3  U9-14  U5-14  U2-14  U153-3  U6-15
                U3-1
    15          GND
    16          +5V
```

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U6 2 7643 18 341-0042 C13
     1           ABK2
                U6-1  U11-6  U10-7  U3-17
     2           ABK1
                U6-2  U11-5  U10-2
     3           RDHIRES
                U175-1  U11-17  U3-2  U6-3  U126-9
     4           PRAS0.3
                U128-5  U11-14  U12-1  U3-15  U6-4
     5           A13
                J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
                U71-1  U70-7  U6-5  U3-6  U174-7
     6           A11
                J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
                U150-13  U74-5  U67-12  U3-5  U174-5
     7           A15
                J15-17  J14-17  J13-17  J12-17  U3-4  U147-3  U70-12
                U174-16  U6-7
     8           Q1
                U6-8  U131-4  U3-8  U124-12  U117-14
     9          GND
     10         GND
     11          PCAS2*
                P1-4  U4-7  U6-11
     12          PCAS1*
                P1-3  U4-4  U6-12  U128-10
     13          PCAS5,7*
                U4-14  P1-5  U6-13
     14          PCAS4,6*
                U4-13  U6-14  P1-2
     15          AY*
                U13-14  U11-3  U9-14  U5-14  U2-14  U153-3  U6-15
                U3-1
     16          A14
                J15-16  J14-16  J13-16  J12-16  U3-7  U147-4  U70-9
                U6-16  U174-4
     17          ABK3
                U6-17  U11-7  U10-10
     18         +5V

U9 2 S153 16 F12
     1          GND
     2           AX*
                U124-8  U2-2  U13-2  U9-2  U5-2  J17-23
     3           MUX2
                U9-3  U175-13
     4          U9-4  U128-11
     5           SUM2
                U1-1  U9-5
     6           A4
                J15-6  J14-6  J13-6  J12-6  U9-6  U77-1  U76-1
                U112-2  U63-9
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    7          AR4
              J17-6  U9-7  P16-6
    8         GND
    9          AR5
              R99-1  U9-9  P16-7
    10         A5
              J15-7  J14-7  J13-7  J12-7  U9-10  U76-2  U77-2
              U112-3  U63-7
    11         SUM3
              U1-13  U9-11
    12         A12
              J15-14  J14-14  J13-14  J12-14  U9-12  U155-11  U165-14
              U70-4  U71-2  U174-6
    13         MUX3
              U9-13  U175-12
    14         AY*
              U13-14  U11-3  U9-14  U5-14  U2-14  U153-3  U6-15
              U3-1
    15        GND
    16        +5V

U10 2 LS399 16 A9
    1         U10-1  U153-6
    2          ABK1
              U6-2  U11-5  U10-2
    3          BKSW1
              U97-2  U10-3
    4          DA0
              J16-9  U10-4  U84-13  U66-2
    5          DA1
              J16-10  U10-5  U84-8  U66-5
    6          BKSW2
              U97-3  U10-6
    7          ABK2
              U6-1  U11-6  U10-7  U3-17
    8         GND
    9          CLKBK
              U136-8  U10-9
    10         ABK3
              U6-17  U11-7  U10-10
    11         BKSW3
              U97-4  U10-11
    12         DA2
              J16-11  U10-12  U84-14  U66-11
    13         S5D
              R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
              U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
    14        GND
    15         ABK4
              U11-15  U174-1  U10-15  U158-10
    16        +5V
```

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U11 2 7643 18 341-0044 C11
     1           ZPAGE*
                U11-1  U174-15  U67-1  U131-8  U70-1
     2           PA8
                U11-2  U174-17  U67-3  U158-6
     3           AY*
                U13-14  U11-3  U9-14  U5-14  U2-14  U153-3  U6-15
                U3-1
     4           PA15
                U135-10  U11-4  U70-13  U65-25
     5           ABK1
                U6-2  U11-5  U10-2
     6           ABK2
                U6-1  U11-6  U10-7  U3-17
     7           ABK3
                U6-17  U11-7  U10-10
     8          GND
     9          GND
     10         GND
     11          PRAS6.7
                U12-12  U11-11
     12          PRAS4.5
                U12-9  U11-12
     13          PRAS1.2
                U12-4  U11-13  U3-16
     14          PRAS0.3
                U128-5  U11-14  U12-1  U3-15  U6-4
     15          ABK4
                U11-15  U174-1  U10-15  U158-10
     16          RFSH
                U158-13  U11-16  U126-2
     17          RDHIRES
                U175-1  U11-17  U3-2  U6-3  U126-9
     18         +5V

U12 2 S00 14 D12
     1           PRAS0.3
                U128-5  U11-14  U12-1  U3-15  U6-4
     2           RAS
                U152-13  U150-9  U119-14  U12-2  U12-5  U12-10  U12-13
     3           RRAS0.3*
                R58-1  U12-3
     4           PRAS1.2
                U12-4  U11-13  U3-16
     5           RAS
                U152-13  U150-9  U119-14  U12-2  U12-5  U12-10  U12-13
     6           RRAS1.2*
                R59-1  U12-6
     7          GND
     8           RRAS4.5*
                R60-1  U12-8
     9           PRAS4.5
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                U12-9  U11-12
     10          RAS
                U152-13  U150-9  U119-14  U12-2  U12-5  U12-10  U12-13
     11          RRAS6.7*
                R61-1  U12-11
     12          PRAS6.7
                U12-12  U11-11
     13          RAS
                U152-13  U150-9  U119-14  U12-2  U12-5  U12-10  U12-13
     14         +5V

U13 2 S153 16 E13
     1          GND
     2           AX*
                U124-8  U2-2  U13-2  U9-2  U5-2  J17-23
     3           V1
                U121-22  U2-13  U118-11  U13-5  U13-3
     4           A8
                J15-10  J14-10  J13-10  J12-10  U67-4  U74-1  U71-6
                U2-12  U13-6  U13-4
     5           V1
                U121-22  U2-13  U118-11  U13-5  U13-3
     6           A8
                J15-10  J14-10  J13-10  J12-10  U67-4  U74-1  U71-6
                U2-12  U13-6  U13-4
     7           AR7
                U13-7  J17-24
     8          GND
     9           AR6
                J17-4  U13-9  P16-5
     10          A7
                J15-9  J14-9  J13-9  J12-9  U13-10  U77-4  U76-6
                U71-7  U63-3
     11          V0
                U121-23  U13-11  U118-12
     12         U13-12  U128-8
     13          PG2*
                U87-9  U13-13
     14          AY*
                U13-14  U11-3  U9-14  U5-14  U2-14  U153-3  U6-15
                U3-1
     15         GND
     16         +5V
                  -  74LS244
U63 3 LS244 20 D6
     1          U70-15  U163-4  U67-15  U63-19  U63-1
     2           PA0
                U64-8  U63-2  U65-9
     3           A7
                J15-9  J14-9  J13-9  J12-9  U13-10  U77-4  U76-6
                U71-7  U63-3
     4           PA1
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              U64-7  U63-4  U65-10
     5         A6
              J15-8  J14-8  J13-8  J12-8  U2-4  U77-3  U76-3
              U71-10  U63-5  U71-11
     6         PA2
              U64-6  U63-6  U65-11
     7         A5
              J15-7  J14-7  J13-7  J12-7  U9-10  U76-2  U77-2
              U112-3  U63-7
     8         PA3
              U64-5  U63-8  U65-12
     9         A4
              J15-6  J14-6  J13-6  J12-6  U9-6  U77-1  U76-1
              U112-2  U63-9
     10       GND
     11        PA4
              U64-4  U63-11  U65-13
     12        A3
              J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
              U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     13        PA5
              U64-3  U63-13  U65-14
     14        A2
              J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
              U177-2  U94-2  U75-2  U73-36  U63-14
     15        PA6
              U64-2  U63-15  U65-15
     16        A1
              J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
              U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     17        PA7
              U64-1  U63-17  U65-16
     18        A0
              J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
              U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
     19       U70-15  U163-4  U67-15  U63-19  U63-1
     20       +5V

U64 3 2332 24 B9
     1         PA7
              U64-1  U63-17  U65-16
     2         PA6
              U64-2  U63-15  U65-15
     3         PA5
              U64-3  U63-13  U65-14
     4         PA4
              U64-4  U63-11  U65-13
     5         PA3
              U64-5  U63-8  U65-12
     6         PA2
              U64-6  U63-6  U65-11
     7         PA1
```

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             U64-7  U63-4  U65-10
     8        PA0
             U64-8  U63-2  U65-9
     9        ID0
             U98-18  U65-33  U97-33  U72-15  U73-33  U64-9  U68-1
    10        ID1
             U98-19  U65-32  U97-32  U72-16  U73-32  U64-10  U68-2
    11        ID2
             U98-20  U65-31  U97-31  U72-17  U73-31  U64-11  U68-3
    12       NO CONNECTION
    13        ID3
             U98-21  U65-30  U97-30  U72-18  U73-30  U64-13  U68-4
    14        ID4
             U98-22  U65-29  U97-29  U72-19  U73-29  U64-14  U68-5
    15        ID5
             U98-23  U65-28  U97-28  U72-20  U73-28  U64-15  U68-6
    16        ID6
             U98-24  U65-27  U97-27  U72-21  U73-27  U64-16  U68-7
    17        ID7
             U98-25  U65-26  U97-26  U72-22  U73-26  U64-17  U68-8
    18        PA11
             U64-18  U144-12  U65-20  U67-13  U135-4
    19        PA10
             U64-19  U155-6  U65-19  U67-10
    20        TROMSEL*
             U153-8  U162-13  U64-20
    21        ROMSEL2
             U73-3  U64-21  P19-8
    22        PA9
             U64-22  U155-5  U65-18  U67-6
    23        PPA8
             U158-4  U152-4  U158-5  U65-17  U64-23  U132-5
    24       +5V

U65 3 6502B 40 B8
     1       GND
     2        RDY
             J15-21  U164-8  J14-21  J13-21  J12-21  P14-4  U65-2
     3       NO CONNECTION
     4        IRQ*
             U97-21  U65-4  U98-26  U97-9  U73-21
     5       NO CONNECTION
     6        NMI*
             U139-6  U65-6  U155-2
     7        SYNC
             U65-7  U136-1  J15-35  U174-3  J14-35  J13-35  J12-35
     8       +5V
     9        PA0
             U64-8  U63-2  U65-9
    10        PA1
             U64-7  U63-4  U65-10
    11        PA2
```

U64-6 U63-6 U65-11
12 PA3
U64-5 U63-8 U65-12
13 PA4
U64-4 U63-11 U65-13
14 PA5
U64-3 U63-13 U65-14
15 PA6
U64-2 U63-15 U65-15
16 PA7
U64-1 U63-17 U65-16
17 PPA8
U158-4 U152-4 U158-5 U65-17 U64-23 U132-5
18 PA9
U64-22 U155-5 U65-18 U67-6
19 PA10
U64-19 U155-6 U65-19 U67-10
20 PA11
U64-18 U144-12 U65-20 U67-13 U135-4
21 GND
22 PA12
U65-22 U135-9 U70-3
23 PA13
U65-23 U135-8 U70-6
24 PA14
U65-24 U135-11 U70-10
25 PA15
U135-10 U11-4 U70-13 U65-25
26 ID7
U98-25 U65-26 U97-26 U72-22 U73-26 U64-17 U68-8
27 ID6
U98-24 U65-27 U97-27 U72-21 U73-27 U64-16 U68-7
28 ID5
U98-23 U65-28 U97-28 U72-20 U73-28 U64-15 U68-6
29 ID4
U98-22 U65-29 U97-29 U72-19 U73-29 U64-14 U68-5
30 ID3
U98-21 U65-30 U97-30 U72-18 U73-30 U64-13 U68-4
31 ID2
U98-20 U65-31 U97-31 U72-17 U73-31 U64-11 U68-3
32 ID1
U98-19 U65-32 U97-32 U72-16 U73-32 U64-10 U68-2
33 ID0
U98-18 U65-33 U97-33 U72-15 U73-33 U64-9 U68-1
34 IR/W*
U98-28 U97-22 U112-14 U73-22 U163-11 U65-34 U160-12
35 NO CONNECTION
36 NO CONNECTION
37 PH0
J15-19 U136-11 J14-19 J13-19 J12-19 U124-5 U65-37
R96-1
38 GND

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    39          PH2M
               P19-10  U141-5  U65-39  U176-17
    40          RESET*
               U65-40  U162-10  U98-4  U97-34  U73-34  U75-15  U79-9
               U173-1

U66 3 S257 16 D3
    1           USELB
               U4-16  U66-1  U69-1
    2           DA0
               J16-9  U10-4  U84-13  U66-2
    3           DB0
               J16-1  U66-3  U80-13
    4           D0
               J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
               U91-16  U66-4  P15-2
    5           DA1
               J16-10  U10-5  U84-8  U66-5
    6           DB1
               J16-2  U66-6  U80-8
    7           D1
               J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
               U91-4  U66-7  P15-3
    8          GND
    9           D2
               J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
               U91-15  U66-9  P15-4
    10          DB2
               J16-3  U66-10  U80-14
    11          DA2
               J16-11  U10-12  U84-14  U66-11
    12          D3
               J15-46  J14-46  J13-46  J12-46  U68-16  J16-20  U109-12
               U91-5  U66-12  P15-5
    13          DB3
               J16-4  U66-13  U80-7
    14          DA3
               J16-12  U66-14  U84-7
    15          EN257
               U176-14  U66-15  U69-15
    16         +5V

U67 3 S257 16 D8
    1           ZPAGE*
               U11-1  U174-15  U67-1  U131-8  U70-1
    2          U67-2  U132-6
    3           PA8
               U11-2  U174-17  U67-3  U158-6
    4           A8
               J15-10  J14-10  J13-10  J12-10  U67-4  U74-1  U71-6
               U2-12  U13-6  U13-4
    5           Z1
```

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               U72-6  U67-5  U73-11
     6          PA9
               U64-22  U155-5  U65-18  U67-6
     7          A9
               J15-11  J14-11  J13-11  J12-11  U5-4  U74-2  U71-5
               U67-7
     8         GND
     9          A10
               J15-12  J14-12  J13-12  J12-12  U128-1  U74-3  U71-4
               U67-9
     10         PA10
               U64-19  U155-6  U65-19  U67-10
     11         Z2
               U72-7  U67-11  U73-12
     12         A11
               J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
               U150-13  U74-5  U67-12  U3-5  U174-5
     13         PA11
               U64-18  U144-12  U65-20  U67-13  U135-4
     14         Z3
               U72-8  U67-14  U73-13
     15        U70-15  U163-4  U67-15  U63-19  U63-1
     16        +5V

U68 3 8304 20 C3
     1          ID0
               U98-18  U65-33  U97-33  U72-15  U73-33  U64-9  U68-1
     2          ID1
               U98-19  U65-32  U97-32  U72-16  U73-32  U64-10  U68-2
     3          ID2
               U98-20  U65-31  U97-31  U72-17  U73-31  U64-11  U68-3
     4          ID3
               U98-21  U65-30  U97-30  U72-18  U73-30  U64-13  U68-4
     5          ID4
               U98-22  U65-29  U97-29  U72-19  U73-29  U64-14  U68-5
     6          ID5
               U98-23  U65-28  U97-28  U72-20  U73-28  U64-15  U68-6
     7          ID6
               U98-24  U65-27  U97-27  U72-21  U73-27  U64-16  U68-7
     8          ID7
               U98-25  U65-26  U97-26  U72-22  U73-26  U64-17  U68-8
     9          EN8304
               U176-13  U68-9
     10        GND
     11         IR*/W
               U91-3  U68-11  U158-2  U163-10
     12         D7
               J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
               U101-5  U91-7  U69-12  P15-9
     13         D6
               J15-43  J14-43  J13-43  J12-43  U68-13  J16-23  U111-9
               U91-13  U69-9  P15-8
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          14          D5
                     J15-44  J14-44  J13-44  J12-44  U68-14  J16-22  U111-7
                     U91-6  U69-7  P15-7
          15          D4
                     J15-45  J14-45  J13-45  J12-45  U68-15  J16-21  U111-4
                     U91-14  U69-4  P15-6
          16          D3
                     J15-46  J14-46  J13-46  J12-46  U68-16  J16-20  U109-12
                     U91-5  U66-12  P15-5
          17          D2
                     J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
                     U91-15  U66-9  P15-4
          18          D1
                     J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
                     U91-4  U66-7  P15-3
          19          D0
                     J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
                     U91-16  U66-4  P15-2
          20         +5V

     U69 3 S257 16 D2
          1           USELB
                     U4-16  U66-1  U69-1
          2           DA4
                     J16-13  U69-2  U84-17
          3           DB4
                     J16-5  U69-3  U80-17
          4           D4
                     J15-45  J14-45  J13-45  J12-45  U68-15  J16-21  U111-4
                     U91-14  U69-4  P15-6
          5           DA5
                     J16-14  U69-5  U84-4
          6           DB5
                     J16-6  U69-6  U80-4
          7           D5
                     J15-44  J14-44  J13-44  J12-44  U68-14  J16-22  U111-7
                     U91-6  U69-7  P15-7
          8          GND
          9           D6
                     J15-43  J14-43  J13-43  J12-43  U68-13  J16-23  U111-9
                     U91-13  U69-9  P15-8
          10          DB6
                     J16-7  U69-10  U80-18
          11          DA6
                     J16-15  U69-11  U84-18
          12          D7
                     J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
                     U101-5  U91-7  U69-12  P15-9
          13          DB7
                     J16-8  U69-13  U80-3
          14          DA7
                     J16-16  U153-5  U84-3  U69-14
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    15          EN257
                U176-14  U66-15  U69-15
    16          +5V

U70 3 S257 16 D7
    1           ZPAGE*
                U11-1  U174-15  U67-1  U131-8  U70-1
    2           Z4
                U72-9  U70-2  U73-14
    3           PA12
                U65-22  U135-9  U70-3
    4           A12
                J15-14  J14-14  J13-14  J12-14  U9-12  U155-11  U165-14
                U70-4  U71-2  U174-6
    5           Z5
                U73-15  U70-5
    6           PA13
                U65-23  U135-8  U70-6
    7           A13
                J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
                U71-1  U70-7  U6-5  U3-6  U174-7
    8           GND
    9           A14
                J15-16  J14-16  J13-16  J12-16  U3-7  U147-4  U70-9
                U6-16  U174-4
    10          PA14
                U65-24  U135-11  U70-10
    11          Z6
                U73-16  U70-11
    12          A15
                J15-17  J14-17  J13-17  J12-17  U3-4  U147-3  U70-12
                U174-16  U6-7
    13          PA15
                U135-10  U11-4  U70-13  U65-25
    14          Z7
                U73-17  U70-14
    15          U70-15  U163-4  U67-15  U63-19  U63-1
    16          +5V

U71 4 LS133 16 G7
    1           A13
                J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
                U71-1  U70-7  U6-5  U3-6  U174-7
    2           A12
                J15-14  J14-14  J13-14  J12-14  U9-12  U155-11  U165-14
                U70-4  U71-2  U174-6
    3           A11
                J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
                U150-13  U74-5  U67-12  U3-5  U174-5
    4           A10
                J15-12  J14-12  J13-12  J12-12  U128-1  U74-3  U71-4
                U67-9
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     5          A9
                J15-11  J14-11  J13-11  J12-11  U5-4  U74-2  U71-5
                U67-7
     6          A8
                J15-10  J14-10  J13-10  J12-10  U67-4  U74-1  U71-6
                U2-12  U13-6  U13-4
     7          A7
                J15-9  J14-9  J13-9  J12-9  U13-10  U77-4  U76-6
                U71-7  U63-3
     8          GND
     9          U112-1  U71-9
     10         A6
                J15-8  J14-8  J13-8  J12-8  U2-4  U77-3  U76-3
                U71-10  U63-5  U71-11
     11         A6
                J15-8  J14-8  J13-8  J12-8  U2-4  U77-3  U76-3
                U71-10  U63-5  U71-11
     12         AIISW*
                U165-6  U71-12  U97-8  U178-1  U178-13  U177-15  U87-3
                U155-3
     13         C-FXXX
                U71-15  U180-2  U71-14  U71-13  U147-6  U147-9  U165-1
     14         C-FXXX
                U71-15  U180-2  U71-14  U71-13  U147-6  U147-9  U165-1
     15         C-FXXX
                U71-15  U180-2  U71-14  U71-13  U147-6  U147-9  U165-1
     16         +5V

U72 4 58167 24 B3
     1          C07X*
                U180-6  U77-7  U112-13  U158-1  U72-1  U150-5  U148-13
     2          CLKRD
                U72-2  U158-3
     3          U72-3  U112-12
     4          NO CONNECTION
     5          Z0
                U72-5  U132-4  U73-10
     6          Z1
                U72-6  U67-5  U73-11
     7          Z2
                U72-7  U67-11  U73-12
     8          Z3
                U72-8  U67-14  U73-13
     9          Z4
                U72-9  U70-2  U73-14
     10         Y2-1  U72-10  C3-3
     11         C4-1  U72-11  Y2-2
     12         GND
     13         CKIRQ*
                U72-13  R79-2  U97-40
     14         PDINT*
                J5-4  U72-14
     15          ID0
                U98-18  U65-33  U97-33  U72-15  U73-33  U64-9  U68-1
     16          ID1
                U98-19  U65-32  U97-32  U72-16  U73-32  U64-10  U68-2
     17          ID2
                U98-20  U65-31  U97-31  U72-17  U73-31  U64-11  U68-3
     18          ID3
                U98-21  U65-30  U97-30  U72-18  U73-30  U64-13  U68-4
     19          ID4
                U98-22  U65-29  U97-29  U72-19  U73-29  U64-14  U68-5
     20          ID5
                U98-23  U65-28  U97-28  U72-20  U73-28  U64-15  U68-6
     21          ID6
                U98-24  U65-27  U97-27  U72-21  U73-27  U64-16  U68-7
     22          ID7
                U98-25  U65-26  U97-26  U72-22  U73-26  U64-17  U68-8
     23          PWRDN*
                U72-23  Q3-3  C2-1  R6-2
     24         U72-24  Q1-1  X1-2

U73 4 6522 40 B6
     1          GND
     2           ROMSEL1
                U165-10  U73-2  P19-9
     3           ROMSEL2
                U73-3  U64-21  P19-8
     4           PRIMSTK
                U73-4  P19-7  U158-9
     5           RWPR
                U73-5  P19-6  U180-16
     6           RESETLK*
                U179-14  U73-6  P19-5  U139-5
     7           SCRN
                U154-13  U73-7  P19-4
     8           IOEN
                U73-8  P19-3  U147-10
     9           SEL1M
                U180-15  U174-2  U150-3  U73-9  P19-2
     10          Z0
                U72-5  U132-4  U73-10
     11          Z1
                U72-6  U67-5  U73-11
     12          Z2
                U72-7  U67-11  U73-12
     13          Z3
                U72-8  U67-14  U73-13
     14          Z4
                U72-9  U70-2  U73-14
     15          Z5
                U73-15  U70-5
     16          Z6
                U73-16  U70-11
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17          Z7
           U73-17  U70-14
18          SCO
           U160-3  U73-18  U160-5  U101-1
19          SER
           U73-19  U160-8  U161-9
20         +5V
21          IRQ*
           U97-21  U65-4  U98-26  U97-9  U73-21
22          IR/W*
           U98-28  U97-22  U112-14  U73-22  U163-11  U65-34  U160-12
23          FFDX*
           U112-5  U73-23  U148-9
24          CS6522
           R68-2  U73-24  C59-1  U97-24
25          PRE1M
           J12-40  J13-40  J14-40  J15-40  U119-12  U73-25  U123-5
           U97-25  U139-10  R94-1
26          ID7
           U98-25  U65-26  U97-26  U72-22  U73-26  U64-17  U68-8
27          ID6
           U98-24  U65-27  U97-27  U72-21  U73-27  U64-16  U68-7
28          ID5
           U98-23  U65-28  U97-28  U72-20  U73-28  U64-15  U68-6
29          ID4
           U98-22  U65-29  U97-29  U72-19  U73-29  U64-14  U68-5
30          ID3
           U98-21  U65-30  U97-30  U72-18  U73-30  U64-13  U68-4
31          ID2
           U98-20  U65-31  U97-31  U72-17  U73-31  U64-11  U68-3
32          ID1
           U98-19  U65-32  U97-32  U72-16  U73-32  U64-10  U68-2
33          ID0
           U98-18  U65-33  U97-33  U72-15  U73-33  U64-9  U68-1
34          RESET*
           U65-40  U162-10  U98-4  U97-34  U73-34  U75-15  U79-9
           U173-1
35          A3
           J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
           U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
36          A2
           J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
           U177-2  U94-2  U75-2  U73-36  U63-14
37          A1
           J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
           U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
38          A0
           J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
           U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
39          SW1/MGNSWUF
           R85-2  U169-19  U73-39  U101-3
40          IOIRQ
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             U73-40  U155-10

U74 4 LS138 16 J6
     1        A8
             J15-10  J14-10  J13-10  J12-10  U67-4  U74-1  U71-6
             U2-12  U13-6  U13-4
     2        A9
             J15-11  J14-11  J13-11  J12-11  U5-4  U74-2  U71-5
             U67-7
     3        A10
             J15-12  J14-12  J13-12  J12-12  U128-1  U74-3  U71-4
             U67-9
     4        GPH1
             U162-3  U76-4  U141-6  U74-4
     5        A11
             J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
             U150-13  U74-5  U67-12  U3-5  U174-5
     6        CXXX
             U176-15  U74-6  U150-1  U147-8
     7        C7XX*
             U176-16  U74-7
     8       GND
     9        C6XX*
             U176-7  U74-9
     10      U74-10  U176-5
     11       IOSEL4*
             U74-11  J15-1
     12       IOSEL3*
             U74-12  J14-1
     13       IOSEL2*
             U74-13  J13-1
     14       IOSEL1*
             U74-14  J12-1
     15       COXX*
             U77-5  U74-15  U76-5
     16      +5V

U75 4 9334 16 H6
     1        A1
             J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
             U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     2        A2
             J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
             U177-2  U94-2  U75-2  U73-36  U63-14
     3        A3
             J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
             U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     4        TEXT
             U87-23  U75-4
     5        MIX
             U87-1  U75-5
     6        PAGE2
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                U87-4  U75-6
     7           HIRES
                U87-2  U75-7
     8          GND
     9           PDLO
                U105-16  U75-9
     10          PDL2
                U160-4  U105-2  U75-10
     11          PDLEN
                U105-3  U75-11
     12          AXCO
                U161-5  U75-12  U105-1
     13          A0
                J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
                U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
     14          C05X*
                U77-10  U75-14
     15          RESET*
                U65-40  U162-10  U98-4  U97-34  U73-34  U75-15  U79-9
                U173-1
     16         +5V

U76 4 LS138 16 K4
     1           A4
                J15-6  J14-6  J13-6  J12-6  U9-6  U77-1  U76-1
                U112-2  U63-9
     2           A5
                J15-7  J14-7  J13-7  J12-7  U9-10  U76-2  U77-2
                U112-3  U63-7
     3           A6
                J15-8  J14-8  J13-8  J12-8  U2-4  U77-3  U76-3
                U71-10  U63-5  U71-11
     4           GPH1
                U162-3  U76-4  U141-6  U74-4
     5           COXX*
                U77-5  U74-15  U76-5
     6           A7
                J15-9  J14-9  J13-9  J12-9  U13-10  U77-4  U76-6
                U71-7  U63-3
     7           SEL6551*
                U98-3  U76-7  U148-12
     8          GND
     9           DEVSEL6*
                U94-14  U76-9  U91-2
     10          DEVSEL5*
                U177-14  U76-10
     11          DEVSEL4*
                J15-41  U76-11
     12          DEVSEL3*
                J14-41  U76-12
     13          DEVSEL2*
                J13-41  U76-13
     14          DEVSEL1*
                J12-41  U76-14
     15         NO CONNECTION
     16         +5V

U77 4 LS138 16 K7
     1           A4
                J15-6  J14-6  J13-6  J12-6  U9-6  U77-1  U76-1
                U112-2  U63-9
     2           A5
                J15-7  J14-7  J13-7  J12-7  U9-10  U76-2  U77-2
                U112-3  U63-7
     3           A6
                J15-8  J14-8  J13-8  J12-8  U2-4  U77-3  U76-3
                U71-10  U63-5  U71-11
     4           A7
                J15-9  J14-9  J13-9  J12-9  U13-10  U77-4  U76-6
                U71-7  U63-3
     5           C0XX*
                U77-5  U74-15  U76-5
     6           GPH2
                U150-2  U77-6  U162-4
     7           C07X*
                U180-6  U77-7  U112-13  U158-1  U72-1  U150-5  U148-13
     8          GND
     9           C06X*
                U101-7  U77-9
     10          C05X*
                U77-10  U75-14
     11          C04X*
                U77-11  U181-6
     12          SPKR*
                U173-11  U77-12
     13          C02X*
                J15-39  U77-13  J14-39  J13-39  J12-39
     14          CLRSTRB*
                U106-1  U77-14
     15           KBD*
                U109-15  U111-15  U77-15
     16         +5V

U78 5 LS374 20 E3
     1           ENHREG*
                U175-11  U78-1
     2           DC7
                U79-2  U78-2  U82-14  U136-4
     3           DV7
                U86-3  U78-3  U80-2  U84-2  U136-3  U136-2
     4           DV5
                U82-3  U86-4  U78-4  U81-3  U80-5  U84-5
     5           DC5
                U79-4  U78-5  U82-13
     6          DC3
               U79-10  U78-6  U82-12
     7          DV3
               U82-2  U86-7  U78-7  U81-2  U80-6  U84-6
     8          DV1
               U82-1  U86-8  U78-8  U81-1  U80-9  U84-9
     9          DC1
               U79-12  U78-9  U82-11
     10        GND
     11         Q0
               U119-13  U150-10  U117-15  U131-2  U78-11
     12         DC0
               U79-14  U78-12  U81-14
     13         DV0
               U82-17  U86-13  U78-13  U81-17  U80-12  U84-12
     14         DV2
               U82-16  U86-14  U78-14  U81-16  U80-15  U84-15
     15         DC2
               U79-11  U78-15  U81-13
     16         DC4
               U79-5  U78-16  U81-12
     17         DV4
               U82-15  U86-17  U78-17  U81-15  U80-16  U84-16
     18         DV6
               U78-18  U86-18  U82-4  U81-4  U80-19  U34-19
     19         DC6
               U78-19  U79-3  U81-11
     20        +5V

U79 5 74166 16 F4
     1         GND
     2          DC7
               U79-2  U78-2  U82-14  U136-4
     3          DC6
               U78-19  U79-3  U81-11
     4          DC5
               U79-4  U78-5  U82-13
     5          DC4
               U79-5  U78-16  U81-12
     6         U153-11  U79-6
     7          C14M
               U146-6  R100-1  U117-10  U119-9  U79-7  U85-11
     8         GND
     9          RESET*
               U65-40  U162-10  U98-4  U97-34  U73-34  U75-15  U79-9
               U173-1
     10         DC3
               U79-10  U78-6  U82-12
     11         DC2
               U79-11  U78-15  U81-13
     12         DC1
               U79-12  U78-9  U82-11
     13          BTO
                U88-3  U85-18  U162-5  U79-13  U83-4  U83-1
     14          DCO
                U79-14  U78-12  U81-14
     15          LDPS*
                U117-9  U79-15  U131-6
     16          +5V

U80 5 LS374 20 F2
     1           VBEN
                U80-1  U132-11
     2           DV7
                U86-3  U78-3  U80-2  U84-2  U136-3  U136-2
     3           DB7
                J16-8  U69-13  U80-3
     4           DB5
                J16-6  U69-6  U80-4
     5           DV5
                U82-3  U86-4  U78-4  U81-3  U80-5  U84-5
     6           DV3
                U82-2  U86-7  U78-7  U81-2  U80-6  U84-6
     7           DB3
                J16-4  U66-13  U80-7
     8           DB1
                J16-2  U66-6  U80-8
     9           DV1
                U82-1  U86-8  U78-8  U81-1  U80-9  U84-9
     10          GND
     11          C1M
                U132-2  U135-1  U119-10  U123-11  U180-5  U98-27  U80-11
                U84-11
     12          DVO
                U82-17  U86-13  U78-13  U81-17  U80-12  U84-12
     13          DBO
                J16-1  U66-3  U80-13
     14          DB2
                J16-3  U66-10  U80-14
     15          DV2
                U82-16  U86-14  U78-14  U81-16  U80-15  U84-15
     16          DV4
                U82-15  U86-17  U78-17  U81-15  U80-16  U84-16
     17          DB4
                J16-5  U69-3  U80-17
     18          DB6
                J16-7  U69-10  U80-18
     19          DV6
                U78-18  U86-18  U82-4  U81-4  U80-19  U84-19
     20          +5V

U81 5 2114 18 E5
     1           DV1
                U82-1  U86-8  U78-8  U81-1  U80-9  U84-9
     2          DV3
               U82-2  U86-7  U78-7  U81-2  U80-6  U84-6
     3          DV5
               U82-3  U86-4  U78-4  U81-3  U80-5  U84-5
     4          DV6
               U78-18  U86-18  U82-4  U81-4  U80-19  U84-19
     5          VA
               U121-3  U175-5  U116-11  U82-5  U81-5
     6          VB
               U121-2  U175-6  U118-14  U82-6  U81-6
     7          VC
               U121-1  U175-7  U118-13  U83-15  U83-14  U82-7  U81-7
     8          DHIRES
               U83-10  U126-8  U82-8  U81-8  U87-17
     9         GND
     10         WE2114*
               U82-10  U175-16  U81-10  U144-6
     11         DC6
               U78-19  U79-3  U81-11
     12         DC4
               U79-5  U78-16  U81-12
     13         DC2
               U79-11  U78-15  U81-13
     14         DC0
               U79-14  U78-12  U81-14
     15         DV4
               U82-15  U86-17  U78-17  U81-15  U80-16  U84-16
     16         DV2
               U82-16  U86-14  U78-14  U81-16  U80-15  U84-15
     17         DV0
               U82-17  U86-13  U78-13  U81-17  U80-12  U84-12
     18         +5V

U82 5 2114 18 E4  .
     1          DV1
               U82-1  U86-8  U78-8  U81-1  U80-9  U84-9
     2          DV3
               U82-2  U86-7  U78-7  U81-2  U80-6  U84-6
     3          DV5
               U82-3  U86-4  U78-4  U81-3  U80-5  U84-5
     4          DV6
               U78-18  U86-18  U82-4  U81-4  U80-19  U84-19
     5          VA
               U121-3  U175-5  U116-11  U82-5  U81-5
     6          VB
               U121-2  U175-6  U118-14  U82-6  U81-6
     7          VC
               U121-1  U175-7  U118-13  U83-15  U83-14  U82-7  U81-7
     8          DHIRES
               U83-10  U126-8  U82-8  U81-8  U87-17
     9         NO CONNECTION
     10         WE2114*
```

```
             U82-10  U175-16  U81-10  U144-6
    11        DC1
             U79-12  U78-9  U82-11
    12        DC3
             U79-10  U78-6  U82-12
    13        DC5
             U79-4  U78-5  U82-13
    14        DC7
             U79-2  U78-2  U82-14  U136-4
    15        DV4
             U82-15  U86-17  U78-17  U81-15  U80-16  U84-16
    16        DV2
             U82-16  U86-14  U78-14  U81-16  U80-15  U84-15
    17        DV0
             U82-17  U86-13  U78-13  U81-17  U80-12  U84-12
    18       +5V

U83 5 S151 16 J3
    1         BT0
             U88-3  U85-18  U162-5  U79-13  U83-4  U83-1
    2         BT1
             U88-6  U83-2  U85-19  U85-17
    3         BT0*
             U83-3  U162-6
    4         BT0
             U88-3  U85-18  U162-5  U79-13  U83-4  U83-1
    5         BTMUX
             U85-13  U83-5
    6        NO CONNECTION
    7         BL
             U97-16  U83-7  U85-7  U126-16
    8        GND
    9         AIILORES
             U83-9  U87-16
    10        DHIRES
             U83-10  U126-8  U82-8  U81-8  U87-17
    11        INV
             U83-11  U173-5
    12       GND
    13       GND
    14        VC
             U121-1  U175-7  U118-13  U83-15  U83-14  U82-7  U81-7
    15        VC
             U121-1  U175-7  U118-13  U83-15  U83-14  U82-7  U81-7
    16       +5V

U84 5 LS374 20 E2
    1         VAEN
             U84-1  U132-3
    2         DV7
             U86-3  U78-3  U80-2  U84-2  U136-3  U136-2
    3         DA7
```

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               J16-16  U153-5  U84-3  U69-14
    4           DA5
               J16-14  U69-5  U84-4
    5           DV5
               U82-3  U86-4  U78-4  U81-3  U80-5  U84-5
    6           DV3
               U82-2  U86-7  U78-7  U81-2  U80-6  U84-6
    7           DA3
               J16-12  U66-14  U84-7
    8           DA1
               J16-10  U10-5  U84-8  U66-5
    9           DV1
               U82-1  U86-8  U78-8  U81-1  U80-9  U84-9
    10         GND
    11          C1M
               U132-2  U135-1  U119-10  U123-11  U180-5  U98-27  U80-11
               U84-11
    12          DV0
               U82-17  U86-13  U78-13  U81-17  U80-12  U84-12
    13          DA0
               J16-9  U10-4  U84-13  U66-2
    14          DA2
               J16-11  U10-12  U84-14  U66-11
    15          DV2
               U82-16  U86-14  U78-14  U81-16  U80-15  U84-15
    16          DV4
               U82-15  U86-17  U78-17  U81-15  U80-16  U84-16
    17          DA4
               J16-13  U69-2  U84-17
    18          DA6
               J16-15  U69-11  U84-18
    19          DV6
               U78-18  U86-18  U82-4  U81-4  U80-19  U84-19
    20         +5V

U85 5 LS374 20 G2
    1          GND
    2           Q0*
               U152-12  U144-2  U85-2
    3           Q3
               J14-37  U85-3  J15-37  J13-37  J12-37  U117-12  R93-1
               U154-2
    4           CIM*
               U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
               U126-11  U85-4  U144-5  U132-12  U150-4
    5           D1M*
               U85-5  U86-11
    6           DBL
               U85-6  U88-15
    7           BL
               U97-16  U83-7  U85-7  U126-16
    8           H2
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               U121-7  U5-5  U114-12  U85-8
     9          DH2
               U132-9  U85-9
     10        GND
     11         C14M
               U146-6  R100-1  U117-10  U119-9  U79-7  U85-11
     12         BTMUXD
               U85-12  U89-1
     13         BTMUX
               U85-13  U83-5
     14         BT2
               U88-10  U85-14  U85-16
     15         BT3
               U88-13  U85-15
     16         BT2
               U88-10  U85-14  U85-16
     17         BT1
               U88-6  U83-2  U85-19  U85-17
     18         BT0
               U88-3  U85-18  U162-5  U79-13  U83-4  U83-1
     19         BT1
               U88-6  U83-2  U85-19  U85-17
     20        +5V

U86 5 LS374 20 F3
     I          OE374
               U87-15  U86-1
     2          DX7
               U89-4  U86-2  P8-6
     3          DV7
               U86-3  U78-3  U80-2  U84-2  U136-3  U136-2
     4          DV5
               U82-3  U86-4  U78-4  U81-3  U80-5  U84-5
     5          DX5
               U89-12  U86-5  P8-3
     6          DX3
               U88-2  U86-6  P13-4
     7          DV3
               U82-2  U86-7  U78-7  U81-2  U80-6  U84-6
     8          DV1
               U82-1  U86-8  U78-8  U81-1  U80-9  U84-9
     9          DX1
               U88-11  U86-9  P13-5
     10        GND
     11         D1M*
               U85-5  U86-11
     12         DX0
               U88-14  U86-12  P13-2
     13         DV0
               U82-17  U86-13  U78-13  U81-17  U80-12  U84-12
     14         DV2
               U82-16  U86-14  U78-14  U81-16  U80-15  U84-15
     15          DX2
                U88-5  U86-15  P13-3
     16          DX4
                U89-13  U86-16  P8-4
     17          DV4
                U82-15  U86-17  U78-17  U81-15  U80-16  U84-16
     18          DV6
                U78-18  U86-18  U82-4  U81-4  U80-19  U84-19
     19          DX6
                U89-5  U86-19  P8-5
     20         +5V

U87 5 2316 24 341-0032 G5
     1           MIX
                U87-1  U75-5
     2           HIRES
                U87-2  U75-7
     3           AIISW*
                U165-6  U71-12  U97-8  U178-1  U178-13  U177-15  U87-3
                U155-3
     4           PAGE2
                U87-4  U75-6
     5           VBL
                U175-15  U87-5  U97-19  U97-18  U121-19  U154-6
     6           FORCPAGE
                U87-6  P10-2  J20-7
     7          +5V
     8          GND
     9           PG2*
                U87-9  U13-13
     10          SEL374
                U87-10  U132-13  U132-1
     11          COLORKILL*
                U147-13  U87-11  J20-9
     12         GND
     13          AHIRES
                U88-1  U87-13  U141-1
     14          CH80*
                U139-9  U153-12  U87-14
     15          OE374
                U87-15  U86-1
     16          AIILORES
                U83-9  U87-16
     17          DHIRES
                U83-10  U126-8  U82-8  U81-8  U87-17
     18         NO CONNECTION
     19          V4
                U87-19  U1-2  U154-4  U120-12  U1-11
     20         GND
     21         +5V
     22          V2
                U120-14  U154-10  U87-22
     23           TEXT
                 U87-23  U75-4
     24          +5V

U88 5 LS157 16 G3
     1            AHIRES
                 U88-1  U87-13  U141-1
     2            DX3
                 U88-2  U86-6  P13-4
     3            BT0
                 U88-3  U85-18  U162-5  U79-13  U83-4  U83-1
     4           U89-3  U88-4
     5            DX2
                 U88-5  U86-15  P13-3
     6            BT1
                 U88-6  U83-2  U85-19  U85-17
     7           U89-6  U88-7
     8           GND
     9           U89-11  U88-9
     10           BT2
                 U88-10  U85-14  U85-16
     11           DX1
                 U88-11  U86-9  P13-5
     12          U89-14  U88-12
     13           BT3
                 U88-13  U85-15
     14           DX0
                 U88-14  U86-12  P13-2
     15           DBL
                 U85-6  U88-15
     16          +5V

U89 5 LS399 16 H3
     1            BTMUXD
                 U85-12  U89-1
     2            RGB8
                 J20-5  P4-5  P17-2  P3-6  P10-3  U90-11  U90-3
                 U89-2
     3           U89-3  U88-4
     4            DX7
                 U89-4  U86-2  P8-6
     5            DX6
                 U89-5  U86-19  P8-5
     6           U89-6  U88-7
     7            RGB4
                 P4-4  P17-4  P3-5  P10-7  U90-4  U90-10  U89-7
                 J20-4
     8           GND
     9            CKDSP
                 U141-11  U89-9
     10           RGB2
                 J20-2  P17-6  P4-3  P3-4  P10-6  U90-5  U90-13
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                U89-10
     11         U89-11  U88-9
     12          DX5
                U89-12  U86-5  P8-3
     13          DX4
                U89-13  U86-16  P8-4
     14         U89-14  U88-12
     15          RGB1
                U89-15  P17-8  P4-2  P3-3  J20-6  P10-4  U90-6
                U90-12
     16         +5V

U90 5 LS153 16 L8
     1          GND
     2           C3.5M*
                U135-13  U119-6  U147-1  U90-2
     3           RGB8
                J20-5  P4-5  P17-2  P3-6  P10-3  U90-11  U90-3
                U89-2
     4           RGB4
                P4-4  P17-4  P3-5  P10-7  U90-4  U90-10  U89-7
                J20-4
     5           RGB2
                J20-2  P17-6  P4-3  P3-4  P10-6  U90-5  U90-13
                U89-10
     6           RGB1
                U89-15  P17-8  P4-2  P3-3  J20-6  P10-4  U90-6
                U90-12
     7           NTSCA
                P3-7  U90-7
     8          GND
     9           NTSCB*
                U163-9  U90-9
     10          RGB4
                P4-4  P17-4  P3-5  P10-7  U90-4  U90-10  U89-7
                J20-4
     11          RGB8
                J20-5  P4-5  P17-2  P3-6  P10-3  U90-11  U90-3
                U89-2
     12          RGB1
                U89-15  P17-8  P4-2  P3-3  J20-6  P10-4  U90-6
                U90-12
     13          RGB2
                J20-2  P17-6  P4-3  P3-4  P10-6  U90-5  U90-13
                U89-10
     14          C7M
                J15-36  J14-36  J13-36  J12-36  U141-9  U119-2  U146-12
                U90-14
     15         GND
     16         +5V

U91 6 LS323 20 K10
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```
     1          U92-7  U91-1
     2           DEVSEL6*
                U94-14  U76-9  U91-2
     3           IR*/W
                U91-3  U68-11  U158-2  U163-10
     4           D1
                J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
                U91-4  U66-7  P15-3
     5           D3
                J15-46  J14-46  J13-46  J12-46  U68-16  J16-20  U109-12
                U91-5  U66-12  P15-5
     6           D5
                J15-44  J14-44  J13-44  J12-44  U68-14  J16-22  U111-7
                U91-6  U69-7  P15-7
     7           D7
                J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
                U101-5  U91-7  U69-12  P15-9
     8          U92-2  U91-8
     9          U92-9  U91-9  R66-1
     10         GND
     11          DWRPROTT
                U167-17  U91-11
     12          Q3*
                U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                U131-5  R102-2  R103-1  U146-1
     13          D6
                J15-43  J14-43  J13-43  J12-43  U68-13  J16-23  U111-9
                U91-13  U69-9  P15-8
     14          D4
                J15-45  J14-45  J13-45  J12-45  U68-15  J16-21  U111-4
                U91-14  U69-4  P15-6
     15          D2
                J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
                U91-15  U66-9  P15-4
     16          D0
                J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
                U91-16  U66-4  P15-2
     17         NO CONNECTION
     18         U92-8  U91-18
     19         U92-6  U91-19
     20         +5V

U92 6 S471 20 341-0028 K11
     1          U93-15  U92-1
     2          U92-2  U91-8
     3          U92-3  U94-11
     4          U163-13  U94-12  U92-4
     5          U161-11  U92-5  R67-2
     6          U92-6  U91-19
     7          U92-7  U91-1
     8          U92-8  U91-18
     9          U92-9  U91-9  R66-1
     10          GND
     11          U93-6  U92-11
     12          U93-14  U92-12
     13          U93-4  U92-13
     14          U93-3  U92-14
     15           MOTON*
                 U179-1  U92-15  U178-15  R65-2  U164-12  U92-16
     16           MOTON*
                 U179-1  U92-15  U178-15  R65-2  U164-12  U92-16
     17          U93-7  U92-17
     18          U93-5  U92-18
     19           DWRDATA
                 U166-18  U92-19  U93-2
     20          +5V

U93 6 LS174 16 K12
     1            S5B
                 R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                 U114-7  U116-5
     2            DWRDATA
                 U166-18  U92-19  U93-2
     3           U93-3  U92-14
     4           U93-4  U92-13
     5           U93-5  U92-18
     6           U93-6  U92-11
     7           U93-7  U92-17
     8           GND
     9            Q3*
                 U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                 U131-5  R102-2  R103-1  U146-1
     10          U161-13  U93-10
     11          U93-12  U161-12  U93-11
     12          U93-12  U161-12  U93-11
     13           DRDATA
                 U166-17  U93-13
     14          U93-14  U92-12
     15          U93-15  U92-1
     16          +5V

U94 6 9334 16 L13
     1            A1
                 J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
                 U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     2            A2
                 J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
                 U177-2  U94-2  U75-2  U73-36  U63-14
     3            A3
                 J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
                 U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     4            VA1
                 U166-12  U175-4  U94-4
     5            VB1
```

```
             U167-12  U175-3  U94-5
    6         VC1
             U166-13  U175-2  U94-6
    7         PDPH3
             U167-13  U94-7
    8        GND
    9         MOTEN*
             U164-11  U94-9
    10        DEXT*
             U167-18  U94-10  U178-2  U163-1
    11       U92-3  U94-11
    12       U163-13  U94-12  U92-4
    13        A0
             J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
             U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
    14        DEVSEL6*
             U94-14  U76-9  U91-2
    15        IORESET*
             J12-31  J13-31  J14-31  J15-31  P14-6  U164-2  U164-4
             U96-4  U94-15
    16       +5V

U96 6-8 556 14 L10
    1        NO CONNECTION
    2         DT1M
             R31-1  U164-10  C7-2  U96-2  U96-6
    3        NO CONNECTION
    4         IORESET*
             J12-31  J13-31  J14-31  J15-31  P14-6  U164-2  U164-4
             U96-4  U94-15
    5         MOTON
             U164-13  U96-5
    6         DT1M
             R31-1  U164-10  C7-2  U96-2  U96-6
    7        GND
    8        U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
             X3-1  C75-1
    9        U96-9  U139-1
    10       U96-10  U162-2  U139-2
    11       NO CONNECTION
    12       U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
             X3-1  C75-1
    13       U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
             X3-1  C75-1
    14       +5V

U97 7 6522 40 B5
    1        GND
    2         BKSW1
             U97-2  U10-3
    3         BKSW2
             U97-3  U10-6
```

4	BKSW3	U97-4 U10-11
5	NO CONNECTION	
6	IRQ4*	U97-6 J15-30 P2-3 U148-5
7	IRQ3*	U97-7 J14-30 P2-4 U148-4
8	AIISW*	U165-6 U71-12 U97-8 U178-1 U178-13 U177-15 U87-3 U155-3
9	IRQ*	U97-21 U65-4 U98-26 U97-9 U73-21
10	SND0	P9-7 U97-10
11	SND1	P9-6 U97-11
12	SND2	P9-5 U97-12
13	SND3	P9-4 U97-13
14	SND4	P9-3 U97-14
15	SND5	P9-2 U97-15
16	BL	U97-16 U83-7 U85-7 U126-16
17	IONMI*	J15-29 U97-17 J14-29 J13-29 U139-13 J12-29
18	VBL	U175-15 U87-5 U97-19 U97-18 U121-19 U154-6
19	VBL	U175-15 U87-5 U97-19 U97-18 U121-19 U154-6
20	+5V	
21	IRQ*	U97-21 U65-4 U98-26 U97-9 U73-21
22	IR/W*	U98-28 U97-22 U112-14 U73-22 U163-11 U65-34 U160-12
23	FFEX*	U97-23 U148-10 U112-6
24	CS6522	R68-2 U73-24 C59-1 U97-24
25	PRE1M	J12-40 J13-40 J14-40 J15-40 U119-12 U73-25 U123-5 U97-25 U139-10 R94-1
26	ID7	U98-25 U65-26 U97-26 U72-22 U73-26 U64-17 U68-8
27	ID6	U98-24 U65-27 U97-27 U72-21 U73-27 U64-16 U68-7
28	ID5	U98-23 U65-28 U97-28 U72-20 U73-28 U64-15 U68-6
29	ID4	U98-22 U65-29 U97-29 U72-19 U73-29 U64-14 U68-5

```
     30          ID3
                U98-21  U65-30  U97-30  U72-18  U73-30  U64-13  U68-4
     31          ID2
                U98-20  U65-31  U97-31  U72-17  U73-31  U64-11  U68-3
     32          ID1
                U98-19  U65-32  U97-32  U72-16  U73-32  U64-10  U68-2
     33          ID0
                U98-18  U65-33  U97-33  U72-15  U73-33  U64-9  U68-1
     34          RESET*
                U65-40  U162-10  U98-4  U97-34  U73-34  U75-15  U79-9
                U173-1
     35          A3
                J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
                U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     36          A2
                J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
                U177-2  U94-2  U75-2  U73-36  U63-14
     37          A1
                J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
                U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     38          A0
                J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
                U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
     39          KBDINT*
                U106-6  U97-39
     40          CKIRQ*
                U72-13  R79-2  U97-40

U98 7 6551 28 B2
     1          GND
     2          +5V
     3           SEL6551*
                U98-3  U76-7  U148-12
     4           RESET*
                U65-40  U162-10  U98-4  U97-34  U73-34  U75-15  U79-9
                U173-1
     5          NO CONNECTION
     6           ACIACLK
                U98-6  U140-5
     7          NO CONNECTION
     8           RTS*
                U99-12  U98-8
     9           CTS*
                U100-6  U98-9
     10          TXD*
                U99-4  U98-10
     11          DTR*
                U99-9  U98-11
     12          RXD*
                U100-3  U98-12
     13          A0
                J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
                U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
    14           A1
                J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
                U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
    15          +5V
    16           DCD*
                U100-11  U98-16
    17           DSR*
                U100-8  U98-17
    18           ID0
                U98-18  U65-33  U97-33  U72-15  U73-33  U64-9  U68-1
    19           ID1
                U98-19  U65-32  U97-32  U72-16  U73-32  U64-10  U68-2
    20           ID2
                U98-20  U65-31  U97-31  U72-17  U73-31  U64-11  U68-3
    21           ID3
                U98-21  U65-30  U97-30  U72-18  U73-30  U64-13  U68-4
    22           ID4
                U98-22  U65-29  U97-29  U72-19  U73-29  U64-14  U68-5
    23           ID5
                U98-23  U65-28  U97-28  U72-20  U73-28  U64-15  U68-6
    24           ID6
                U98-24  U65-27  U97-27  U72-21  U73-27  U64-16  U68-7
    25           ID7
                U98-25  U65-26  U97-26  U72-22  U73-26  U64-17  U68-8
    26           IRQ*
                U97-21  U65-4  U98-26  U97-9  U73-21
    27           C1M
                U132-2  U135-1  U119-10  U123-11  U180-5  U98-27  U80-11
                U84-11
    28           IR/W*
                U98-28  U97-22  U112-14  U73-22  U163-11  U65-34  U160-12

U99 7 1488 14 J2
    1           -12V
    2           NO CONNECTION
    3           NO CONNECTION
    4            TXD*
                U99-4  U98-10
    5           +5V
    6            PTXD
                U172-12  U99-6
    7           GND
    8            PDTR
                U172-17  U99-8
    9            DTR*
                U99-9  U98-11
    10          +5V
    11           PRTS
                U172-14  U99-11
    12           RTS*
                U99-12  U98-8
```

```
     13         +5V
     14         +12V

U100 7 1489 14 K2
     1           PRXD
                U172-13  U100-1
     2          NO CONNECTION
     3           RXD*
                U100-3  U98-12
     4           PCTS
                R87-2  U172-15  U100-4
     5          NO CONNECTION
     6           CTS*
                U100-6  U98-9
     7          GND
     8           DSR*
                U100-8  U98-17
     9          NO CONNECTION
     10          PDSR
                R88-2  U172-16  U100-10
     11          DCD*
                U100-11  U98-16
     12         NO CONNECTION
     13          PDCD
                R89-2  U172-18  U100-13
     14         +5V

U101 7 LS251 16 L7
     1           SC0
                U160-3  U73-18  U160-5  U101-1
     2           SW2UF
                U101-2  U169-14
     3           SW1/MGNSWUF
                R85-2  U169-19  U73-39  U101-3
     4           SW0UF
                U101-4  U169-13
     5           D7
                J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
                U101-5  U91-7  U69-12  P15-9
     6          NO CONNECTION
     7           C06X*
                U101-7  U77-9
     8          GND
     9           A2
                J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
                U177-2  U94-2  U75-2  U73-36  U63-14
     10          A1
                J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
                U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     11          A0
                J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
                U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
     12          MUX1
                U101-12  U175-14  U5-13
     13          PDLOT*
                U101-13  U105-7  R57-2
     14          IRQ1*
                U101-14  J12-30  P2-7  U148-1
     15          IRQ2*
                U101-15  J13-30  P2-6  U148-2
     16         +5V

U103 7 380N-8N 8 M11
     1          NO CONNECTION
     2          C78-1  U103-2  R34-2  R36-1
     3          GND
     4          GND
     5          GND
     6          R69-2  U103-6
     7          +12V
     8          C13-1  U103-8

U105 7 9708 16 M9
     1           AXCO
                U161-5  U75-12  U105-1
     2           PDL2
                U160-4  U105-2  U75-10
     3           PDLEN
                U105-3  U75-11
     4           TCAP
                C15-1  U105-4
     5          GND
     6          U105-6  R39-2  C9-1
     7           PDLOT*
                U101-13  U105-7  R57-2
     8          U105-8  R37-2  R38-1  C76-1
     9          NO CONNECTION
     10         R9-1  T1-1  X1-1  U105-10
     11          Y1/XCOUF
                U161-6  U169-17  U105-11
     12          PX1/SER
                U105-12  U161-8  U160-9  U169-18
     13          YOUF
                U105-13  U169-15
     14         +5V
     15          XOUF
                U105-15  U169-12
     16          PDLO
                U105-16  U75-9

U106 8 LS74 14 H11
     1           CLRSTRB*
                U106-1  U77-14
     2           S5B
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                R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                U114-7  U116-5
     3          U139-3  U106-3
     4           S5B
                R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                U114-7  U116-5
     5          U106-5  U111-14
     6           KBDINT*
                U106-6  U97-39
     7          GND
     8          NO CONNECTION
     9           KAPPLEII*
                U106-9  X3-2  U111-6
     10          S5B
                R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                U114-7  U116-5
     11          ANYKEY
                U107-4  R40-1  X2-2  U106-11  U109-3
     12          APPLEII*
                J7-5  P11-5  U106-12  U164-5
     13          S5B
                R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                U114-7  U116-5
     14         +5V

U107 8 AY3600 40 H14
     1          C16-1  U107-1
     2          U107-2  C16-2  R47-2
     3          U107-3  R47-1
     4           ANYKEY
                U107-4  R40-1  X2-2  U106-11  U109-3
     5          NO CONNECTION
     6           KSHIFT*
                U107-6  U109-6
     7           ASCII7
                U107-7  U111-13
     8           ASCII6
                U107-8  U111-11
     9           ASCII5
                U107-9  U111-5
     10          ASCII4
                U107-10  U111-2
     11          ASCII3
                U107-11  U109-14
     12          ASCII2
                U107-12  U109-11
     13          ASCII1
                U107-13  U109-5
     14          ASCII0
                U107-14  U109-2
     15         GNDF
     16          DTRDY*
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                U107-16  U162-1
     17          KY0
                J7-1  U107-17
     18          KY1
                J7-2  U107-18
     19          KY2
                J7-4  U107-19
     20          KY3
                J7-6  U107-20
     21          KY4
                J7-8  U107-21
     22          KY5
                J7-10  U107-22
     23          KY6
                J7-23  U107-23
     24          KY7
                J7-25  U107-24
     25          KY8
                J7-12  U107-25
     26          KY9
                J7-22  U107-26
     27         -12FV
     28          CONTROL*
                J7-11  U179-13  U107-28  U109-10  P11-2
     29          SHIFT*
                J7-24  P11-6  U107-29
     30         +5FV
     31         U107-31  C22-1
     32         NO CONNECTION
     33          KX7UF
                U171-14  U107-33
     34          KX6UF
                U171-19  U107-34
     35          KX5UF
                U171-16  U107-35
     36          KX4UF
                U171-18  U107-36
     37          KX3UF
                U171-17  U107-37
     38          KX2UF
                U171-13  U107-38
     39          KX1UF
                U171-15  U107-39
     40          KX0UF
                U171-12  U107-40

U109 8 LS257 16 J12
     1           A3
                J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
                U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     2           ASCII0
                U107-14  U109-2
     3          ANYKEY
               U107-4  R40-1  X2-2  U106-11  U109-3
     4          D0
               J15-49  J14-49  J13-49  J12-49  U68-19  J16-17  U109-4
               U91-16  U66-4  P15-2
     5          ASCII1
               U107-13  U109-5
     6          KSHIFT*
               U107-6  U109-6
     7          D1
               J15-48  J14-48  J13-48  J12-48  U68-18  J16-18  U109-7
               U91-4  U66-7  P15-3
     8         GND
     9          D2
               J15-47  J14-47  J13-47  J12-47  U68-17  J16-19  U109-9
               U91-15  U66-9  P15-4
     10         CONTROL*
               J7-11  U179-13  U107-28  U109-10  P11-2
     11         ASCII2
               U107-12  U109-11
     12         D3
               J15-46  J14-46  J13-46  J12-46  U68-16  J16-20  U109-12
               U91-5  U66-12  P15-5
     13         CAPLCK*
               J7-9  P11-3  U109-13
     14         ASCII3
               U107-11  U109-14
     15         KBD*
               U109-15  U111-15  U77-15
     16         +5V

U111 8 LS257 16 H12
     1          A3
               J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
               U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     2          ASCII4
               U107-10  U111-2
     3          APPLE1*
               J7-7  P11-4  U111-3
     4          D4
               J15-45  J14-45  J13-45  J12-45  U68-15  J16-21  U111-4
               U91-14  U69-4  P15-6
     5          ASCII5
               U107-9  U111-5
     6          KAPPLEII*
               U106-9  X3-2  U111-6
     7          D5
               J15-44  J14-44  J13-44  J12-44  U68-14  J16-22  U111-7
               U91-6  U69-7  P15-7
     8          GND
     9          D6
               J15-43  J14-43  J13-43  J12-43  U68-13  J16-23  U111-9
               U91-13  U69-9  P15-8
    10         Q9-3  R43-1  U111-10
    11          ASCII6
               U107-8  U111-11
    12          D7
               J15-42  J14-42  J13-42  J12-42  U68-12  J16-24  U111-12
               U101-5  U91-7  U69-12  P15-9
    13          ASCII7
               U107-7  U111-13
    14         U106-5  U111-14
    15          KBD*
               U109-15  U111-15  U77-15
    16         +5V

U112 4 LS139 16 C8
    1          U112-1  U71-9
    2           A4
               J15-6  J14-6  J13-6  J12-6  U9-6  U77-1  U76-1
               U112-2  U63-9
    3           A5
               J15-7  J14-7  J13-7  J12-7  U9-10  U76-2  U77-2
               U112-3  U63-7
    4           FFCX*
               U165-7  U112-4
    5           FFDX*
               U112-5  U73-23  U148-9
    6           FFEX*
               U97-23  U148-10  U112-6
    7          NO CONNECTION
    8          GND
    9          NO CONNECTION
    10         NO CONNECTION
    11         NO CONNECTION
    12         U72-3  U112-12
    13          C07X*
               U180-6  U77-7  U112-13  U158-1  U72-1  U150-5  U148-13
    14          IR/W*
               U98-28  U97-22  U112-14  U73-22  U163-11  U65-34  U160-12
    15          IOSTOPD*
               U123-9  U112-15  U180-3
    16         +5V

U113 8 556 14 A5
    1          NO CONNECTION
    2           UPRST*
               C20-1  U113-6  U113-2  R44-2  X4-2  X6-1
    3          NO CONNECTION
    4          +5V
    5           TRESET
               U113-5  R92-1
    6           UPRST*
               C20-1  U113-6  U113-2  R44-2  X4-2  X6-1
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     7          GND
     8          U113-8  R46-2  U113-12  C21-1
     9           FLASH
                U113-9  U136-5
     10         +5V
     11         NO CONNECTION
     12         U113-8  R46-2  U113-12  C21-1
     13         U113-13  R45-2  R46-1
     14         +5V

U114 9 LS161 16 F10
     1           UUTRST*
                U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
                U120-1  U118-1  U117-1
     2           CIM*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     3          GND
     4          GND
     5          GND
     6          GND
     7           S5B
                R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                U114-7  U116-5
     8          GND
     9           HPE*
                U135-3  U152-2  U114-9  U116-9  U116-12
     10          S5B
                R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                U114-7  U116-5
     11          H3
                U114-11  U1-5  U121-6
     12          H2
                U121-7  U5-5  U114-12  U85-8
     13          H1
                U114-13  U2-11  U155-9
     14          H0
                U114-14  U2-5
     15         U116-10  U114-15  U116-7
     16         +5V

U116 9 LS161 16 F11
     1           UUTRST*
                U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
                U120-1  U118-1  U117-1
     2           CIM*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     3          GND
     4          GND
     5           S5B
                R107-2  U106-2  U106-4  U106-10  U106-13  U93-1  U114-10
                U114-7  U116-5
     6           COMP
                U116-6  U121-17  U118-3
     7          U116-10  U114-15  U116-7
     8          GND
     9           HPE*
                U135-3  U152-2  U114-9  U116-9  U116-12
     10         U116-10  U114-15  U116-7
     11          VA
                U121-3  U175-5  U116-11  U82-5  U81-5
     12          HPE*
                U135-3  U152-2  U114-9  U116-9  U116-12
     13          H5
                U121-4  U1-14  U116-13
     14          H4
                U121-5  U1-3  U116-14
     15         U118-5  U116-15  U118-10  U118-7
     16         +5V

U117 9 S195 16 D10
     1           UUTRST*
                U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
                U120-1  U118-1  U117-1
     2           Q3*
                U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                U131-5  R102-2  R103-1  U146-1
     3           Q3*
                U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                U131-5  R102-2  R103-1  U146-1
     4           S5D
                R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
                U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     5           S5D
                R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
                U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     6           S5D
                R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
                U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     7           S5D
                R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
                U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     8          GND
     9           LDPS*
                U117-9  U79-15  U131-6
     10          C14M
                U146-6  R100-1  U117-10  U119-9  U79-7  U85-11
     11          Q3*
                U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                U131-5  R102-2  R103-1  U146-1
     12          Q3
                J14-37  U85-3  J15-37  J13-37  J12-37  U117-12  R93-1
                U154-2
     13         NO CONNECTION
     14          Q1
                U6-8  U131-4  U3-8  U124-12  U117-14
     15          Q0
                U119-13  U150-10  U117-15  U131-2  U78-11
     16         +5V

U118 9 LS161 16 G11
     1           UUTRST*
                U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
                U120-1  U118-1  U117-1
     2           CIM*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     3           COMP
                U116-6  U121-17  U118-3
     4          GND
     5          U118-5  U116-15  U118-10  U118-7
     6           S5060
                U120-3  U121-15  U118-6
     7          U118-5  U116-15  U118-10  U118-7
     8          GND
     9           UUTSUNK*
                J19-1  U118-9  U162-8  U120-9
     10         U118-5  U116-15  U118-10  U118-7
     11          V1
                U121-22  U2-13  U118-11  U13-5  U13-3
     12          V0
                U121-23  U13-11  U118-12
     13          VC
                U121-1  U175-7  U118-13  U83-15  U83-14  U82-7  U81-7
     14          VB
                U121-2  U175-6  U118-14  U82-6  U81-6
     15         U120-5  U118-15  U120-4  U120-10  U120-7
     16         +5V

U119 9 S175 16 B12
     1           UUTRST*
                U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
                U120-1  U118-1  U117-1
     2           C7M
                J15-36  J14-36  J13-36  J12-36  U141-9  U119-2  U146-12
                U90-14
     3           C7M*
                U119-3  U153-13  U119-4
     4           C7M*
                U119-3  U153-13  U119-4
     5          U119-5  U146-11
     6           C3.5M*
                U135-13  U119-6  U147-1  U90-2
     7           C3.5M
                U132-10  U141-10  U146-13  U119-7  J20-3
     8          GND
     9           C14M
                U146-6  R100-1  U117-10  U119-9  U79-7  U85-11
     10          C1M
                U132-2  U135-1  U119-10  U123-11  U180-5  U98-27  U80-11
                U84-11
     11          C1M*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     12          PRE1M
                J12-40  J13-40  J14-40  J15-40  U119-12  U73-25  U123-5
                U97-25  U139-10  R94-1
     13          Q0
                U119-13  U150-10  U117-15  U131-2  U78-11
     14          RAS
                U152-13  U150-9  U119-14  U12-2  U12-5  U12-10  U12-13
     15         NO CONNECTION
     16         +5V

U120 9 LS161 16 G12
     1           UUTRST*
                U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
                U120-1  U118-1  U117-1
     2           C1M*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     3           S5060
                U120-3  U121-15  U118-6
     4          U120-5  U118-15  U120-4  U120-10  U120-7
     5          U120-5  U118-15  U120-4  U120-10  U120-7
     6          GND
     7          U120-5  U118-15  U120-4  U120-10  U120-7
     8          GND
     9           UUTSUNK*
                J19-1  U118-9  U162-8  U120-9
     10         U120-5  U118-15  U120-4  U120-10  U120-7
     11          V5
                U120-11  U154-9
     12          V4
                U87-19  U1-2  U154-4  U120-12  U1-11
     13          V3
                U120-13  U1-15  U154-5  U1-6
     14          V2
                U120-14  U154-10  U87-22
     15         U162-9  U120-15
     16         +5V

U121 9 2316 24 341-0030 G9
     1           VC
                U121-1  U175-7  U118-13  U83-15  U83-14  U82-7  U81-7
     2           VB
                U121-2  U175-6  U118-14  U82-6  U81-6
     3           VA
                U121-3  U175-5  U116-11  U82-5  U81-5
     4           H5
                U121-4  U1-14  U116-13
     5           H4
                U121-5  U1-3  U116-14
     6           H3
                U114-11  U1-5  U121-6
     7           H2
                U121-7  U5-5  U114-12  U85-8
     8           V2*V5
                U121-8  U154-8  U5-3
     9           RSYNCH
                U121-9  U126-4
     10          RCOLRGT
                U121-10  U126-7
     11          RTCWRT
                U126-13  U121-11
     12         GND
     13          RBL
                U121-13  U154-12
     14          RRFSH
                U121-14  U126-3
     15          S5060
                U120-3  U121-15  U118-6
     16          RFIELD
                U121-16  U126-18
     17          COMP
                U116-6  U121-17  U118-3
     18          FIELDIN
                J19-3  U121-18  R63-1
     19          VBL
                U175-15  U87-5  U97-19  U97-18  U121-19  U154-6
     20         GND
     21         +5V
     22          V1
                U121-22  U2-13  U118-11  U13-5  U13-3
     23          V0
                U121-23  U13-11  U118-12
     24         +5V

U123 9 S74 14 D11
     1           UUTRST*
                U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
                U120-1  U118-1  U117-1
     2           CIM*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     3           AX
                U124-9  U123-3
     4           S5D
                R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
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              U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     5         PRE1M
              J12-40  J13-40  J14-40  J15-40  U119-12  U73-25  U123-5
              U97-25  U139-10  R94-1
     6         PRE1M*
              J12-38  J13-38  J14-38  J15-38  U123-6  R95-1
     7        GND
     8        NO CONNECTION
     9         IOSTOPD*
              U123-9  U112-15  U180-3
     10        S5D
              R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
              U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     11        C1M
              U132-2  U135-1  U119-10  U123-11  U180-5  U98-27  U80-11
              U84-11
     12        FSPACE*
              U180-1  U176-1  U165-12  U123-12  U148-8
     13        S5D
              R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
              U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     14       +5V

U124  9 S74  14 A11
     1         S5D
              R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
              U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     2        U124-2  U152-8
     3        U124-3  U146-3
     4         S5D
              R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
              U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     5         PHO
              J15-19  U136-11  J14-19  J13-19  J12-19  U124-5  U65-37
              R96-1
     6        NO CONNECTION
     7        GND
     8         AX*
              U124-8  U2-2  U13-2  U9-2  U5-2  J17-23
     9         AX
              U124-9  U123-3
     10        S5D
              R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
              U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
     11        C14M*
              U141-13  U146-8  U124-11  J21-2
     12        Q1
              U6-8  U131-4  U3-8  U124-12  U117-14
     13        UUTRST*
              U124-13  U119-1  U123-1  R53-2  U114-1  J21-3  U116-1
              U120-1  U118-1  U117-1
     14       +5V
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U126 9 LS374 20 G10
     1          GND
     2           RFSH
                U158-13  U11-16  U126-2
     3           RRFSH
                U121-14  U126-3
     4           RSYNCH
                U121-9  U126-4
     5           SYNCH
                J20-1  P17-10  U126-5  P3-2  P4-6
     6           COLRGATE
                J20-3  U147-2  U126-6
     7           RCOLRGT
                U121-10  U126-7
     8           DHIRES
                U83-10  U126-8  U82-8  U81-8  U87-17
     9           RDHIRES
                U175-1  U11-17  U3-2  U6-3  U126-9
     10         GND
     11          CIM*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     12          TCWRT
                U126-12  U144-4
     13          RTCWRT
                U126-13  U121-11
     14         U126-14  U152-1  U154-11
     15         U158-12  U126-15
     16          BL
                U97-16  U83-7  U85-7  U126-16
     17         U126-17  U152-3
     18           RFIELD
                U121-16  U126-18
     19          FIELDOUT
                U126-19  J19-2
     20         +5V

U128 2 S86 14 E10
     1           A10
                J15-12  J14-12  J13-12  J12-12  U128-1  U74-3  U71-4
                U67-9
     2           PCAS3*
                U128-2  U128-13  P1-6  U3-11  U4-8
     3          U5-12  U128-3
     4           A13
                J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
                U71-1  U70-7  U6-5  U3-6  U174-7
     5           PRAS0.3
                U128-5  U11-14  U12-1  U3-15  U6-4
     6          U128-9  U128-6
     7          GND
     8           U13-12  U128-8
     9           U128-9  U128-6
     10           PCAS1*
                 P1-3  U4-4  U6-12  U128-10
     11          U9-4  U128-11
     12           A11
                 J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
                 U150-13  U74-5  U67-12  U3-5  U174-5
     13           PCAS3*
                 U128-2  U128-13  P1-6  U3-11  U4-8
     14          +5V

U131 3-9 LS51 14 B11
     1           U152-6  U144-10  U131-1
     2            Q0
                 U119-13  U150-10  U117-15  U131-2  U78-11
     3           U131-3  U135-5
     4            Q1
                 U6-8  U131-4  U3-8  U124-12  U117-14
     5            Q3*
                 U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                 U131-5  R102-2  R103-1  U146-1
     6            LDPS*
                 U117-9  U79-15  U131-6
     7           GND
     8            ZPAGE*
                 U11-1  U174-15  U67-1  U131-8  U70-1
     9            DMA1
                 U131-11  U163-6  U131-10  U131-9  U160-13
     10           DMA1
                 U131-11  U163-6  U131-10  U131-9  U160-13
     11           DMA1
                 U131-11  U163-6  U131-10  U131-9  U160-13
     12          U135-6  U131-12
     13          U144-9  U131-13  U155-4
     14          +5V

U132 3-5-7 LS86 14 D4
     1            SEL374
                 U87-10  U132-13  U132-1
     2            C1M
                 U132-2  U135-1  U119-10  U123-11  U180-5  U98-27  U80-11
                 U84-11
     3            VAEN
                 U84-1  U132-3
     4            Z0
                 U72-5  U132-4  U73-10
     5            PPA8
                 U158-4  U152-4  U158-5  U65-17  U64-23  U132-5
     6           U67-2  U132-6
     7           GND
     8           U140-3  U132-8
     9          DH2
               U132-9  U85-9
     10         C3.5M
               U132-10  U141-10  U146-13  U119-7  J20-3
     11         VBEN
               U80-1  U132-11
     12         CIM*
               U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
               U126-11  U85-4  U144-5  U132-12  U150-4
     13         SEL374
               U87-10  U132-13  U132-1
     14         +5V

U135 3-9 LS260 14 C9
     1          C1M
               U132-2  U135-1  U119-10  U123-11  U180-5  U98-27  U80-11
               U84-11
     2          HPEDIS
               U135-2  J21-1  R54-1
     3          HPE*
               U135-3  U152-2  U114-9  U116-9  U116-12
     4          PA11
               U64-18  U144-12  U65-20  U67-13  U135-4
     5         U131-3  U135-5
     6         U135-6  U131-12
     7         GND
     8          PA13
               U65-23  U135-8  U70-6
     9          PA12
               U65-22  U135-9  U70-3
     10         PA15
               U135-10  U11-4  U70-13  U65-25
     11         PA14
               U65-24  U135-11  U70-10
     12         Q3*
               U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
               U131-5  R102-2  R103-1  U146-1
     13         C3.5M*
               U135-13  U119-6  U147-1  U90-2
     14         +5V

U136 2-5 LS51 14 H4
     1          SYNC
               U65-7  U136-1  J15-35  U174-3  J14-35  J13-35  J12-35
     2          DV7
               U86-3  U78-3  U80-2  U84-2  U136-3  U136-2
     3          DV7
               U86-3  U78-3  U80-2  U84-2  U136-3  U136-2
     4          DC7
               U79-2  U78-2  U82-14  U136-4
     5          FLASH
               U113-9  U136-5
     6           U173-2  U136-6
     7           GND
     8            CLKBK
                 U136-8  U10-9
     9            R/W*
                 J15-18  J14-18  J13-18  J12-18  U3-3  U136-9  U180-17
                 U176-6  U165-11  U160-11
     10           IND*
                 U136-10  U147-5  U174-12
     11           PHO
                 J15-19  U136-11  J14-19  J13-19  J12-19  U124-5  U65-37
                 R96-1
     12           Q3*
                 U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                 U131-5  R102-2  R103-1  U146-1
     13          NO CONNECTION
     14          +5V

U139 5-8 LS132 14 H10
     1           U96-9  U139-1
     2           U96-10  U162-2  U139-2
     3           U139-3  U106-3
     4           U139-4  U139-11
     5            RESETLK*
                 U179-14  U73-6  P19-5  U139-5
     6            NMI*
                 U139-6  U65-6  U155-2
     7           GND
     8           U139-8  U154-1
     9            CH80*
                 U139-9  U153-12  U87-14
     10           PRE1M
                 J12-40  J13-40  J14-40  J15-40  U119-12  U73-25  U123-5
                 U97-25  U139-10  R94-1
     11          U139-4  U139-11
     12           KRESET*
                 U139-12  R80-1  C71-1  U179-15  J7-15
     13           IONMI*
                 J15-29  U97-17  J14-29  J13-29  U139-13  J12-29
     14          +5V

U140 7-9 S74 14 D5
     1            S5C
                 R108-2  U140-1  U140-4  U140-10  U140-13
     2           U140-6  U140-2
     3           U140-3  U132-8
     4            S5C
                 R108-2  U140-1  U140-4  U140-10  U140-13
     5            ACIACLK
                 U98-6  U140-5
     6           U140-6  U140-2
     7           GND
     8          NO CONNECTION
     9          U152-9  U140-9
     10          S5C
                R108-2  U140-1  U140-4  U140-10  U140-13
     11         U152-10  U152-11  U140-11
     12          PHASEN
                U140-12  U180-13
     13          S5C
                R108-2  U140-1  U140-4  U140-10  U140-13
     14         +5V

U141 4-5 LS00 14 H2
     1           AHIRES
                U88-1  U87-13  U141-1
     2          U141-2  U141-8
     3          U141-12  U141-3
     4          U141-4  U150-6
     5           PH2M
                P19-10  U141-5  U65-39  U176-17
     6           GPH1
                U162-3  U76-4  U141-6  U74-4
     7          GND
     8          U141-2  U141-8
     9           C7M
                J15-36  J14-36  J13-36  J12-36  U141-9  U119-2  U146-12
                U90-14
     10          C3.5M
                U132-10  U141-10  U146-13  U119-7  J20-3
     11          CKDSP
                U141-11  U89-9
     12         U141-12  U141-3
     13          C14M*
                U141-13  U146-8  U124-11  J21-2
     14         +5V

U144 3-5 LS20 14 B10
     1           ENCWRT
                U177-10  U144-1
     2           Q0*
                U152-12  U144-2  U85-2
     3          NO CONNECTION
     4           TCWRT
                U126-12  U144-4
     5           CIM*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     6           WE2114*
                U82-10  U175-16  U81-10  U144-6
     7          GND
     8           DMAOK
                U144-8  J12-27  J15-27  J14-27  J13-27
     9          U144-9  U131-13  U155-4
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    10          U152-6  U144-10  U131-1
    11          NO CONNECTION
    12           PA11
                U64-18  U144-12  U65-20  U67-13  U135-4
    13           TROMSEL
                U162-12  U144-13
    14          +5V

U146 9 S86 14 B13
    1            Q3*
                U93-9  U136-12  U91-12  U117-11  U117-2  U117-3  U135-12
                U131-5  R102-2  R103-1  U146-1
    2
                Q11-3  R51-1  U146-10  U146-5  U146-2
    3           U124-3  U146-3
    4            S5D
                R109-2  U124-1  U124-4  U124-10  U10-13  U146-4  U123-4
                U123-10  U123-13  U117-4  U117-5  U117-6  U117-7
    5
                Q11-3  R51-1  U146-10  U146-5  U146-2
    6            C14M
                U146-6  R100-1  U117-10  U119-9  U79-7  U85-11
    7           GND
    8            C14M*
                U141-13  U146-8  U124-11  J21-2
    9           GND
    10
                Q11-3  R51-1  U146-10  U146-5  U146-2
    11          U119-5  U146-11
    12           C7M
                J15-36  J14-36  J13-36  J12-36  U141-9  U119-2  U146-12
                U90-14
    13           C3.5M
                U132-10  U141-10  U146-13  U119-7  J20-3
    14          +5V

U147 4-5 LS11 14 K8
    1            C3.5M*
                U135-13  U119-6  U147-1  U90-2
    2            COLRGATE
                J20-8  U147-2  U126-6
    3            A15
                J15-17  J14-17  J13-17  J12-17  U3-4  U147-3  U70-12
                U174-16  U6-7
    4            A14
                J15-16  J14-16  J13-16  J12-16  U3-7  U147-4  U70-9
                U6-16  U174-4
    5            IND*
                U136-10  U147-5  U174-12
    6            C-FXXX
                U71-15  U180-2  U71-14  U71-13  U147-6  U147-9  U165-1
    7           GND
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     8          CXXX
               U176-15  U74-6  U150-1  U147-8
     9          C-FXXX
               U71-15  U180-2  U71-14  U71-13  U147-6  U147-9  U165-1
     10         IOEN
               U73-8  P19-3  U147-10
     11        U147-11  U155-13
     12         COLORBURST
               R55-1  U147-12
     13         COLORKILL*
               U147-13  U87-11  J20-9
     14        +5V

U148 4 LS21 14 J4
     1          IRQ1*
               U101-14  J12-30  P2-7  U148-1
     2          IRQ2*
               U101-15  J13-30  P2-6  U148-2
     3         NO CONNECTION
     4          IRQ3*
               U97-7  J14-30  P2-4  U148-4
     5          IRQ4*
               U97-6  J15-30  P2-3  U148-5
     6         U155-8  U148-6
     7         GND
     8          FSPACE*
               U180-1  U176-1  U165-12  U123-12  U148-8
     9          FFDX*
               U112-5  U73-23  U148-9
     10         FFEX*
               U97-23  U148-10  U112-6
     11        NO CONNECTION
     12         SEL6551*
               U98-3  U76-7  U148-12
     13         C07X*
               U180-6  U77-7  U112-13  U158-1  U72-1  U150-5  U148-13
     14        +5V

U150 2-4 S10 14 E9
     1          CXXX
               U176-15  U74-6  U150-1  U147-8
     2          GPH2
               U150-2  U77-6  U162-4
     3          SEL1M
               U180-15  U174-2  U150-3  U73-9  P19-2
     4          CIM*
               U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
               U126-11  U85-4  U144-5  U132-12  U150-4
     5          C07X*
               U180-6  U77-7  U112-13  U158-1  U72-1  U150-5  U148-13
     6         U141-4  U150-6
     7         GND
     8           RAMR/W*
                J17-11  U150-8
     9           RAS
                U152-13  U150-9  U119-14  U12-2  U12-5  U12-10  U12-13
     10          Q0
                U119-13  U150-10  U117-15  U131-2  U78-11
     11          WRAMEN
                U180-12  U150-11
     12          IOSTRB*
                J15-20  U150-12  J14-20  J13-20  J12-20
     13          A11
                J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
                U150-13  U74-5  U67-12  U3-5  U174-5
     14         +5V

U152  3-9  LS00  14  E7
     1          U126-14  U152-1  U154-11
     2           HPE*
                U135-3  U152-2  U114-9  U116-9  U116-12
     3          U126-17  U152-3
     4           PPA8
                U158-4  U152-4  U158-5  U65-17  U64-23  U132-5
     5          U158-8  U152-5
     6          U152-6  U144-10  U131-1
     7          GND
     8          U124-2  U152-8
     9          U152-9  U140-9
     10         U152-10  U152-11  U140-11
     11         U152-10  U152-11  U140-11
     12          Q0*
                U152-12  U144-2  U85-2
     13          RAS
                U152-13  U150-9  U119-14  U12-2  U12-5  U12-10  U12-13
     14         +5V

U153  2-4-5  LS08  14  E8
     1          U158-11  U153-1  U180-4
     2           CIM*
                U153-2  U123-2  U119-11  U120-2  U118-2  U116-2  U114-2
                U126-11  U85-4  U144-5  U132-12  U150-4
     3           AY*
                U13-14  U11-3  U9-14  U5-14  U2-14  U153-3  U6-15
                U3-1
     4           S399
                U174-14  U153-4
     5           DA7
                J16-16  U153-5  U84-3  U69-14
     6          U10-1  U153-6
     7          GND
     8           TROMSEL*
                U153-8  U162-13  U64-20
     9           DMAI*
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                U176-2  J12-28  J15-28  J14-28  J13-28  U163-5  P14-2
                U153-9
     10          ROMSEL*
                U153-10  U165-9  U176-3
     11         U153-11  U79-6
     12          CH80*
                U139-9  U153-12  U87-14
     13          C7M*
                U119-3  U153-13  U119-4
     14         +5V

U154 5-9 LS08 14 F8
     1          U139-8  U154-1
     2           Q3
                J14-37  U85-3  J15-37  J13-37  J12-37  U117-12  R93-1
                U154-2
     3          U173-3  U154-3
     4           V4
                U87-19  U1-2  U154-4  U120-12  U1-11
     5           V3
                U120-13  U1-15  U154-5  U1-6
     6           VBL
                U175-15  U87-5  U97-19  U97-18  U121-19  U154-6
     7          GND
     8           V2*V5
                U121-8  U154-8  U5-3
     9           V5
                U120-11  U154-9
     10          V2
                U120-14  U154-10  U87-22
     11         U126-14  U152-1  U154-11
     12          RBL
                U121-13  U154-12
     13          SCRN
                U154-13  U73-7  P19-4
     14         +5V

U155 3-4-8 LS02 14 D9
     1          U155-1  U164-1
     2           NMI*
                U139-6  U65-6  U155-2
     3           AIISW*
                U165-6  U71-12  U97-8  U178-1  U178-13  U177-15  U87-3
                U155-3
     4          U144-9  U131-13  U155-4
     5           PA9
                U64-22  U155-5  U65-18  U67-6
     6           PA10
                U64-19  U155-6  U65-19  U67-10
     7          GND
     8          U155-8  U148-6
     9           H1
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                U114-13  U2-11  U155-9
     10          IOIRQ
                U73-40  U155-10
     11          A12
                J15-14  J14-14  J13-14  J12-14  U9-12  U155-11  U165-14
                U70-4  U71-2  U174-6
     12          A13
                J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
                U71-1  U70-7  U6-5  U3-6  U174-7
     13         U147-11  U155-13
     14         +5V

U158 3-4-9 LS32 14 J8
     1           C07X*
                U180-6  U77-7  U112-13  U158-1  U72-1  U150-5  U148-13
     2           IR*/W
                U91-3  U68-11  U158-2  U163-10
     3           CLKRD
                U72-2  U158-3
     4           PPA8
                U158-4  U152-4  U158-5  U65-17  U64-23  U132-5
     5           PPA8
                U158-4  U152-4  U158-5  U65-17  U64-23  U132-5
     6           PA8
                U11-2  U174-17  U67-3  U158-6
     7          GND
     8          U158-8  U152-5
     9           PRIMSTK
                U73-4  P19-7  U158-9
     10          ABK4
                U11-15  U174-1  U10-15  U158-10
     11         U158-11  U153-1  U180-4
     12         U158-12  U126-15
     13          RFSH
                U158-13  U11-16  U126-2
     14         +5V

U160 3-7 LS125 14 J9
     1           ENSEL
                U161-4  U160-1  U177-11  U161-1
     2           PSW3/SCO
                U169-16  U161-3  U160-2
     3           SCO
                U160-3  U73-18  U160-5  U101-1
     4           PDL2
                U160-4  U105-2  U75-10
     5           SCO
                U160-3  U73-18  U160-5  U101-1
     6          R86-1  U160-6  U161-2
     7          GND
     8           SER
                U73-19  U160-8  U161-9
     9            PX1/SER
                 U105-12  U161-8  U160-9  U169-18
     10           ENSIO
                 U160-10  U177-12  U161-10
     11           R/W*
                 J15-18  J14-18  J13-18  J12-18  U3-3  U136-9  U180-17
                 U176-6  U165-11  U160-11
     12           IR/W*
                 U98-28  U97-22  U112-14  U73-22  U163-11  U65-34  U160-12
     13           DMA1
                 U131-11  U163-6  U131-10  U131-9  U160-13
     14          +5V

U161 6-7 LS126 14 J10
     1            ENSEL
                 U161-4  U160-1  U177-11  U161-1
     2           R86-1  U160-6  U161-2
     3            PSW3/SCO
                 U169-16  U161-3  U160-2
     4            ENSEL
                 U161-4  U160-1  U177-11  U161-1
     5            AXCO
                 U161-5  U75-12  U105-1
     6            Y1/XCOUF
                 U161-6  U169-17  U105-11
     7           GND
     8            PX1/SER
                 U105-12  U161-8  U160-9  U169-18
     9            SER
                 U73-19  U160-8  U161-9
     10           ENSIO
                 U160-10  U177-12  U161-10
     11          U161-11  U92-5  R67-2
     12          U93-12  U161-12  U93-11
     13          U161-13  U93-10
     14          +5V

U162 3-4-5-8-9 LS04 14 H8
     1            DTRDY*
                 U107-16  U162-1
     2           U96-10  U162-2  U139-2
     3            GPH1
                 U162-3  U76-4  U141-6  U74-4
     4            GPH2
                 U150-2  U77-6  U162-4
     5            BTO
                 U88-3  U85-18  U162-5  U79-13  U83-4  U83-1
     6            BTO*
                 U83-3  U162-6
     7           GND
     8            UUTSUNK*
                 J19-1  U118-9  U162-8  U120-9
     9          U162-9  U120-15
     10          RESET*
                U65-40  U162-10  U98-4  U97-34  U73-34  U75-15  U79-9
                U173-1
     11          UUTUPRST
                R92-2  U162-11  J21-4  U164-3
     12          TROMSEL
                U162-12  U144-13
     13          TROMSEL*
                U153-8  U162-13  U64-20
     14         +5V

U163 3-5-6 LS04 14 K9
     1           DEXT*
                U167-18  U94-10  U178-2  U163-1
     2           PINT*
                U167-19  U163-2  U178-5
     3           TSADB*
                J15-22  J12-22  J14-22  J13-22  U163-3  P14-3
     4          U70-15  U163-4  U67-15  U63-19  U63-1
     5           DMAI*
                U176-2  J12-28  J15-28  J14-28  J13-28  U163-5  P14-2
                U153-9
     6           DMAI
                U131-11  U163-6  U131-10  U131-9  U160-13
     7          GND
     8           NTSCB
                P3-8  U163-8
     9           NTSCB*
                U163-9  U90-9
     10          IR*/W
                U91-3  U68-11  U158-2  U163-10
     11          IR/W*
                U98-28  U97-22  U112-14  U73-22  U163-11  U65-34  U160-12
     12          DWRREQ
                U166-14  U163-12
     13         U163-13  U94-12  U92-4
     14         +5V

U164 2-6-8 LS05 14 H9
     1          U155-1  U164-1
     2           IORESET*
                J12-31  J13-31  J14-31  J15-31  P14-6  U164-2  U164-4
                U96-4  U94-15
     3           UUTUPRST
                R92-2  U162-11  J21-4  U164-3
     4           IORESET*
                J12-31  J13-31  J14-31  J15-31  P14-6  U164-2  U164-4
                U96-4  U94-15
     5           APPLEII*
                J7-5  P11-5  U106-12  U164-5
     6          U164-6  C17-2  X5-2  C75-2
     7          GND
     8           RDY
                J15-21  U164-8  J14-21  J13-21  J12-21  P14-4  U65-2
     9           PRDY
                U164-9  U174-13
    10           DT1M
                R31-1  U164-10  C7-2  U96-2  U96-6
    11           MOTEN*
                U164-11  U94-9
    12           MOTON*
                U179-1  U92-15  U178-15  R65-2  U164-12  U92-16
    13           MOTON
                U164-13  U96-5
    14          +5V

U165 4 LS133 16 J7
     1           C-FXXX
                U71-15  U180-2  U71-14  U71-13  U147-6  U147-9  U165-1
     2           S5A
                R106-2  U165-2  U165-3  U165-4  U165-5  U173-4  U173-13
                U173-10
     3           S5A
                R106-2  U165-2  U165-3  U165-4  U165-5  U173-4  U173-13
                U173-10
     4           S5A
                R106-2  U165-2  U165-3  U165-4  U165-5  U173-4  U173-13
                U173-10
     5           S5A
                R106-2  U165-2  U165-3  U165-4  U165-5  U173-4  U173-13
                U173-10
     6           AIISW*
                U165-6  U71-12  U97-8  U178-1  U178-13  U177-15  U87-3
                U155-3
     7           FFCX*
                U165-7  U112-4
     8          GND
     9           ROMSEL*
                U153-10  U165-9  U176-3
    10           ROMSEL1
                U165-10  U73-2  P19-9
    11           R/W*
                J15-18  J14-18  J13-18  J12-18  U3-3  U136-9  U180-17
                U176-6  U165-11  U160-11
    12           FSPACE*
                U180-1  U176-1  U165-12  U123-12  U148-8
    13           INH*
                J15-32  J14-32  J13-32  J12-32  U176-4  U165-13  P14-5
    14           A12
                J15-14  J14-14  J13-14  J12-14  U9-12  U155-11  U165-14
                U70-4  U71-2  U174-6
    15           A13
                J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
                U71-1  U70-7  U6-5  U3-6  U174-7
     16         +5V

U166 6 FILTER 20 N13
     1          GNDF
     2           ENBL3.E*
                J1-21  U166-2
     3           WRDATA
                J6-18  U166-3  J1-18
     4           RDDATA
                J6-16  U166-4  J1-16
     5           ENBL1.E*
                J1-14  U166-5
     6           ENBL1.I*
                J6-14  U166-6
     7           WRREQ
                J6-10  U166-7  J1-10
     8           DPH2
                J6-6  U166-8  J1-6
     9           DPH0
                J6-2  U166-9  J1-2
     10         GNDF
     11         GNDF
     12          VA1
                U166-12  U175-4  U94-4
     13          VC1
                U166-13  U175-2  U94-6
     14          DWRREQ
                U166-14  U163-12
     15          PENBL1,I*
                U166-15  U178-4
     16          PENBLE*
                U166-16  U178-7
     17          DRDATA
                U166-17  U93-13
     18          DWRDATA
                U166-18  U92-19  U93-2
     19          PENBL3,E*
                U166-19  U179-7
     20         GNDF

U167 6 FILTER 20 M13
     1          GNDF
     2           EXT*
                J1-26  U167-2
     3           INT*
                J6-26  U167-3
     4           WRPROT
                J6-20  U167-4  J1-20
     5           AII*
                U167-5  J1-23  J6-23
     6           ENBL2.E*
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            J1-22  U167-6
     7       SIDE2/1
            J6-24  U167-7  J1-24
     8       DPH3
            J6-8  U167-8  J1-8
     9       DPH1
            J6-4  U167-9  J1-4
     10     GNDF
     11     GNDF
     12      VB1
            U167-12  U175-3  U94-5
     13      PDPH3
            U167-13  U94-7
     14      PSIDE
            U167-14  U177-7
     15      PENBL2,E*
            U167-15  U179-6
     16      PAII
            U178-12  U167-16
     17      DWRPROTT
            U167-17  U91-11
     18      DEXT*
            U167-18  U94-10  U178-2  U163-1
     19      PINT*
            U167-19  U163-2  U178-5
     20     GNDF

 U169 7 FILTER 20 N10
     1      GNDF
     2       SW1/MGNSW
            J3-5  U169-2
     3       X1/SER
            J3-4  U169-3
     4       Y1/XCO
            J3-8  U169-4
     5       SW3/SCO
            J3-9  U169-5
     6       Y0
            U169-6  J2-8
     7       SW2
            U169-7  J2-5
     8       SW0
            U169-8  J2-9
     9       X0
            U169-9  J2-4
     10     GNDF
     11     GNDF
     12      X0UF
            U105-15  U169-12
     13      SW0UF
            U101-4  U169-13
     14      SW2UF
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               U101-2  U169-14
     15         YOUF
               U105-13  U169-15
     16         PSW3/SCO
               U169-16  U161-3  U160-2
     17         Y1/XCOUF
               U161-6  U169-17  U105-11
     18         PX1/SER
               U105-12  U161-8  U160-9  U169-18
     19         SW1/MGNSWUF
               R85-2  U169-19  U73-39  U101-3
     20        GNDF

U171 8 FILTER 20 K13
     1         GNDF
     2          KX6
               J7-26  U171-2
     3          KX4
               J7-21  U171-3
     4          KX3
               J7-20  U171-4
     5          KX5
               J7-19  U171-5
     6          KX1
               J7-18  U171-6
     7          KX7
               J7-17  U171-7
     8          KX2
               J7-16  U171-8
     9          KX0
               J7-14  U171-9
     10        GNDF
     11        GNDF
     12         KX0UF
               U171-12  U107-40
     13         KX2UF
               U171-13  U107-38
     14         KX7UF
               U171-14  U107-33
     15         KX1UF
               U171-15  U107-39
     16         KX5UF
               U171-16  U107-35
     17         KX3UF
               U171-17  U107-37
     18         KX4UF
               U171-18  U107-36
     19         KX6UF
               U171-19  U107-34
     20        GNDF

U172 7 FILTER 20 N3
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```
     1          GNDF
     2           EXTSPK2
                J11-2  U172-2
     3           DCD
                J4-8  U172-3
     4           DTR
                J4-20  U172-4
     5           DSR
                J4-6  U172-5
     6           CTS
                J4-5  U172-6
     7           RTS
                J4-4  U172-7
     8           DATA IN
                J4-3  U172-8
     9           TXD
                J4-2  U172-9
     10         GNDF
     11         GNDF
     12          PTXD
                U172-12  U99-6
     13          PRXD
                U172-13  U100-1
     14          PRTS
                U172-14  U99-11
     15          PCTS
                R87-2  U172-15  U100-4
     16          PDSR
                R88-2  U172-16  U100-10
     17          PDTR
                U172-17  U99-8
     18          PDCD
                R89-2  U172-18  U100-13
     19          PEXTSPK
                U172-19  C10-2
     20         GNDF

U173 5-7 LS74 14 H7
     1           RESET*
                U65-40  U162-10  U98-4  U97-34  U73-34  U75-15  U79-9
                U173-1
     2          U173-2  U136-6
     3          U173-3  U154-3
     4           S5A
                R106-2  U165-2  U165-3  U165-4  U165-5  U173-4  U173-13
                U173-10
     5           INV
                U83-11  U173-5
     6          NO CONNECTION
     7          GND
     8          U173-8  U173-12
     9           AIISPKR
```

```
                R35-1  U173-9
     10          S5A
                R106-2  U165-2  U165-3  U165-4  U165-5  U173-4  U173-13
                U173-10
     11          SPKR*
                U173-11  U77-12
     12         U173-8  U173-12
     13          S5A
                R106-2  U165-2  U165-3  U165-4  U165-5  U173-4  U173-13
                U173-10
     14         +5V

U174 2 7643 18 341-0043 C10
     1           ABK4
                U11-15  U174-1  U10-15  U158-10
     2           SEL1M
                U180-15  U174-2  U150-3  U73-9  P19-2
     3           SYNC
                U65-7  U136-1  J15-35  U174-3  J14-35  J13-35  J12-35
     4           A14
                J15-16  J14-16  J13-16  J12-16  U3-7  U147-4  U70-9
                U6-16  U174-4
     5           A11
                J15-13  J14-13  J13-13  J12-13  U128-12  U6-6  U71-3
                U150-13  U74-5  U67-12  U3-5  U174-5
     6           A12
                J15-14  J14-14  J13-14  J12-14  U9-12  U155-11  U165-14
                U70-4  U71-2  U174-6
     7           A13
                J15-15  J14-15  J13-15  J12-15  U128-4  U155-12  U165-15
                U71-1  U70-7  U6-5  U3-6  U174-7
     8          GND
     9          GND
     10         GND
     11         NO CONNECTION
     12          IND*
                U136-10  U147-5  U174-12
     13          PRDY
                U164-9  U174-13
     14          S399
                U174-14  U153-4
     15          ZPAGE*
                U11-1  U174-15  U67-1  U131-8  U70-1
     16           A15
                J15-17  J14-17  J13-17  J12-17  U3-4  U147-3  U70-12
                U174-16  U6-7
     17           PA8
                U11-2  U174-17  U67-3  U158-6
     18         +5V

U175 2 7643 18 341-0055 F9
     1           RDHIRES
```

```
             U175-1  U11-17  U3-2  U6-3  U126-9
    2         VC1
             U166-13  U175-2  U94-6
    3         VB1
             U167-12  U175-3  U94-5
    4         VA1
             U166-12  U175-4  U94-4
    5         VA
             U121-3  U175-5  U116-11  U82-5  U81-5
    6         VB
             U121-2  U175-6  U118-14  U82-6  U81-6
    7         VC
             U121-1  U175-7  U118-13  U83-15  U83-14  U82-7  U81-7
    8        GND
    9        GND
    10       GND
    11        ENHREG*
             U175-11  U78-1
    12        MUX3
             U9-13  U175-12
    13        MUX2
             U9-3  U175-13
    14        MUX1
             U101-12  U175-14  U5-13
    15        VBL
             U175-15  U87-5  U97-19  U97-18  U121-19  U154-6
    16        WE2114*
             U82-10  U175-16  U81-10  U144-6
    17        SCR
             U177-9  U175-17
    18       +5V

U176 4 7643 18 341-0045 F5
    1         FSPACE*
             U180-1  U176-1  U165-12  U123-12  U148-8
    2         DMAI*
             U176-2  J12-28  J15-28  J14-28  J13-28  U163-5  P14-2
             U153-9
    3         ROMSEL*
             U153-10  U165-9  U176-3
    4         INH*
             J15-32  J14-32  J13-32  J12-32  U176-4  U165-13  P14-5
    5        U74-10  U176-5
    6         R/W*
             J15-18  J14-18  J13-18  J12-18  U3-3  U136-9  U180-17
             U176-6  U165-11  U160-11
    7         C6XX*
             U176-7  U74-9
    8        GND
    9        GND
    10       GND
    11        RAMEN
```

```
                 U180-7  U176-11
     12          NO CONNECTION
     13           EN8304
                 U176-13  U68-9
     14           EN257
                 U176-14  U66-15  U69-15
     15           CXXX
                 U176-15  U74-6  U150-1  U147-8
     16           C7XX*
                 U176-16  U74-7
     17           PH2M
                 P19-10  U141-5  U65-39  U176-17
     18          +5V

U177 6 9334 16 L12
     1            A1
                 J15-3  J14-3  J13-3  J12-3  U2-10  U97-37  U98-14
                 U101-10  U177-1  U94-1  U73-37  U75-1  U63-16
     2            A2
                 J15-4  J14-4  J13-4  J12-4  U5-6  U101-9  U97-36
                 U177-2  U94-2  U75-2  U73-36  U63-14
     3            A3
                 J15-5  J14-5  J13-5  J12-5  U5-10  U109-1  U111-1
                 U97-35  U177-3  U94-3  U75-3  U73-35  U63-12
     4            EXT0
                 U179-2  U177-4
     5            EXT1
                 U179-3  U177-5
     6            INTON
                 U177-6  U178-3
     7            PSIDE
                 U167-14  U177-7
     8           GND
     9            SCR
                 U177-9  U175-17
     10           ENCWRT
                 U177-10  U144-1
     11           ENSEL
                 U161-4  U160-1  U177-11  U161-1
     12           ENSIO
                 U160-10  U177-12  U161-10
     13           A0
                 J15-2  J14-2  J13-2  J12-2  U2-6  U97-38  U98-13
                 U101-11  U94-13  U73-38  U75-13  U63-18  U177-13
     14           DEVSEL5*
                 U177-14  U76-10
     15           AIISW*
                 U165-6  U71-12  U97-8  U178-1  U178-13  U177-15  U87-3
                 U155-3
     16          +5V

U178 3-6 LS257 16 L11
```

```
     1          AIISW*
                U165-6  U71-12  U97-8  U178-1  U178-13  U177-15  U87-3
                U155-3
     2          DEXT*
                U167-18  U94-10  U178-2  U163-1
     3          INTON
                U177-6  U178-3
     4          PENBL1,I*
                U166-15  U178-4
     5          PINT*
                U167-19  U163-2  U178-5
     6          NENBLE*
                U179-5  U178-6
     7          PENBLE*
                U166-16  U178-7
     8          GND
     9          NO CONNECTION
     10         NO CONNECTION
     11         NO CONNECTION
     12         PAII
                U178-12  U167-16
     13         AIISW*
                U165-6  U71-12  U97-8  U178-1  U178-13  U177-15  U87-3
                U155-3
     14         GND
     15         MOTON*
                U179-1  U92-15  U178-15  R65-2  U164-12  U92-16
     16         +5V

U179 6-8 LS139 16 J11
     1          MOTON*
                U179-1  U92-15  U178-15  R65-2  U164-12  U92-16
     2          EXT0
                U179-2  U177-4
     3          EXT1
                U179-3  U177-5
     4          NO CONNECTION
     5          NENBLE*
                U179-5  U178-6
     6          PENBL2,E*
                U167-15  U179-6
     7          PENBL3,E*
                U166-19  U179-7
     8          GND
     9          NO CONNECTION
     10         NO CONNECTION
     11         X6-2  U179-11
     12         NO CONNECTION
     13         CONTROL*
                J7-11  U179-13  U107-28  U109-10  P11-2
     14         RESETLK*
                U179-14  U73-6  P19-5  U139-5
```

```
    15          KRESET*
               U139-12  R80-1  C71-1  U179-15  J7-15
    16         +5V

U180 9 7643 18 341-0046 F7
    1           FSPACE*
               U180-1  U176-1  U165-12  U123-12  U148-8
    2           C-FXXX
               U71-15  U180-2  U71-14  U71-13  U147-6  U147-9  U165-1
    3           IOSTOPD*
               U123-9  U112-15  U180-3
    4          U158-11  U153-1  U180-4
    5           C1M
               U132-2  U135-1  U119-10  U123-11  U180-5  U98-27  U80-11
               U84-11
    6           C07X*
               U180-6  U77-7  U112-13  U158-1  U72-1  U150-5  U148-13
    7           RAMEN
               U180-7  U176-11
    8          GND
    9          GND
    10         GND
    11         NO CONNECTION
    12          WRAMEN
               U180-12  U150-11
    13          PHASEN
               U140-12  U180-13
    14          PCS6522
               R68-1  U180-14
    15          SEL1M
               U180-15  U174-2  U150-3  U73-9  P19-2
    16          RWPR
               U73-5  P19-6  U180-16
    17          R/W*
               J15-18  J14-18  J13-18  J12-18  U3-3  U136-9  U180-17
               U176-6  U165-11  U160-11
    18         +5V

U181 7 556 14 A7
    1          C69-2  R75-2  U181-1  U181-2
    2          C69-2  R75-2  U181-1  U181-2
    3          NO CONNECTION
    4          +5V
    5          U181-5  U181-10
    6           C04X*
               U77-11  U181-6
    7          GND
    8          R77-2  U181-8  U181-12  C70-1
    9          U181-9  R78-1
    10         U181-5  U181-10
    11         NO CONNECTION
    12         R77-2  U181-8  U181-12  C70-1
```

```
     13          R76-2  R77-1  U181-13
     14          +5V

X1 4 SCHOTTKY 2 DIODE A2
     1           R9-1  T1-1  X1-1  U105-10
     2           U72-24  Q1-1  X1-2

X2 8 1N4148 2 DIODE L10
     1           U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
                 X3-1  C75-1
     2            ANYKEY
                 U107-4  R40-1  X2-2  U106-11  U109-3

X3 8 1N4148 2 DIODE L11
     1           U96-13  U96-12  U96-8  R40-2  X2-1  C18-1  C17-1
                 X3-1  C75-1
     2            KAPPLEII*
                 U106-9  X3-2  U111-6

X4 8 1N4148 2 DIODE A5
     1           +5V
     2            UPRST*
                 C20-1  U113-6  U113-2  R44-2  X4-2  X6-1

X5 8 1N4148 2 DIODE M7
     1           GND
     2           U164-6  C17-2  X5-2  C75-2

X6 8 1N4148 2 DIODE A6
     1            UPRST*
                 C20-1  U113-6  U113-2  R44-2  X4-2  X6-1
     2           X6-2  U179-11

X7 1 LED 2 LED M4
     1           +5V
     2           X7-2  R81-1

Y1 9 14MHZ 2 XTAL1 A12
     1           R52-1  Q10-3  Y1-1
     2

                 Y1-2  Q11-2  R49-2

Y2 4 32KHZ 2 XTAL2 A3
     1           Y2-1  U72-10  C3-3
     2           C4-1  U72-11  Y2-2


END OF DATA
```

APPLE III

MODULE REPLACEMENT PROCEDURES

TABLE OF CONTENTS **PAGE**

I. Peripheral Logic Access Cover Removal 2-35
II. Peripheral Card Removal/Installation 2-37
III. Keyboard Replacement 2-39
IV. Analog Board Replacement — Disk Assembly 2-42
V. Disk Mechanical Assembly Replacement—Disk Assembly 2-46
VI. Power Supply Replacement 2-48
VII. Logic Assembly Removal 2-51
VIII. Logic Assembly Replacement 2-54
  A) Memory Board Removal
  B) Memory Board Installation
  C) Encoder Board Removal
  D) Encoder Board Installation
  E) Main Logic Board Replacement

I. PERIPHERAL LOGIC ACCESS COVER REMOVAL

1. Power down the Apple ///. Disconnect the AC power cord from the source and then from the power supply receptacle of the Apple ///.

2. Disconnect all external cables. Refer to Figure 1.1.

3. Lift up the front edge of the Apple and tilt it up 90 degrees so that it rests on the back side of the casting.

4. Locate the 1/4 turn locking screw on each side of the Apple and, with a flat blade screw driver, turn each one 1/4 turn counterclockwise to loosen. Do not attempt to remove these screws as they are self capturing and will not normally come out. Refer to Figure 1.2 item A.

5. Lower the Apple /// to the operating position and with a hand on each side of the access cover lift up and pull forward to remove. Refer to Figure 1.3.

6. To replace the cover reverse the procedure as outlined in steps 1 through 5.

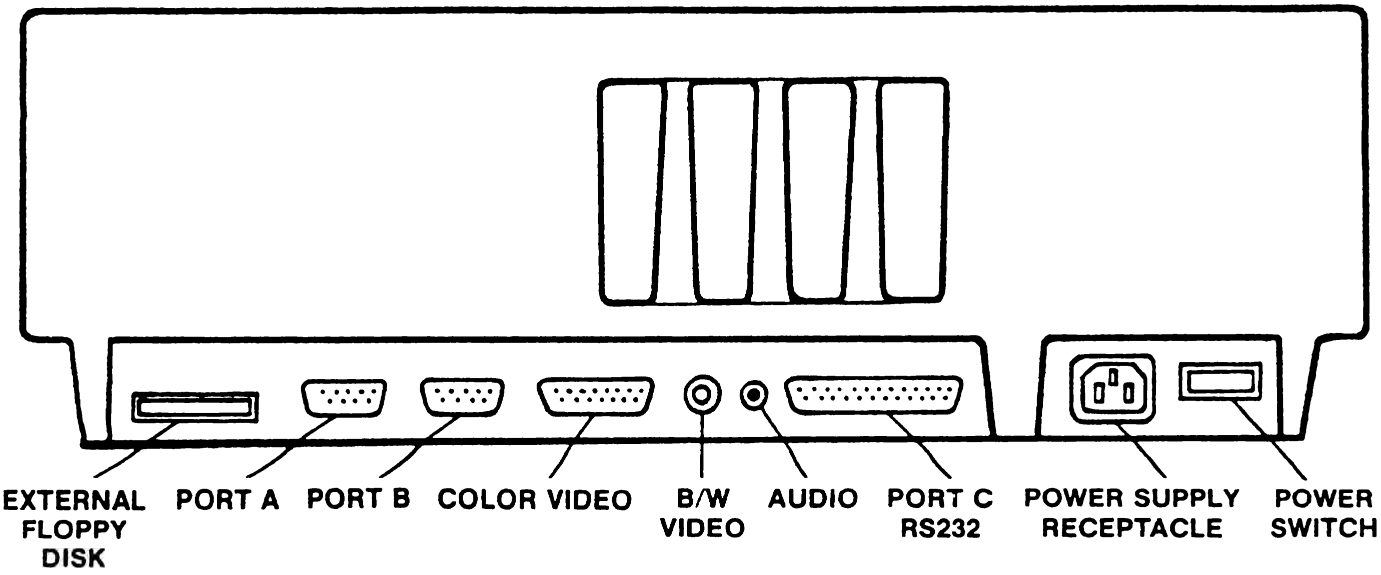


FIGURE 1.1

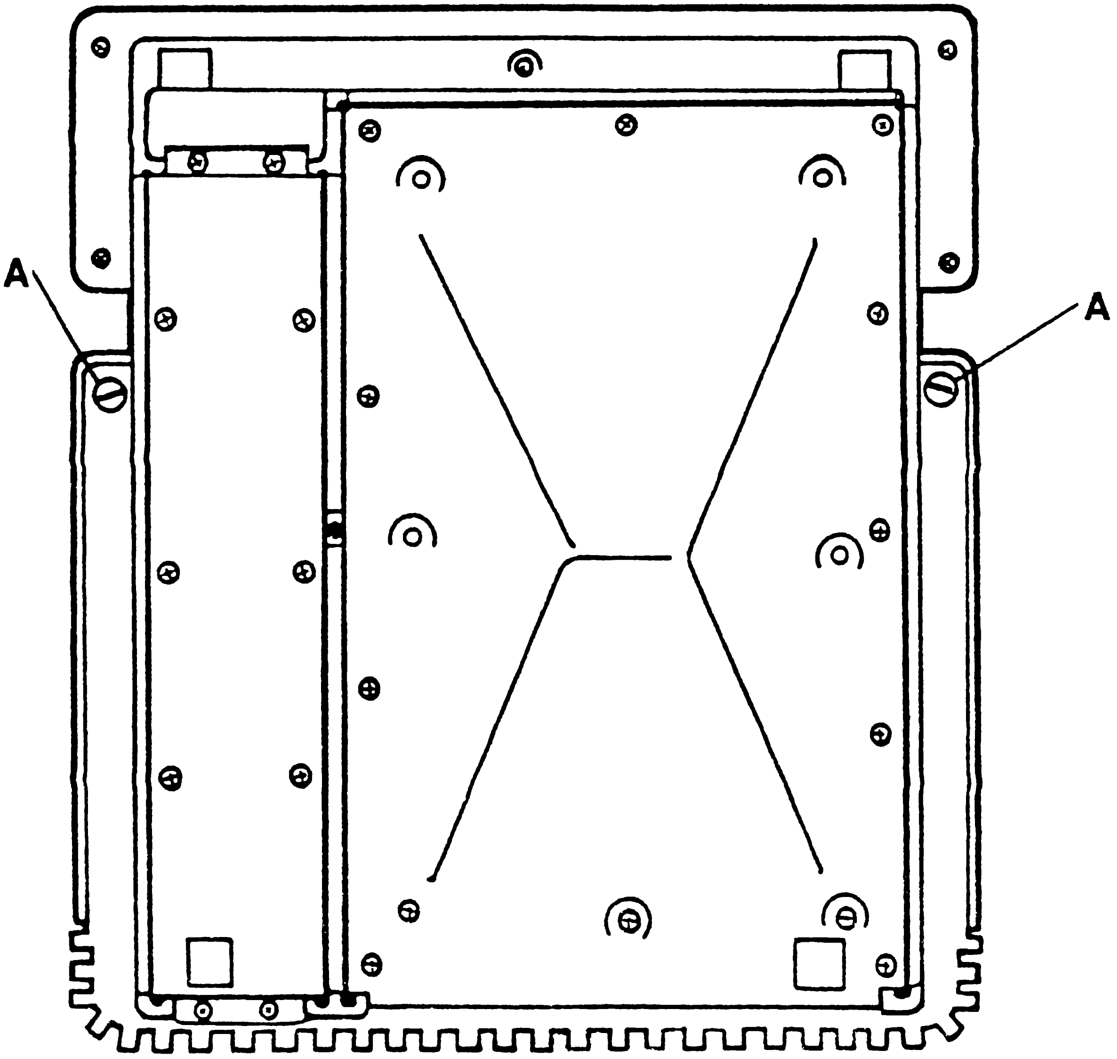


FIGURE 1.2

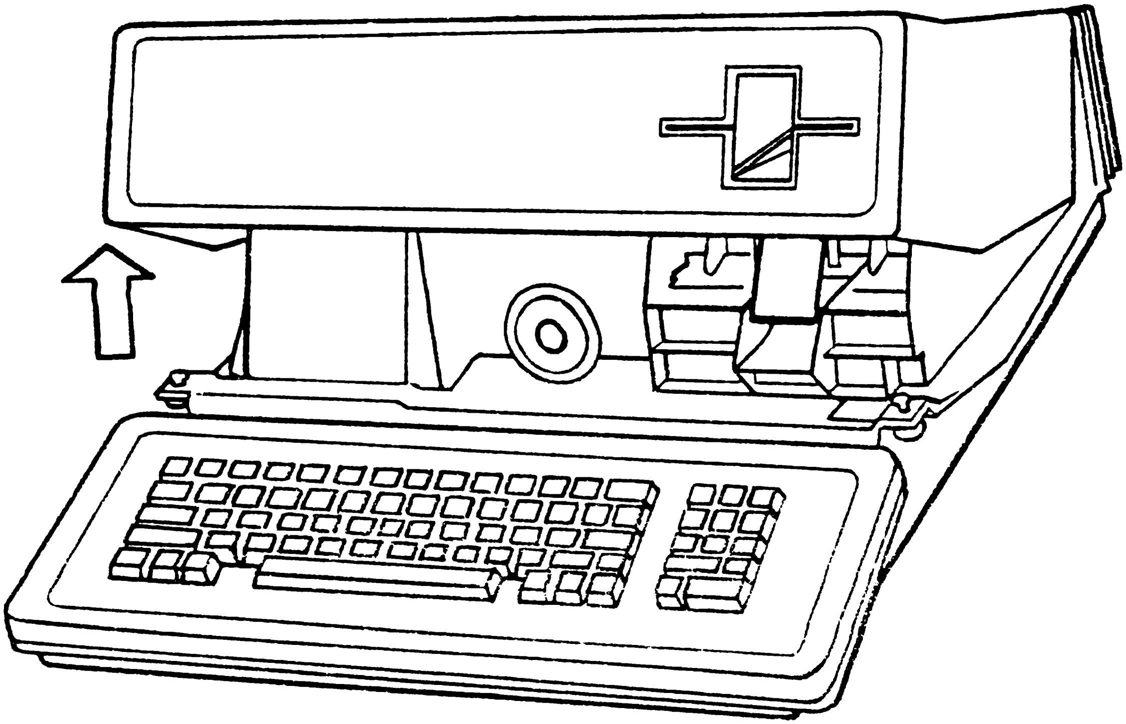


FIGURE 1.3

II. PERIPHERAL CARD REMOVAL/INSTALLATION

1. Power down the Apple ///. Disconnect the AC power cord from the source and then the power supply receptacle of the Apple ///.

2. Remove the peripheral logic access cover. Refer to Procedure I.

3. Locate the desired peripheral card. Refer to Figure 2.1 for slot number assignment. Disconnect all cords or cables connected to the peripheral card or cards to be removed.

4. Grasping the card firmly with both hands (using thumbs and forefingers) gently pull straight up on the card to free it from the connector and guide slots. Refer to Figure 2.2.

NOTE: If the card is too firmly captured to allow removal using just the fingers, a metal hook in the pilot hole near the top rear of the card may be used to gain a better grip on the card. Be careful not to tilt or rotate the card, or damage to the card and/or connector may occur.

CAUTION: Never remove or install any card or device with the power on or catastrophic shorting of signal to power supplies may occur.

5. To replace a peripheral card reverse the procedure as outlined in steps 1 through 4.

6. To install a new peripheral card, remove the RFI shield card (dummy card) from the desired slot and follow the detailed procedure enclosed with the new peripheral card.

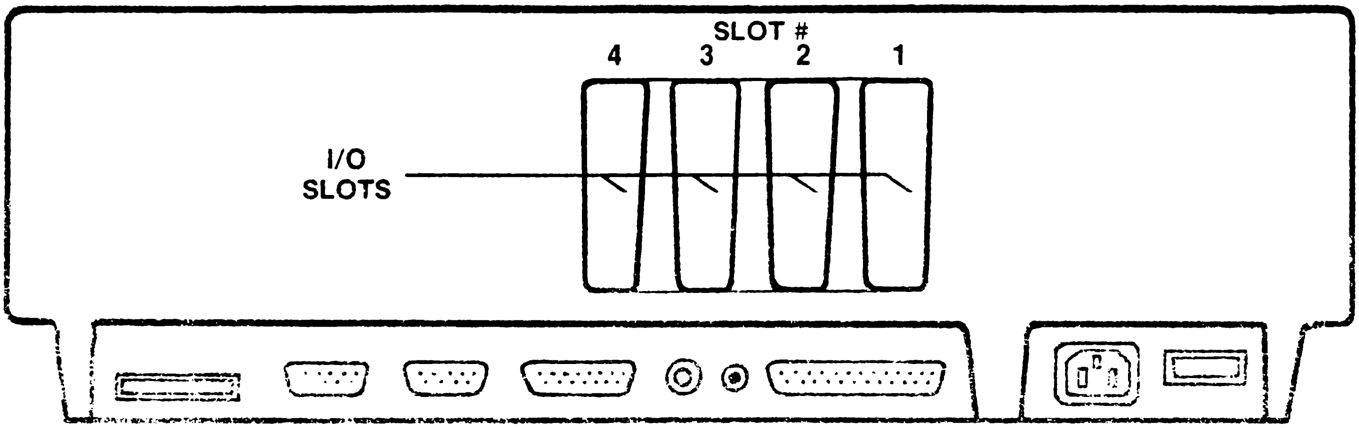


FIGURE 2.1

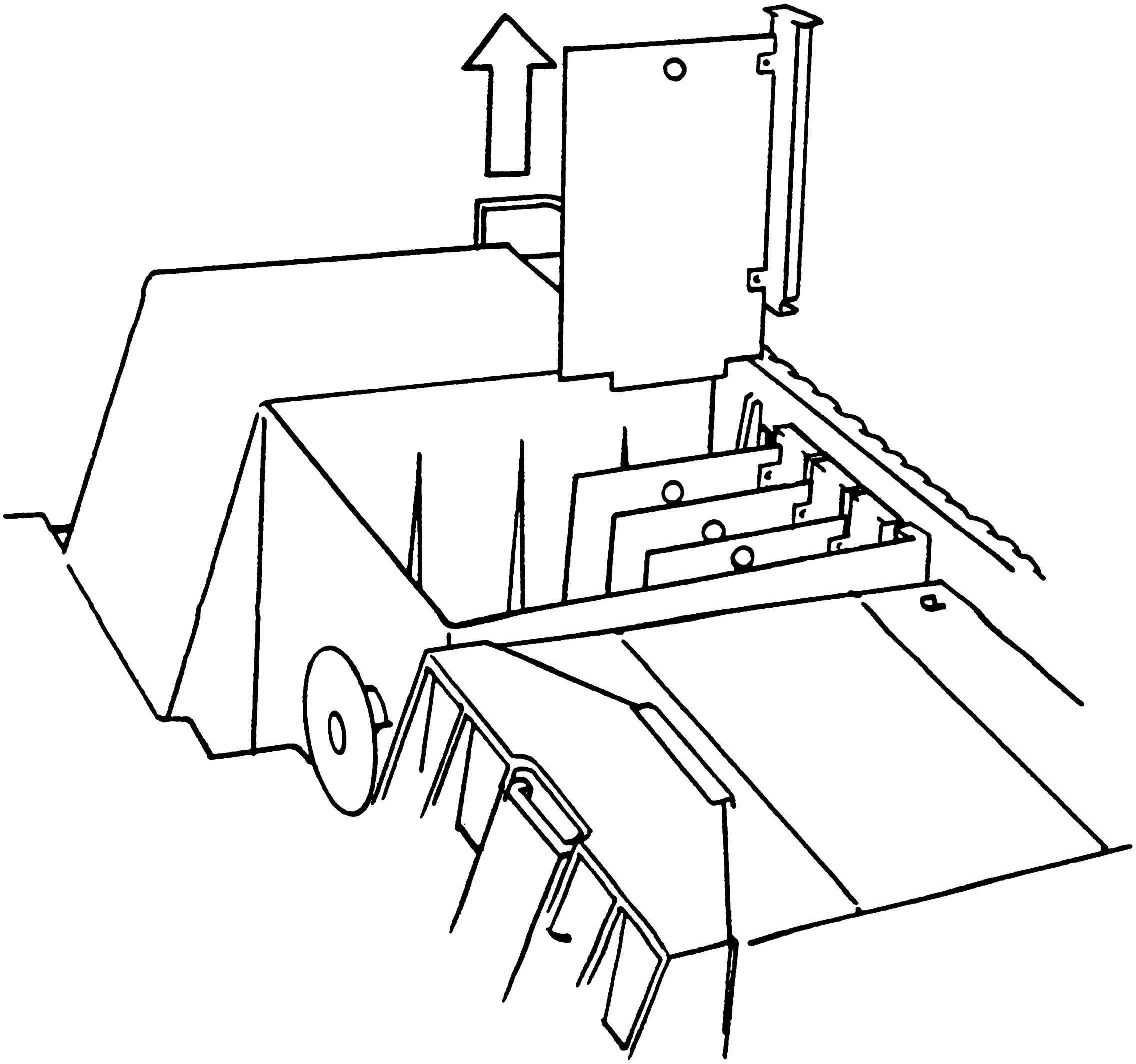


FIGURE 2.2

III. KEYBOARD REPLACEMENT

1. Power down the Apple ///. Disconnect the AC power cord from the source and then from the power supply receptacle of the Apple ///.

2. Place the Apple on its right side with the bottom facing you.

3. Locate, remove and retain the five (5) keyboard cover mounting screws located two each on the right and left ends and one in the front center. Refer to Figure 3.1 item A.

4. Remove the keyboard cover.

5. Place the Apple back into its normal operating position.

6. Locate and remove the two (2) retaining screws on the left end of the keyboard. Refer to Figure 3.2 item A. Loosen the right two (2) retaining screws. Refer to Figure 3.2 item B.

7. Remove the keyboard by lifting the left end and sliding the right end from under the loosened screws. Refer to Figure 3.3.

8. Disconnect the keyboard cable, located on the middle rear edge of the exposed keyboard. Refer to Figure 3.2 item C. Do not pull on the cable. Disconnect by using a screwdriver to push on the tab on the cable connector. Refer to Figure 3.2 item D.

9. Install the replacement keyboard by reversing the steps as outlined in 1 through 8 above. Observe that the keyboard cable makes a tight turn where it wraps to the underside of the keyboard. This is necessary if the keyboard cover is to fit properly.

Caution: Exercise care when tightening the five (5) keyboard cover screws to keep from stripping the threads in the cover.

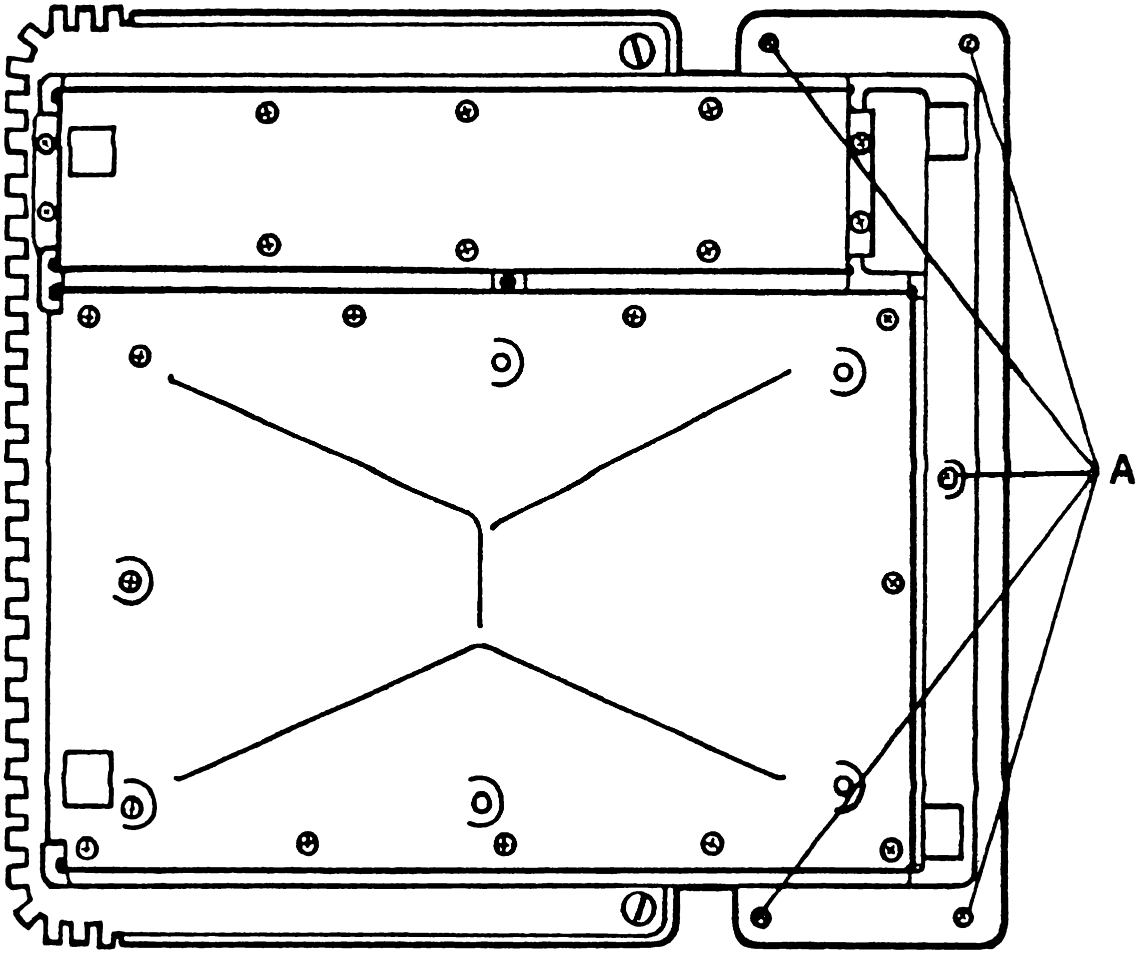


FIGURE 3.1

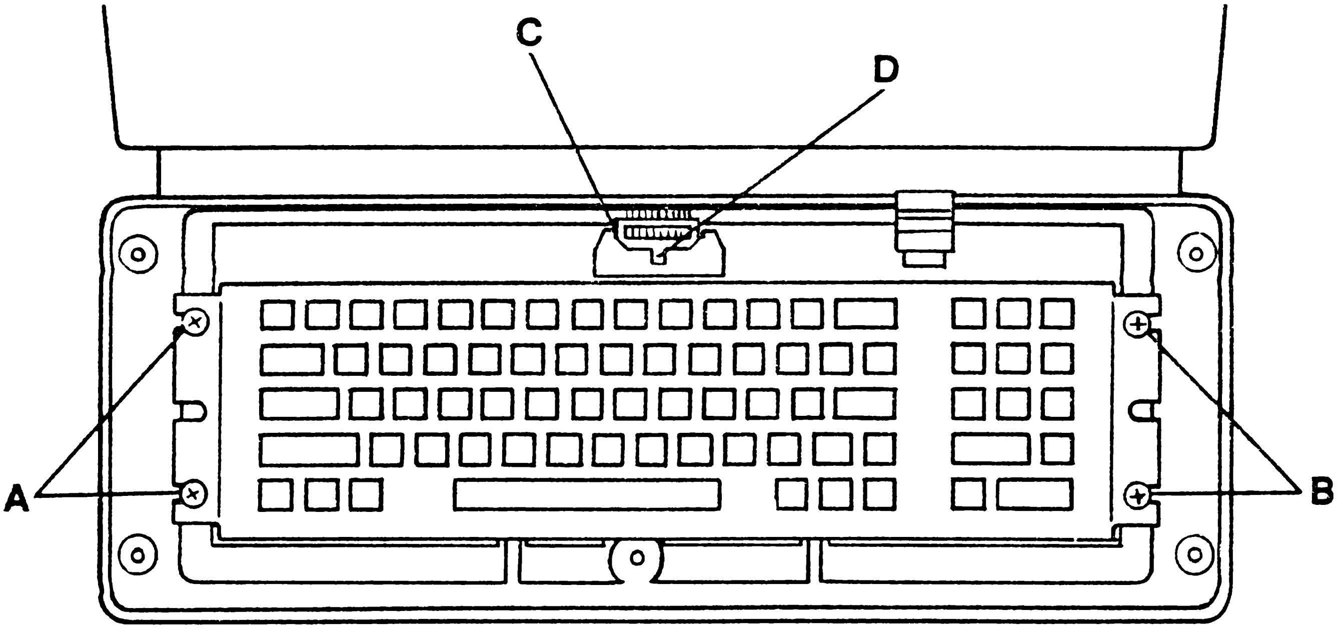


FIGURE 3.2

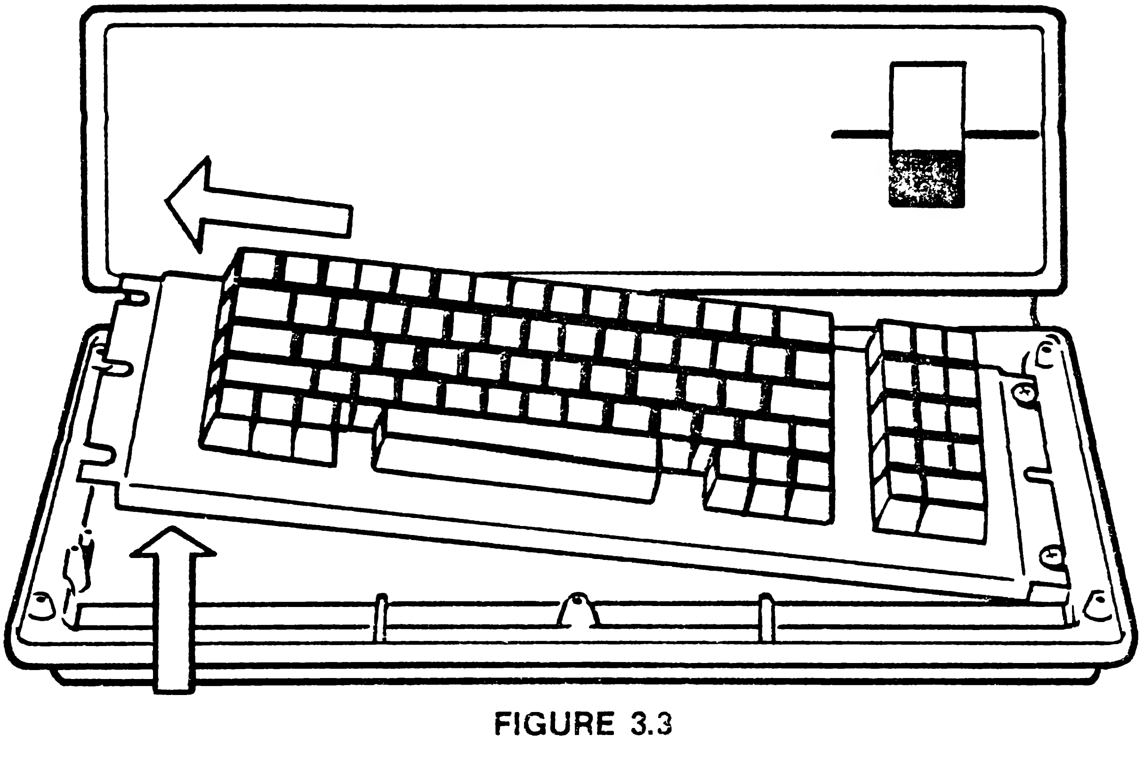


FIGURE 3.3

IV. ANALOG BOARD REPLACEMENT - DISK ASSEMBLY*

1. Power down the Apple ///. Disconnect the AC power cord from the source and then from the power supply receptacle of the Apple ///.

2. Remove the peripheral logic access cover. Refer to Procedure I.

3. Locate the two Tinnerman retaining clips which hold down the Disk Assembly shield. Refer to Figure 4.1 item A.

4. Using the blade of a screwdriver, slide the clips forward until the enlarged slots of the clips are around the mounting posts.

5. Remove and retain the clips.

6. Remove and retain the Disk Assembly shield by flexing the side out (Figure 4.1 item B) and lifting up on the shield. NOTE: The shield is only retained by the spring tension of the sides and four dimples which fit into depressions of the disk casting.

7. Disconnect the disk ribbon cable by pushing on the center tab of the plug with a small screwdriver. Do not pull it out by the cable. Refer to Figure 4.2 item A. Disconnect the read/write head cable. Refer to Figure 4.2 item B. Do not attempt to remove motor control cable yet. Refer to Figure 4.2 item D.

8. Remove and retain the two small Phillips head mounting screws which hold the Analog board at the front of the casting. Refer to Figure 4.2 item C.

9. To remove the Analog board, gently slide the left front of the board forward until it clears the guide holding the left edge. Then slide the right rear of the board to the left until it clears the guide holding the right edge. Refer to Figure 4.3. Tilt up the right rear of the board and lift clear.

10. At this time disconnect the motor control cable. Refer to Figure 4.2 item D. Note there are four nylon locking pawls which engage two holes in the board from both the top and bottom. These must be disengaged before the connector can be disconnected.

11. Install the replacement Analog board by reversing the steps as outlined in 1 through 10 above.

* The Disk Assembly is comprised of two modules, the Analog Board and the Disk Mechanical Assembly.

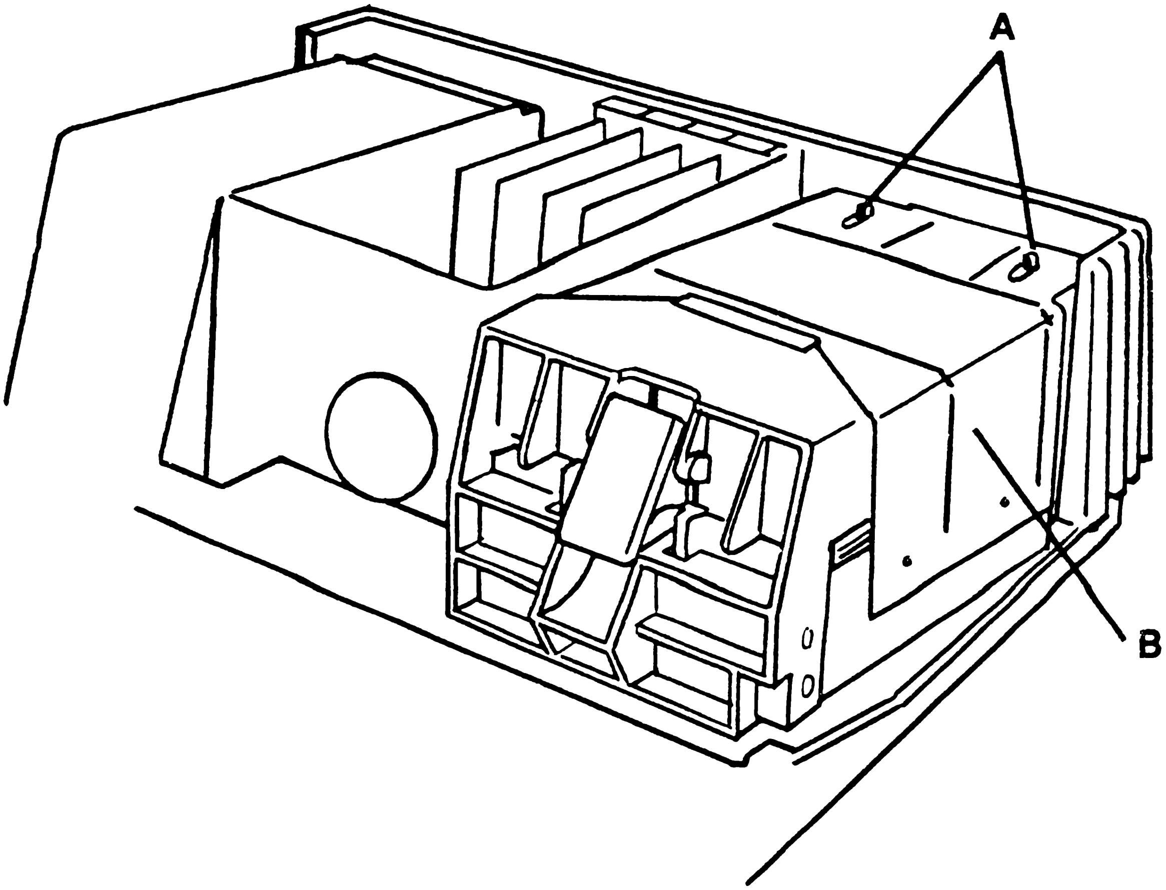


FIGURE 4.1

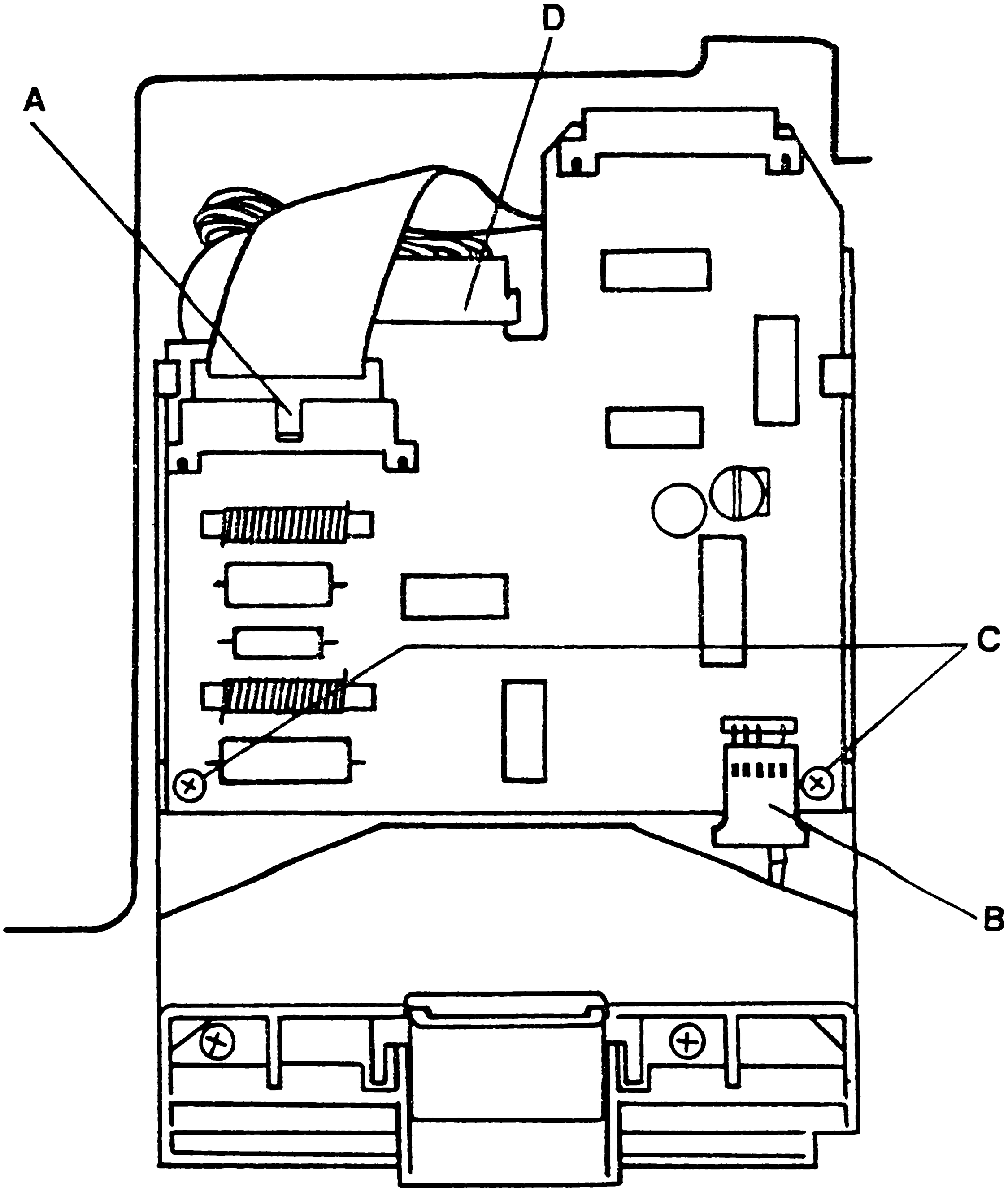


FIGURE 4.2

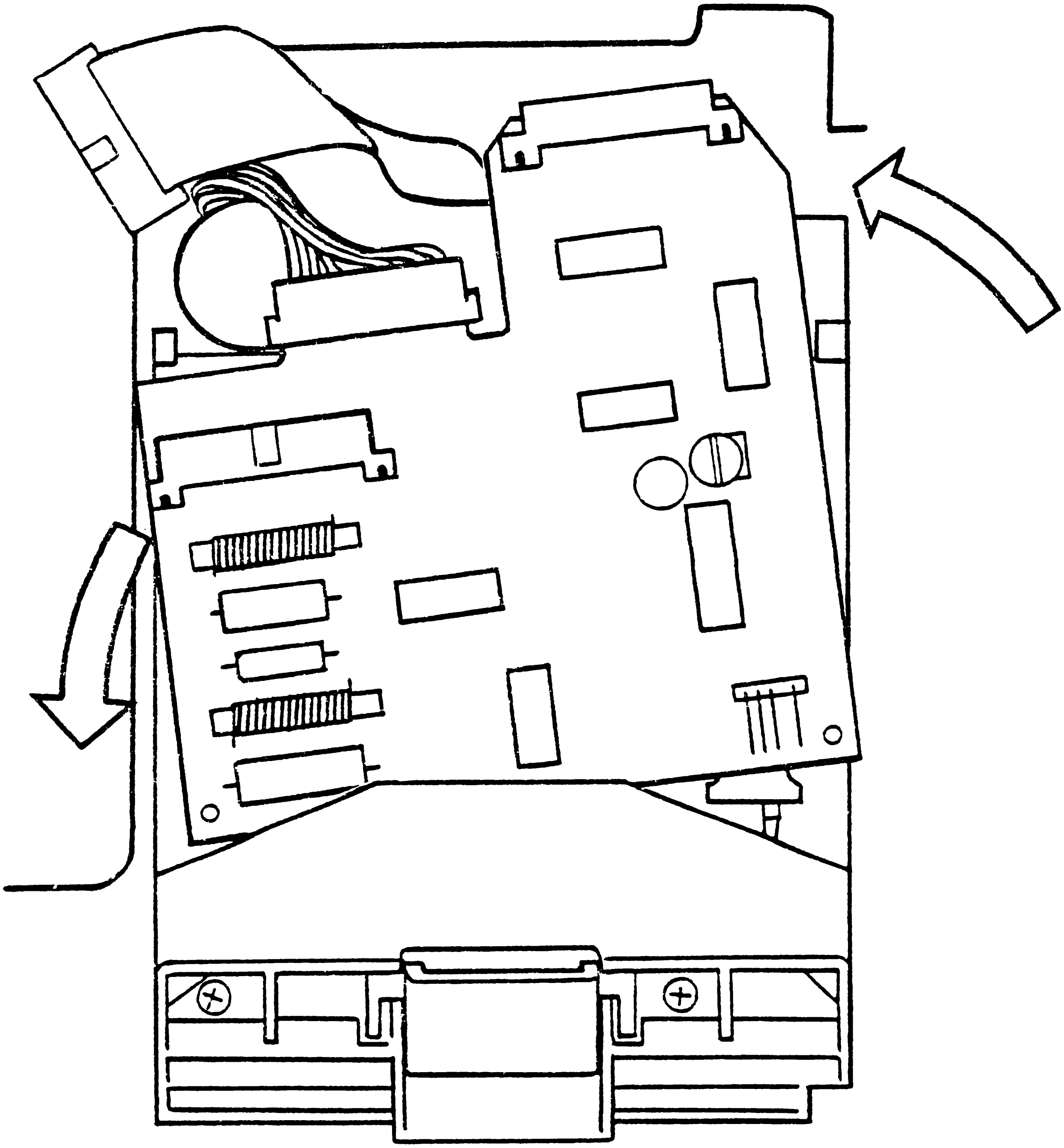


FIGURE 4.3

V. DISK MECHANICAL ASSEMBLY REPLACEMENT-DISK ASSEMBLY*

1. Power down the Apple ///. Disconnect the AC power cord from the source and then from the power supply receptacle of the Apple ///.

2. Remove the peripheral logic access cover. Refer to Procedure I.

3. Remove the disk shield. Refer to steps 3 through 6 in Procedure IV.

4. Disconnect the disk ribbon cable by pushing on the center tab of the plug with a small screwdriver. Refer to Figure 5.1 item A. Do not pull on the cable.

5. Scribe a line on the Apple /// chassis along the front (Figure 5.1 item B) and left side (Figure 5.1 item C) of the Disk Assembly bezel. This line will provide a location reference when the Disk Assembly is re-installed.

6. Locate the two Phillips head screws which mount the Disk Assembly to the Apple chassis. They can be seen by looking down through the front diskette guide and door assembly. Refer to Figure 5.1 item D.

7. Completely loosen the two mounting screws but let them remain sitting where they are.

8. Loosen (Don't Remove!) the Phillips head screw through the retaining clip which holds the lower left rear edge of the Disk casting. Refer to Figure 5.1 item E.

9. Remove the Disk Assembly by sliding it forward until it clears the retaining spring clip and then lift it from the chassis.

10. Recover the two front screws from the Disk Assembly.

11. Separate the Analog Board from the Disk Mechanical Assembly as outlined in Procedure IV step 9.

12. Install the replacement Disk Mechanical Assembly by reversing the steps as outlined in steps 1 through 11 above. Use the reference mark made in step 5 to insure proper alignment of the Disk Assembly.

---

* The Disk Assembly is comprised of two modules, the Analog Board and the Disk Mechanical assembly.

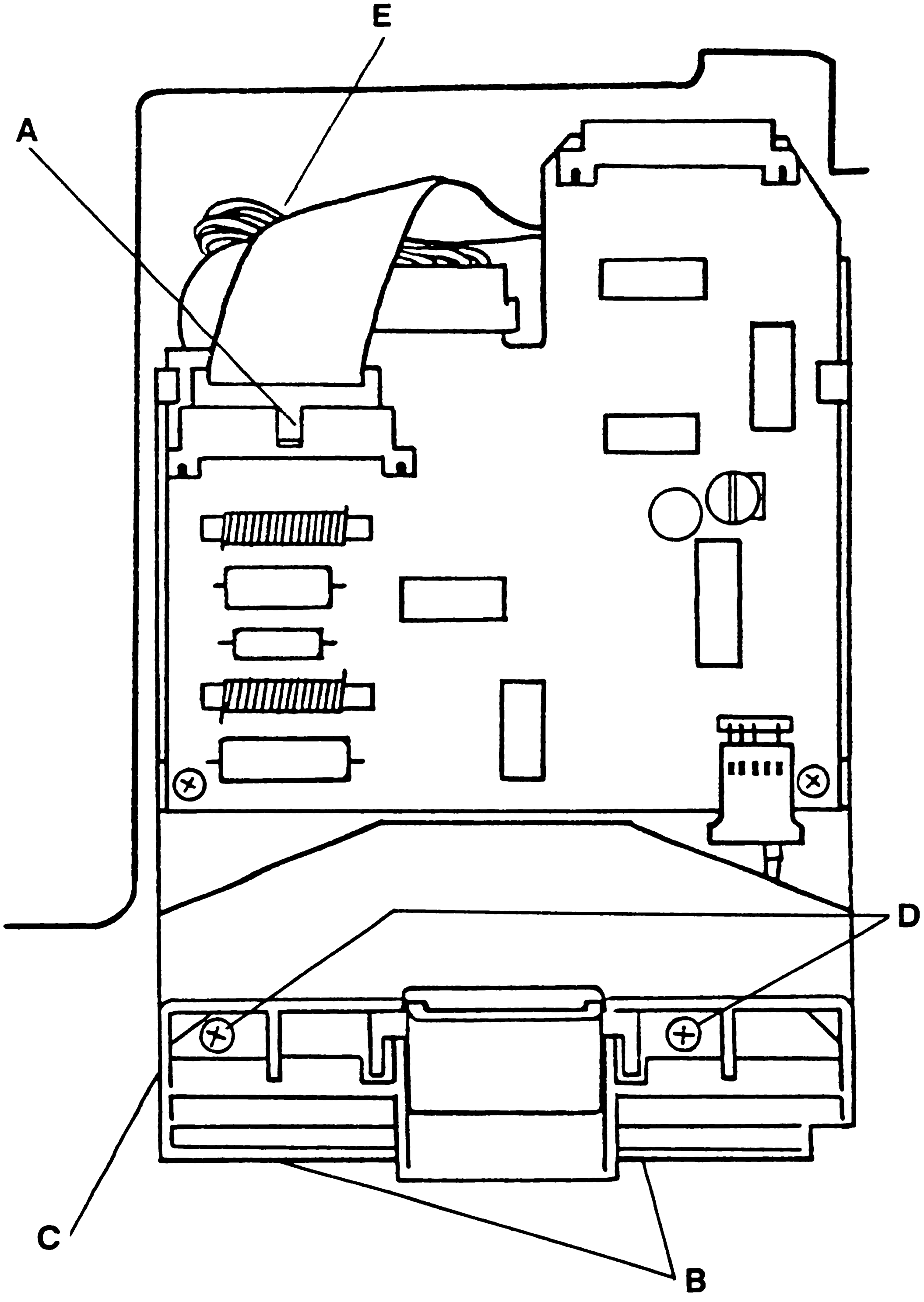


FIGURE 5.1

VI. POWER SUPPLY REPLACEMENT

1. Power down the Apple ///. Disconnect the AC power cord from the source and then remove it from the power supply receptacle of the Apple ///.

2. Disconnect all external cables.

3. Turn the Apple /// upside down with the keyboard facing you and place on a soft pad.

NOTE: You may want to place a foam block under the keyboard to keep the unit from rocking while it is upside down.

4. Loosen (Don't Remove!) the two Phillips head screws located on the rear edge of the power supply bottom cover, near the on/off switch and power supply receptacle. Refer to Figure 6.1 item A.

5. Locate and loosen the eight (8) screws securing the power supply bottom to the chassis. Refer to Figure 6.1 item B. These screws may be captured and if so should not come free of the assembly.

6. Lift up the front edge and slide the power supply forward until the rear edge clears the two rear mounting screws. Gently lift up the power supply assembly to gain access to the electrical connector. Refer to Figure 6.2.

7. Disconnect the power supply connector by pressing in the tabs while gently pulling. Refer to Figure 6.2 item A. If the leads are secured to the power supply by a wire tie, cut the tie. The power supply can now be removed.

8. Prior to replacing or re-installing the supply replace the wire tie, if one was removed.

9. When re-installing the power supply, insert the cover under the two rear most screws and lower the power supply into place.

10. Tighten all screws.

CAUTION: When re-installing the securing screws use only enough torque to rotate the screw. These screws will strip out the chassis, if excessive torque is applied. Also, be certain that the screw is not starting at an angle to avoid cross-threading. If it appears the screw is cross-threading, back it out and try again.

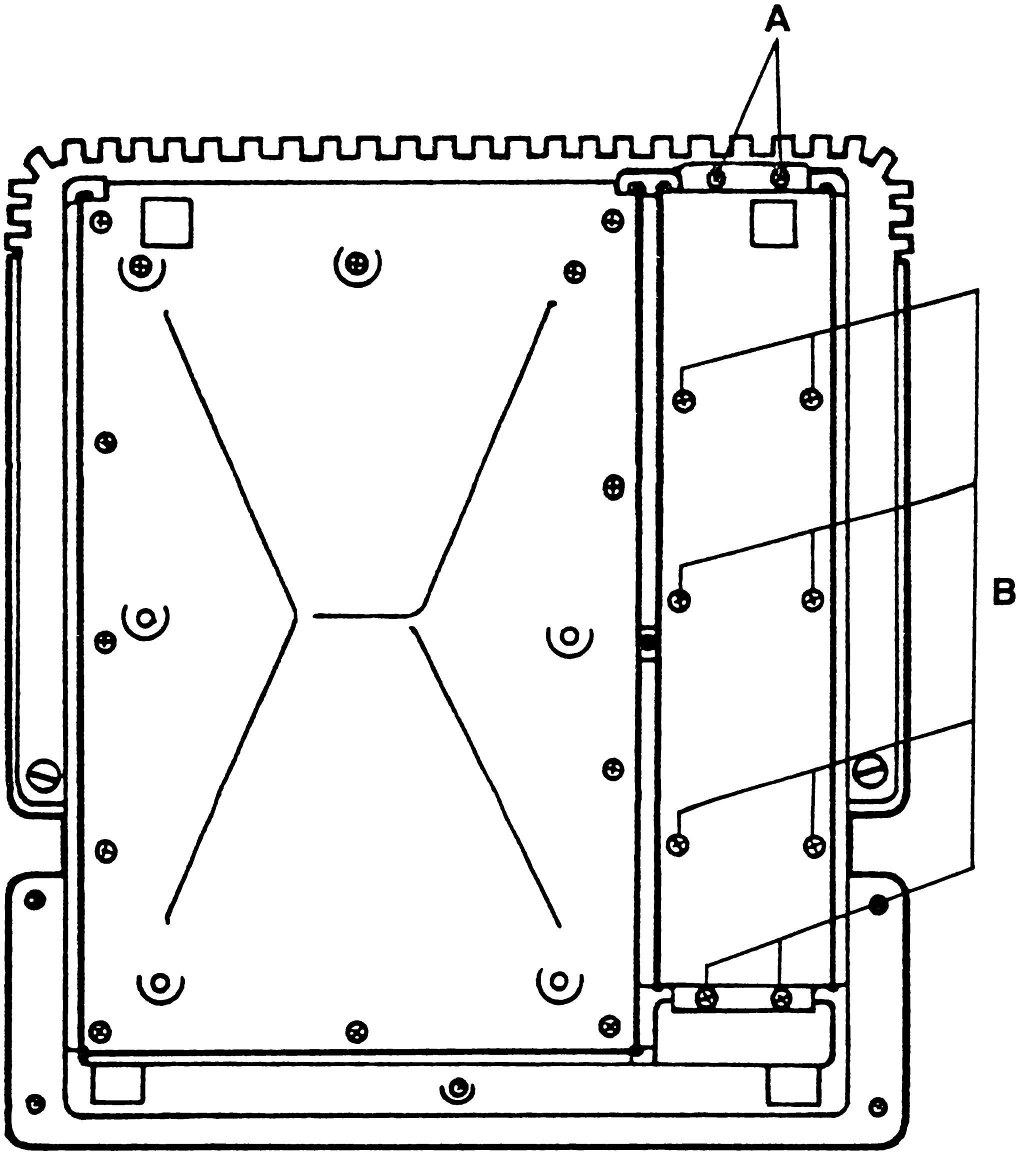


FIGURE 6.1

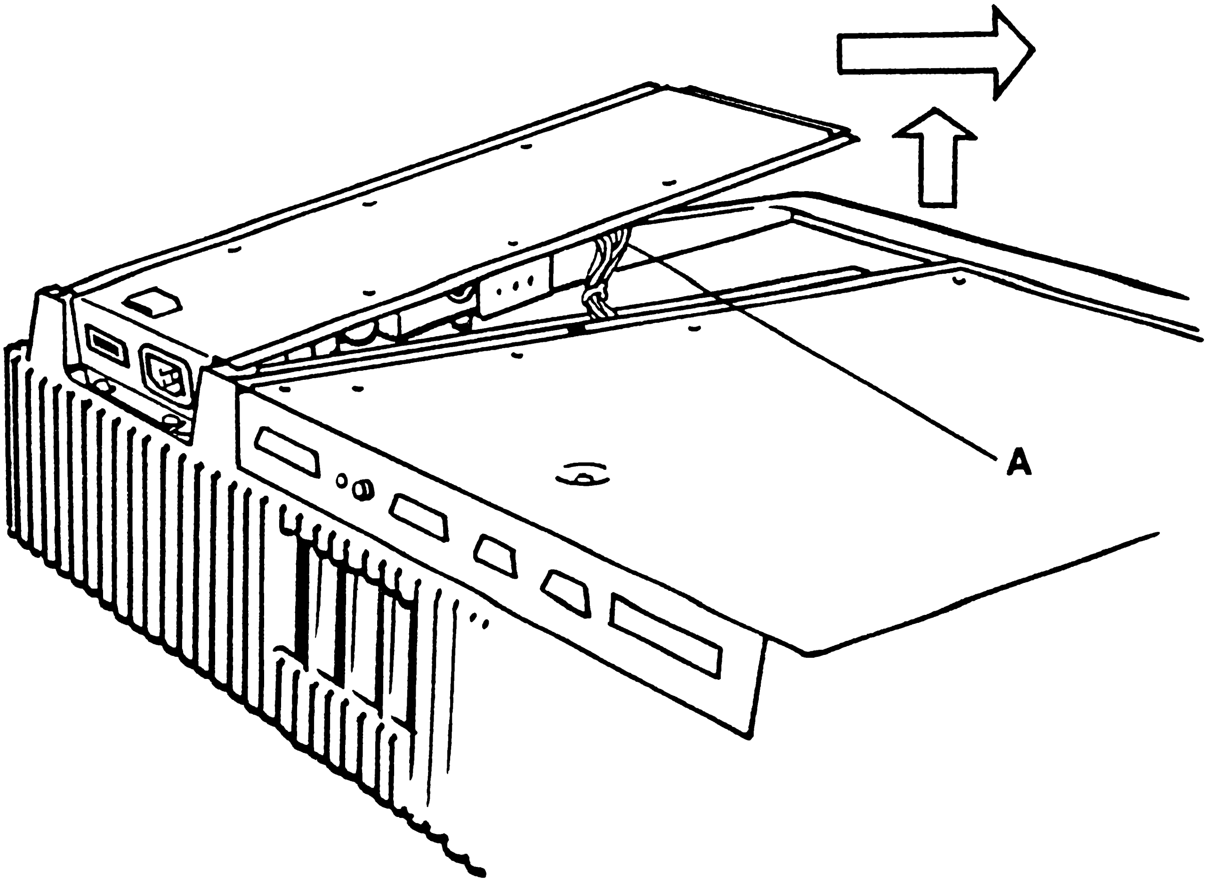


FIGURE 6.2

VII. LOGIC ASSEMBLY REMOVAL*

1. Power down the Apple ///. Disconnect the AC power cord from the source and then from the power supply receptacle of the Apple ///.

2. Disconnect all external cables.

3. Remove the peripheral logic access cover and all peripheral cards, or RFI shield cards. Refer to Procedure I and II.

4. Replace the access cover to protect disk bezel.

5. Place the Apple upside down on a soft pad. The rear of the Apple should face you.

6. Locate the ten (10) Phillips screws around the edge of the Logic access panel. Refer to Figure 7.1 item A. Locate the ~~two~~ ONE (~~2~~1) additional recessed screws that are about one and one-half inches in from the rear edge of the panel. Refer to Figure 7.1 item B.

7. Loosen these ~~twelve (12~~ eleven (11)) securing screws. These screws may be captured and if so should not come free of the access panel.

CAUTION: The logic board is attached to the access panel, and is still connected electrically to the keyboard, disk, speaker and the power supply. Cable travel allows the access panel to be tilted from the chassis about 45 degrees.

8. Slowly tilt up the access panel from the right side. Allow the panel to remain resting on its edge nearest the power supply. Refer to Figure 7.2.

9. Note the orientation and routing of the cables. While supporting the logic board from the underside remove the speaker cable (Figure 7.2 item A), the keyboard cable (Figure 7.2 item B), the disk cable (Figure 7.2 item C), and the power supply cable (Figure 7.2 item D).

10. The logic assembly is now free from the Apple and can be accessed for testing and repair.

11. To re-install the logic assembly reverse the procedure as outlined in steps 1 through 10 above.

CAUTION: Make sure cables are installed correctly and are not crimped or punctured by the mounting hardware when re-installing the logic assembly.

* The Logic Assembly is comprised of either three or four major elements, depending upon the time of manufacture. The earlier Logic Assemblies have four major elements: the access panel, the Main Logic board module, the Memory board module and the Encoder board module. The later Logic Assemblies have the Encoder board incorporated into the Main Logic board, and therefore, have three major elements: the access panel, the Main Logic board module and the Memory board module.

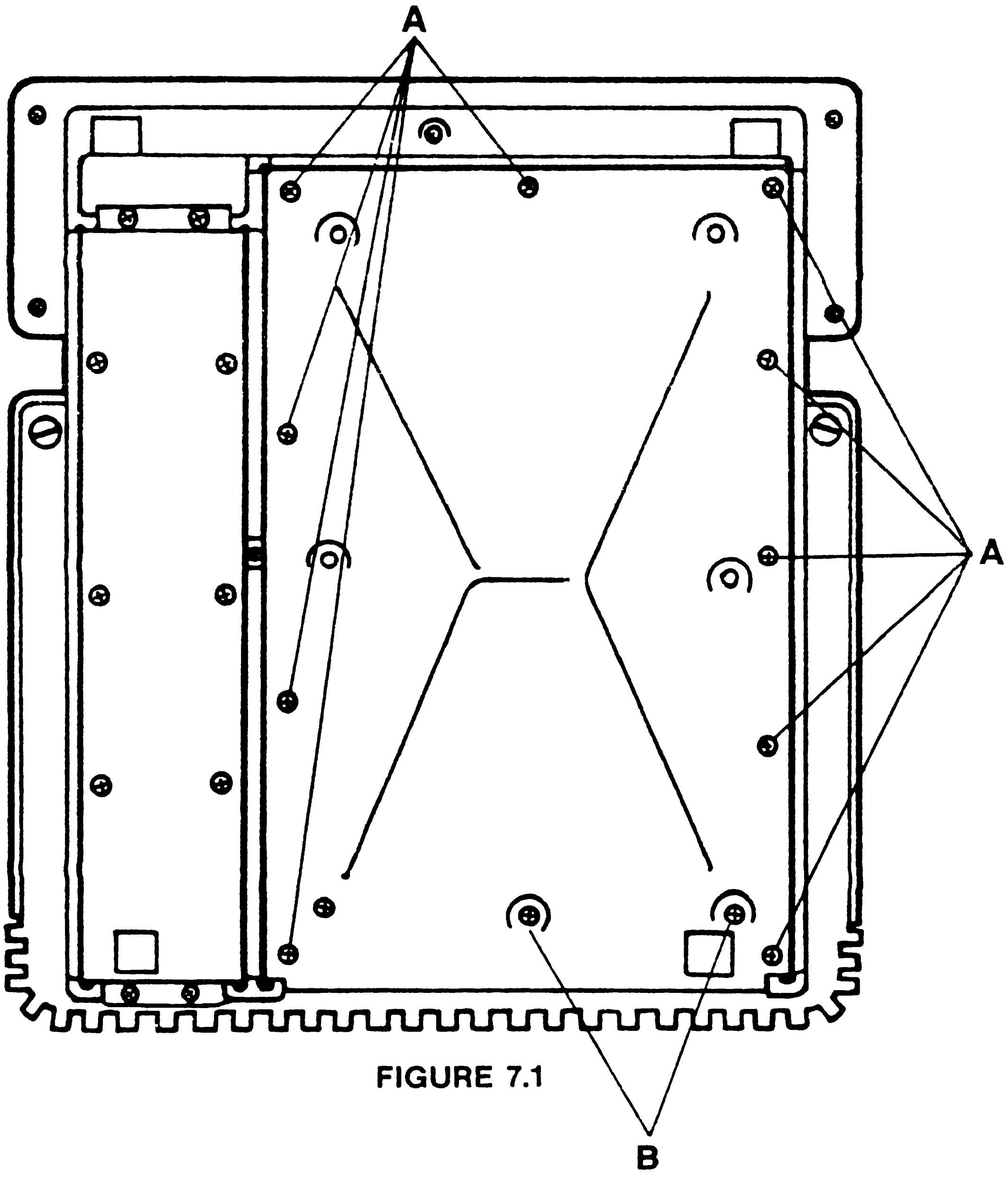


FIGURE 7.1

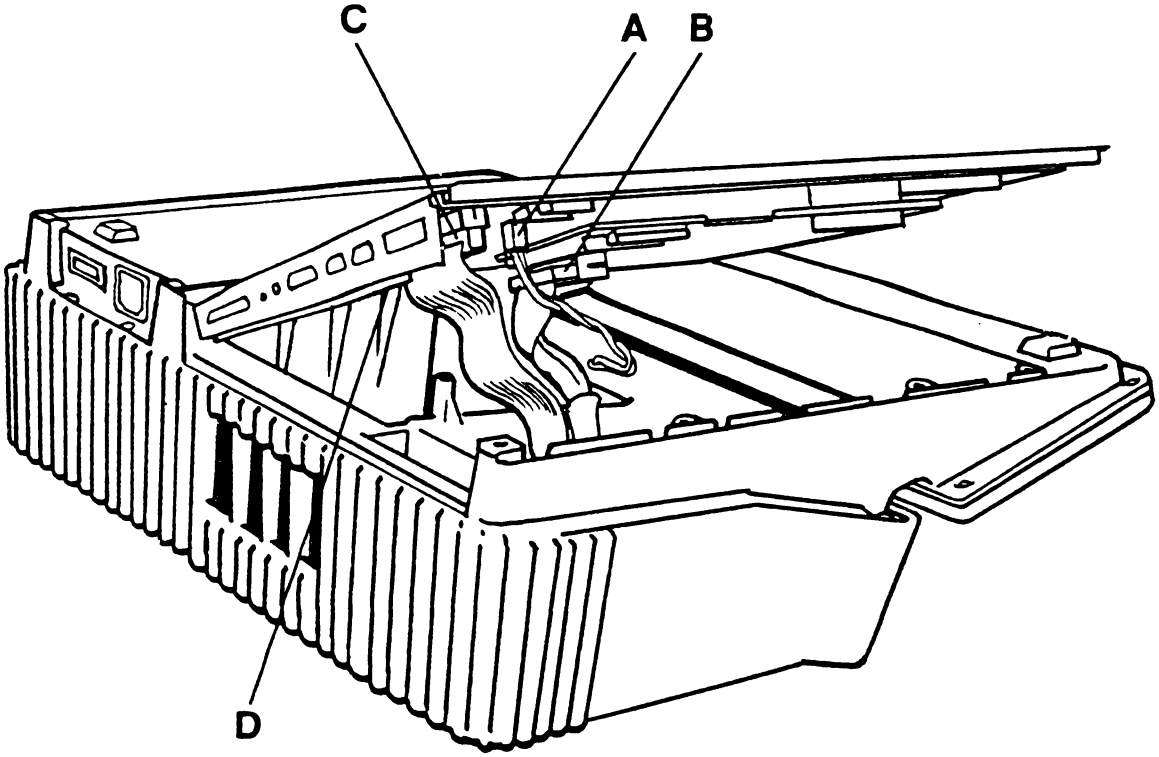


FIGURE 7.2

VIII. LOGIC ASSEMBLY REPLACEMENT

Before implementing any of this procedure the Logic Assembly must first be removed from the Apple. Refer to Procedure VII.

A. MEMORY BOARD REMOVAL

1. With the Logic Assembly placed flat on the work surface, use both hands to lift off the Memory board (Figure 8.1 item A) from the Main Logic board.

NOTE: The mechanical connection is also the electrical connection. Take care and lift straight up, or bending/breaking of the male connector pins mounted in the Main Logic board will occur.

B. MEMORY BOARD INSTALLATION

1. Align the connectors of the replacement Memory board over the connectors of the Main Logic board. The best way to do this is to tilt the Memory board and align the first pins on each side and lower the raised edge slowly, starting the next pins on each side as it is lowered.

CAUTION: Make sure that the board is properly oriented. The reference notches on the Memory board IC should face to the rear of the Logic Assembly (towards the output connectors).

2. Check that all the male pins are started correctly into the female connector of the Memory board. If any of the male pins are not properly started, lift up the Memory board slightly and "wiggle" it until the pins are aligned.

3. Once the pins of the connectors are all aligned, gently push straight down on the connectors on both sides of the Memory board until the connectors are fully seated.

C. ENCODER BOARD REMOVAL (early version of Logic Assembly only)

1. Locate Encoder board mount standoff. Refer to Figure 8.1 item B.

NOTE: The Encoder board connector on the Main Logic board has been re-formed for clearance purposes. This repositioning does not allow the standoff to match the pilot hole of the Encoder board. Therefore, the standoff can be removed, if you choose.

2. Remove the Encoder board from its connector.

D. ENCODER BOARD INSTALLATION (early version of logic assembly only)

1. Engage the replacement Encoder board on the connector and press into place.

E. MAIN LOGIC BOARD REPLACEMENT

1. Remove and retain the Memory board as detailed in Procedure VIII section A.

2. Remove and retain the Encoder board as outlined in Procedure VIII section C. (early version of logic assembly only)

3. Locate the retaining screw. Refer to Figure 8.1 item C. Remove and retain. Slide the board out from the peripheral connector opening of the access panel.

4. Lift off and set aside the Main Logic board.

CAUTION: Make sure that the insulating mylar shield (or substitute insulator) located between the board and the access panel remains in place before replacing the Main Logic board.

5. Place the replacement Main Logic board into the access panel, making sure that the peripheral connectors are aligned into their respective cutouts in the rear of the access panel.

6. Replace the retaining screw.

7. Replace the Encoder board. Refer to Procedure VIII section D.

8. Replace the Memory board. Refer to Procedure VIII section B.

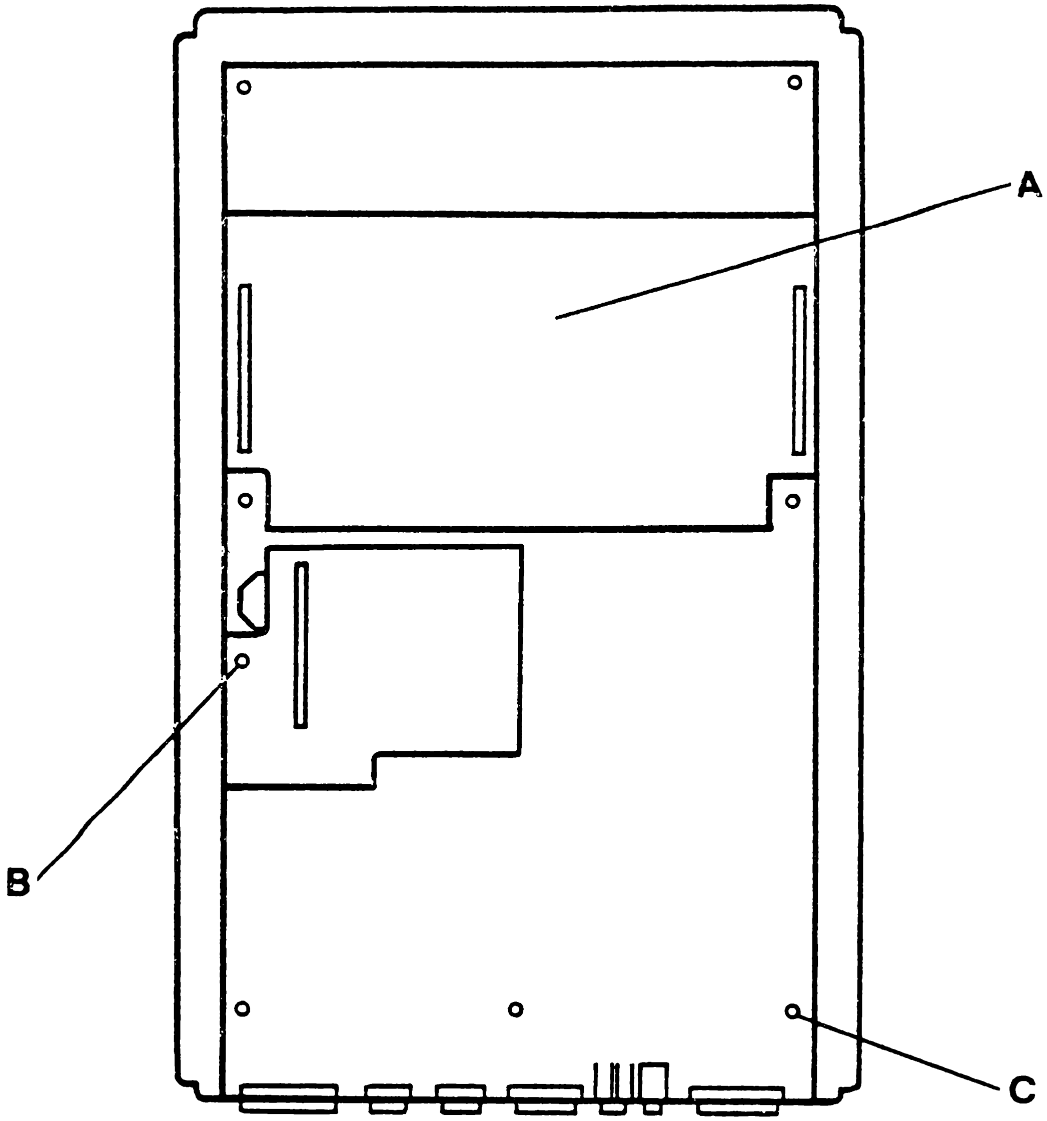


FIGURE 8.1

APPLE /// DEALER SERVICE DIAGNOSTICS REFERENCE

INTRODUCTION

The DIAGNOSTIC disk (part #652-0327), used in conjunction with this document will allow you to diagnose Apple /// failure modes at the modular level. Additionally, RAM failures may be diagnosed to the chip level.

The descriptions of the tests that follow contain information relative to the specific test environment that you are using. For instance, it will be necessary to evaluate test results differently when using color verses B&W monitors.

EQUIPMENT REQUIRED

Apple /// computer.
External Disk /// drives native to system under test.
B&W monitor w/ cable.
Apple /// Diagnostic diskette.
Apple /// External Test diskettes as required. *
* See MAKE TEST DISKS.

OPTIONAL EQUIPMENT

RGB Color Monitor, NTSC Color Monitor, or Color Receiver.
Sup'r'mod'II, for Color Receiver.
NTSC adapter, for Color Receiver and NTSC Color Monitor.
Cables.

EQUIPMENT SETUP

As ALWAYS, insure that the Apple /// POWER is OFF BEFORE CONNECTING OR DISCONNECTING ANYTHING from the Apple /// or any equipment connected to the Apple ///.

a. Connect external drives native to system under test.
b. Connect B&W Monitor to J10 or,
c. Where available: connect Color Monitor, NTSC adapter, and Sup'r'mod II to J5, as required.
d. Connect power sources to system under test.
e. Turn on monitor power.
f. Install Diagnostic diskette in UUT internal drive.
g. Install External Drive Test diskettes in external drives as required.

RUNNING DIAGNOSTICS

There are three critical operations that happen in order to run Apple /// Diagnostics.

With proper test setup configured as above and Diagnostic diskette installed in internal drive, turn on Apple /// power.

1. Power on internal diagnostic.
   This fast internal diagnostic is described further in Apple /// owners guide. Refer to that document with questions on the start-up diagnostic. Let it suffice to say that these tests must be passed before the disk boot process may begin.

2. Boot
   Disk boot is a several stage process that begins with the execution of a code block contained in ROM. On a successful

boot, control is passed to code loaded from disk. Several loads and transfers of control are made resulting in the loading and execution of the Diagnostic program.

3. Diagnostic
   Having come this far is a vote of confidence for correct system operation. Now, under control of the Diagnostic, a thorough investigation of system hardware resources may begin.

DIAGNOSTIC MENU
After a sucessful boot load of the diagnostic program, the following menu will be presented.

```
TEST ALL

VIDEO                    (NOT TESTED)
SOUND                    (NOT TESTED)
RAM MAP                  (NOT TESTED)
DISK                     (NOT TESTED)
KEYBOARD                 (NOT TESTED)
ROM                      (NOT TESTED)

RAM TEST
MAKE TEST DISKS

CHOOSE:

ESC(APE
  A(CCEPT S(KIP
```

The menu you actually see on the screen will show the 'TEST ALL' option in inverse video. This is to indicate that if the 'A' or A(CCEPT key is depressed, the inverse menu option will be selected for execution. Individual tests or the two special functions may be made candidates to A(CCEPT by S(KIPing through the list of menu options, with the 'S' or S(KIP key. As a menu option is S(KIPped, it is returned to normal video, and the next logical menu option is inverted or highlighted.
Finally, the Diagnostic program itself may be exited by depressing the 'ESC', or ESC(APE key. Actually the TAB key performs this function as well. This feature allows diagnostics running on an Apple][that use the same menu selection technique to 'feel' the same. ESC(CAPing the Diagnostic tests will prompt the user to reboot.

APPLE /// DEALER SERVICE DIAGNOSTICS REFERENCE

TEST ALL

A(CCEPTing this option will sequentially perform all of the diagnostic modules below:

- VIDEO
- SOUND
- RAM MAP
- DISK
- KEYBOARD
- ROM

Each of the Diagnostic modules operates in a manner identical to that encountered if each were A(CCEPTed individually. For a detailed discription of the various Diagnostic modules, consult the following sections for each module by name.

VIDEO

The VIDEO Diagnostic module will test all of the various screen and color modes available on the Apple ///. You will be asked to make a subjective evaluation of each of the video mode tests. Of course if you are not using a Color Monitor, you will not be able to verify that the colors used in the test are actually present. Users of B&W Monitors will only be able to observe the different colors used as 16 shades of grey. An additional inconvenience that B&W Monitor users will have to put up with is that many B&W Monitors are not capable of displaying 16 linearly arranged shades of grey with a single setting of the monitor controls. In the description of each of the video mode tests, a warning will be given if this problem is anticipated.

The responses used for all of the video mode tests uses the format below:

SPACE BAR	TEST PASSES
RETURN KEY	TEST FAILS
ESCAPE KEY	LEAVE VIDEO TESTS
LEFT ARROW KEY	RETRY THE TEST

Except for the text mode and 16 color tests, each of the tests will display the same pattern: A picture of Winston Curchill will appear in the upper left corner, and a grid of diagonal lines will appear in the upper right corner, followed by a prompt field at the bottom of the screen.

1. HIRES MODE 1 - B&W pattern.

2. HIRES MODE 2 - B&W pattern.

3. 280 x 192 COLOR HIRES MODE 1 - Will appear as a negative image. A color monitor will show red and black.

4. 280 x 192 COLOR HIRES MODE 2 - Will appear as a green and white/ or yellow pattern.

5. SUPER HIRES MODE 1 - B&W pattern as in 1.

6. SUPER HIRES MODE 2 - B&W pattern as in 1.

7. AHIRES TEST 1 - On this and test 8, the screen will be divided into 4 horizontal sections, each a different color. The top half of Winston and the diagonal pattern are blue. The first two lines of the message are green, and the last two lines of the message are gold or orange. You may expect to have difficulty resolving the gray scale differences that represent these colors on a B&W Monitor on this and test 8.

8. AHIRES TEST 2 - pattern as in 7.

9. COLOR BAR & GRAY SCALE TEST - will display vertical bars of different colors. The border is blue. The colors, in order from left to right are: white, aqua, yellow ,green, pink, grey, orange, brown, light blue, medium blue, grey, dark green, light purple, dark blue, magenta, and black.
When viewed on a B&W Monitor, these colors will appear as a grey scale darkening from: white on left to black on right. You may expect to have difficulty resolving the gray scale differences that represent these colors on a B&W Monitor on this test. Although you will not be prompted for a response on this test, you must respond in the manner defined above. (That is... press space bar if test passes, etc.)

10. APPLE II TEXT MODE 1 - This screen will display:

```
THE QUICK BROWN FOX JUMPS OVER THE LAZY DOGS

abcdefghijklmnopqrstuvwxyz    0123456789
                               (inverse)


                  ...
               (flashing)
```

11. APPLE II TEXT MODE 2 - will display:

```
22222222222222222222
22222222222222222222
22222222222222222222
                 222
                 222
                 222
22222222222222222222
22222222222222222222
22222222222222222222
222
222
222
22222222222222222222
22222222222222222222
22222222222222222222
```

12. APPLE /// 40 COLUMN TEXT MODE - display will be divided into sixteen

blocks each of one of the sixteen colors white through black. Each block will have a text phrase in a complementary color that describes the background color. You may expect to have difficulty resolving the gray scale differences that represent these colors on a B&W Monitor on this test. Although you will not be prompted for a response on this test, you are required to respond in the manner described above.

13. APPLE /// 80 COLUMN TEXT MODE - will display characters that are much smaller. In fact, you may expect to have difficulty reading these characters on a NTSC Color Monitor or Color Receiver due to the inherent 3.8 mhz bandwidth limitation of these types of displays. B&W composite video and RGB Color monitors will display this test screen in full splendor.

SOUND

1. SOFT BELL - The speaker will beep on and off. Press the space bar if you hear the sound. Press the return key of you do not.

2. HARD BELL - Same as 1. above but at a different pitch.

3. DAC OUTPUT - The digital to analog converter will produce a sound at the speaker output that periodically is of zero amplitude that grows in amplitude to be cut off again to zero amplitude. The change in amplitude should be regular and of constant pitch (except for the cut off of sound at max amplitude).

RAM MAP

This test does a cursory test of the ram to determine the configuration in the unit under test. The results will be displayed as a message discribing the ram map determined in the test. eg:

```
RAM MAP GOOD FOR A 128K SYSTEM
```

If the message does not correspond to the physical configuration determined by inspection, press press return key to reject test. If the message describes the true configuration, press the space bar.

DISK

At this time you will be prompted to remove the Apple /// Diagnostic Diskette, and to insert the Internal Drive Test Diskette. Previous to this point, you should have inserted any External Drive Test Diskettes in external drives as required. This setup is acknowledged by depressing the return key.
You will then be required to enter the number of external drives connected to the unit under test.
At this point the test runs automatically, terminated with a disk test summary for each drive specified above.

Upon completion of disk tests, you will be prompted to reinsert the Apple /// Diagnostic Diskette. You will acknowledge this operation by depressing the return key.

APPLE /// DEALER SERVICE DIAGNOSTICS REFERENCE

KEYBOARD

1. ALPHANUMERIC - depress each of the keys on the alphanumeric keyboard and verify that its representation on the display is removed.
Three keys require special key stroke sequences to test their function. These sequences are described at the top of the keyboard test screen. If, after depressing all alphanumeric keys, some key representations remain on the test display, then type the sequence CTRL-S.

2. SPECIAL FUNCTION KEYS - Depress the ALPHA LOCK key and note that the state of the ALPHA LOCK key changes. Leave the ALPHA LOCK key in the UP state.

Depress OPEN APPLE key and note that its state is reported as down.

Depress any key, (except SPACE or RETURN), and hold. Note the REPEAT SPEED. Anything from 5 to 15 / sec is acceptable. While holding a key down in repeat mode, depress the CLOSED APPLE key. Note that the REPEAT SPEED will increase to approximately double the normal rate.

Accept or reject this test as prompted at the bottom of the screen.

The SOLID APPLE key test will prompt you with a key stroke sequence that must be followed exactly. Perform the indicated operations as the test proceeds automatically.

3. NUMERIC KEYPAD - same as in 1. above.

ROM

This test is a straight forward go, no-go test, that reports the message: ROM PASSES... / ROM FAILS...

At this point, if you had selected the TEST ALL option, the main menu will appear with the test summary to the right of each of the test options.

OTHER DIAGNOSTIC OPTIONS

The Diagnostic Diskette menu contains two other options that may be accepted for execution. These options are separated from the options described above because they are 'one way' trips, in that upon completion of the execution of these modules, you will be required to reboot the unit under test. These modules are described below.

RAM TEST

This test performs a thorough exercising of all ram contained in the system. This test takes several seconds to complete and should not be interrupted. On invocation of this module however, you are given the chance to return to main menu.

Successful completion of this test module is indicated by the display of a diagnostic message on the upper left hand corner of the display. This message will contain a matrix of dots (.) and ones (1), if ram errors are encountered. These are placed in the matrix in a logical fashion. Ram chip failures may be determined by comparing ones (1) found in the displayed matrix against the ram chip locator matrix below.

B9	B8	B7	B6	B5	B4	B3	B2	*
B17	B16	B15	B14	B13	B12	B11	B10	*
B9	B8	B7	B6	B5	B4	B3	B2	
B17	B16	B15	B14	B13	B12	B11	B10	
C17	C16	C15	C14	C13	C12	C11	C10	
D9	D8	D7	D6	D5	D4	D3	D2	
D17	D16	D15	D14	D13	D12	D11	D10	
C9	C8	C7	C6	C5	C4	C3	C2	

* DISREGARD THESE TWO ROWS ON 96K SYSTEMS

NOTE: All other diagnostic messages displayed shall be disregarded.
No prompt will be given to reboot the system under test.

MAKE TEST DISKS

You will use this module to prepare Drive Test Diskettes used in the DISK test module described above.

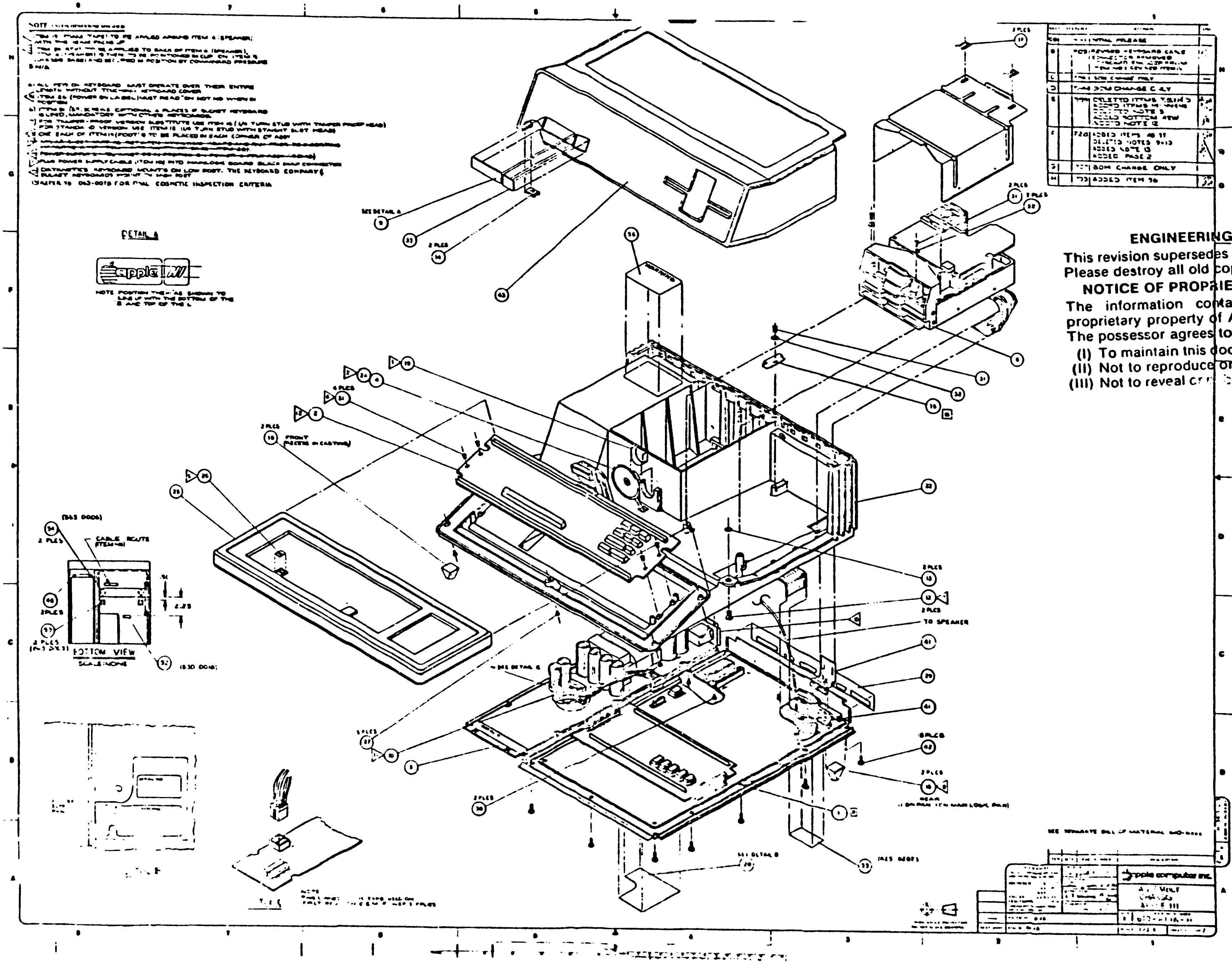
Upon accepting this module you will be prompted to remove the Diagnostic Diskette.

You will then be prompted to enter the drive number corresponding to the test diskette you wish to make. Enter this number <1 = internal , 2..4 = external>, followed by depressing RETURN.

You will be asked to insert a blank diskette into internal drive and acknowledge by depressing RETURN.

The utility will inform you that it is creating the test diskette for the drive that you specified in the operation above.

A 'DONE message' will be displayed on completion. You will be asked if you want to make another diskette. If you reply 'y' the above process will be repeated, otherwise you will be prompted to reboot.



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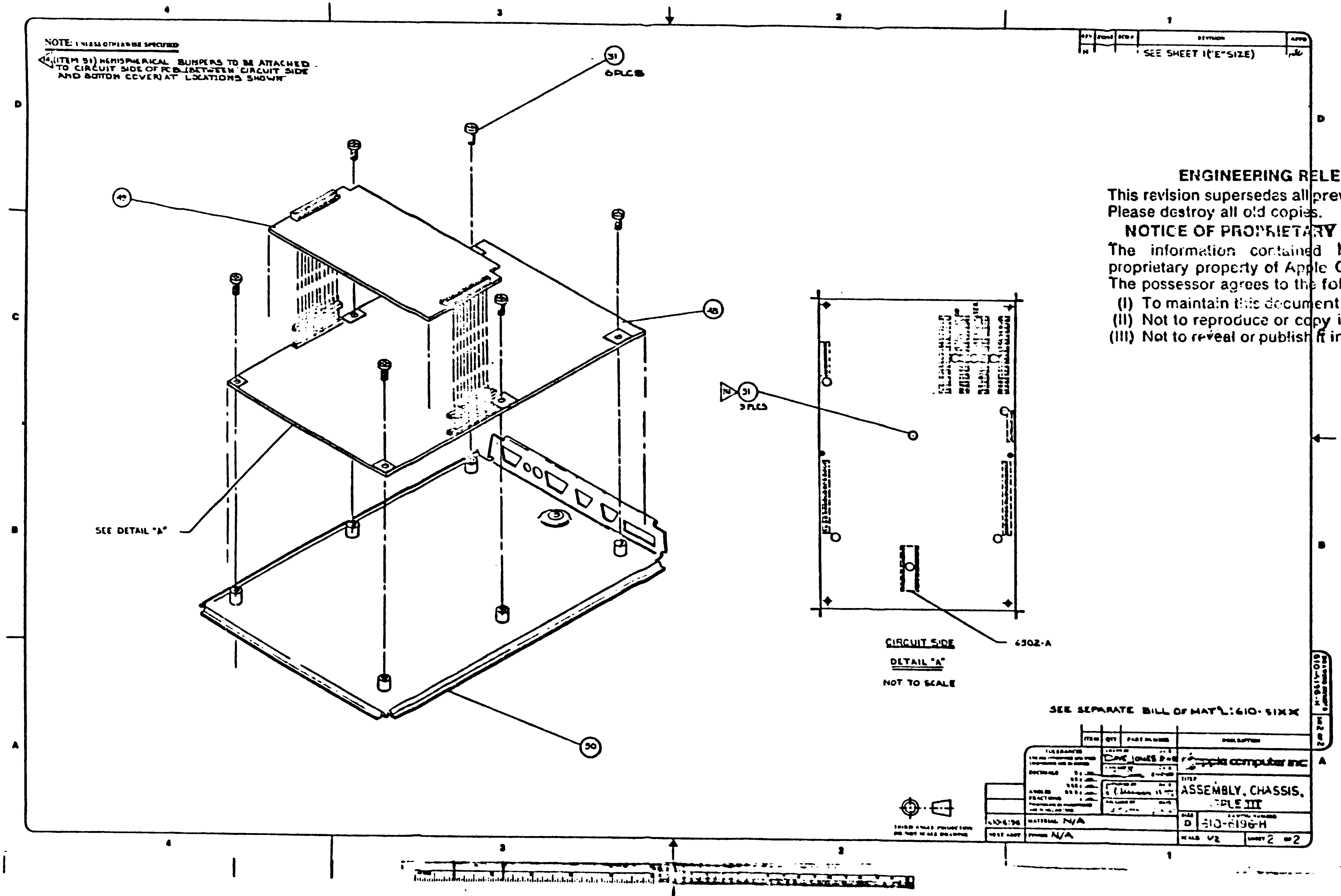

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FIG. 1

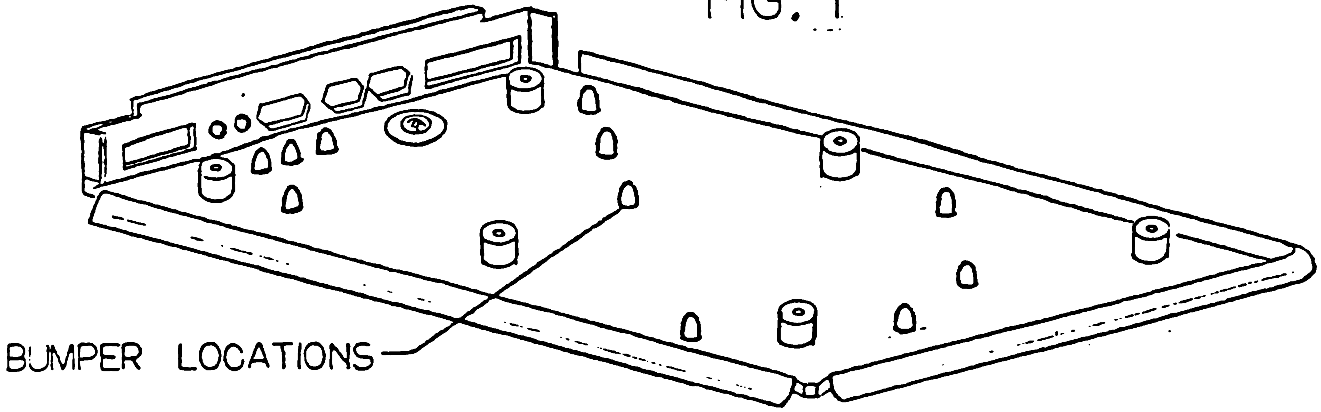
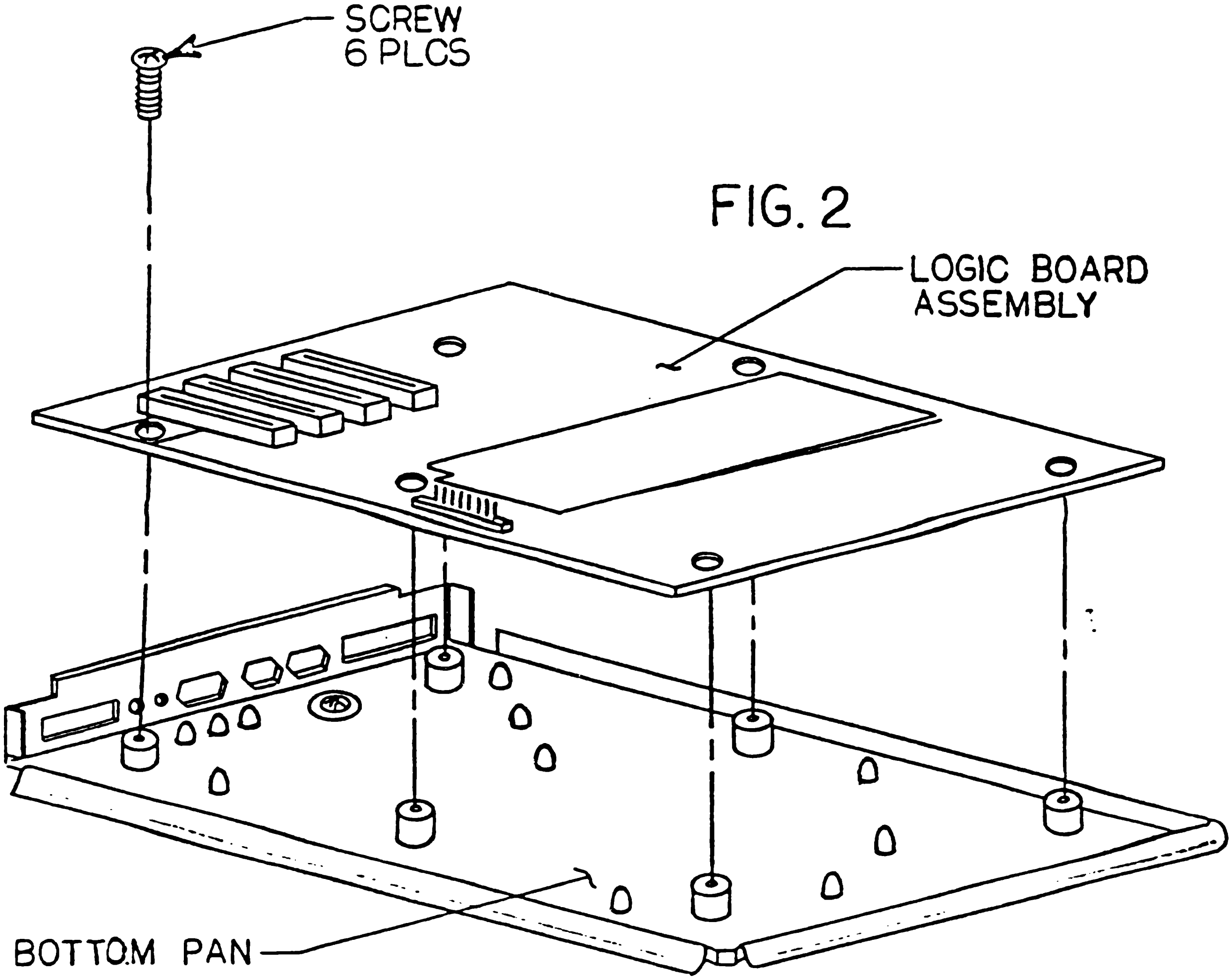


FIG. 2



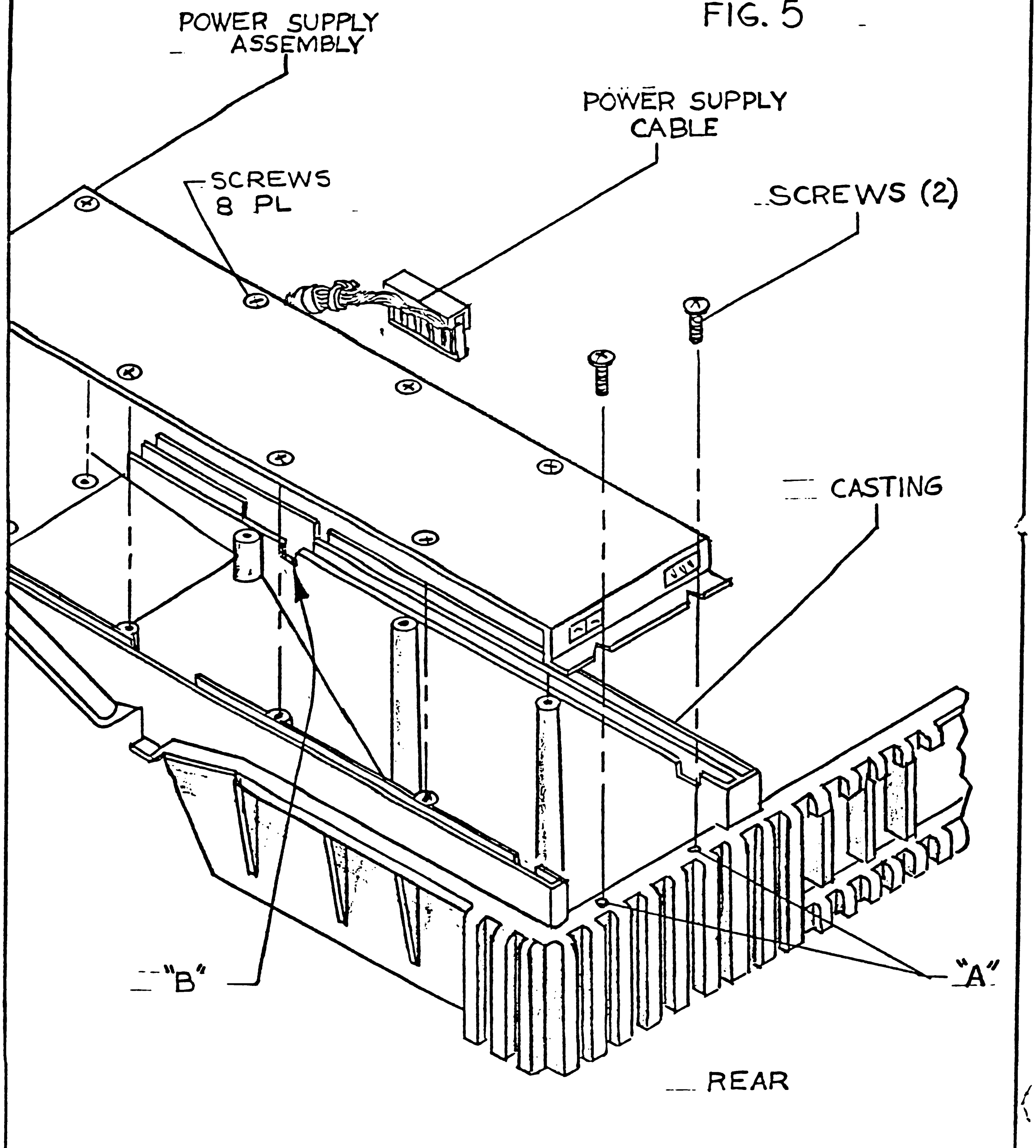
DRAWN BY	OPERATION NO.	TITLE
M. Castillo	A20	LOGIC BOARD PAN ASSY.

apple computer inc.

DOCUMENT NO. [illegible]-064-0156

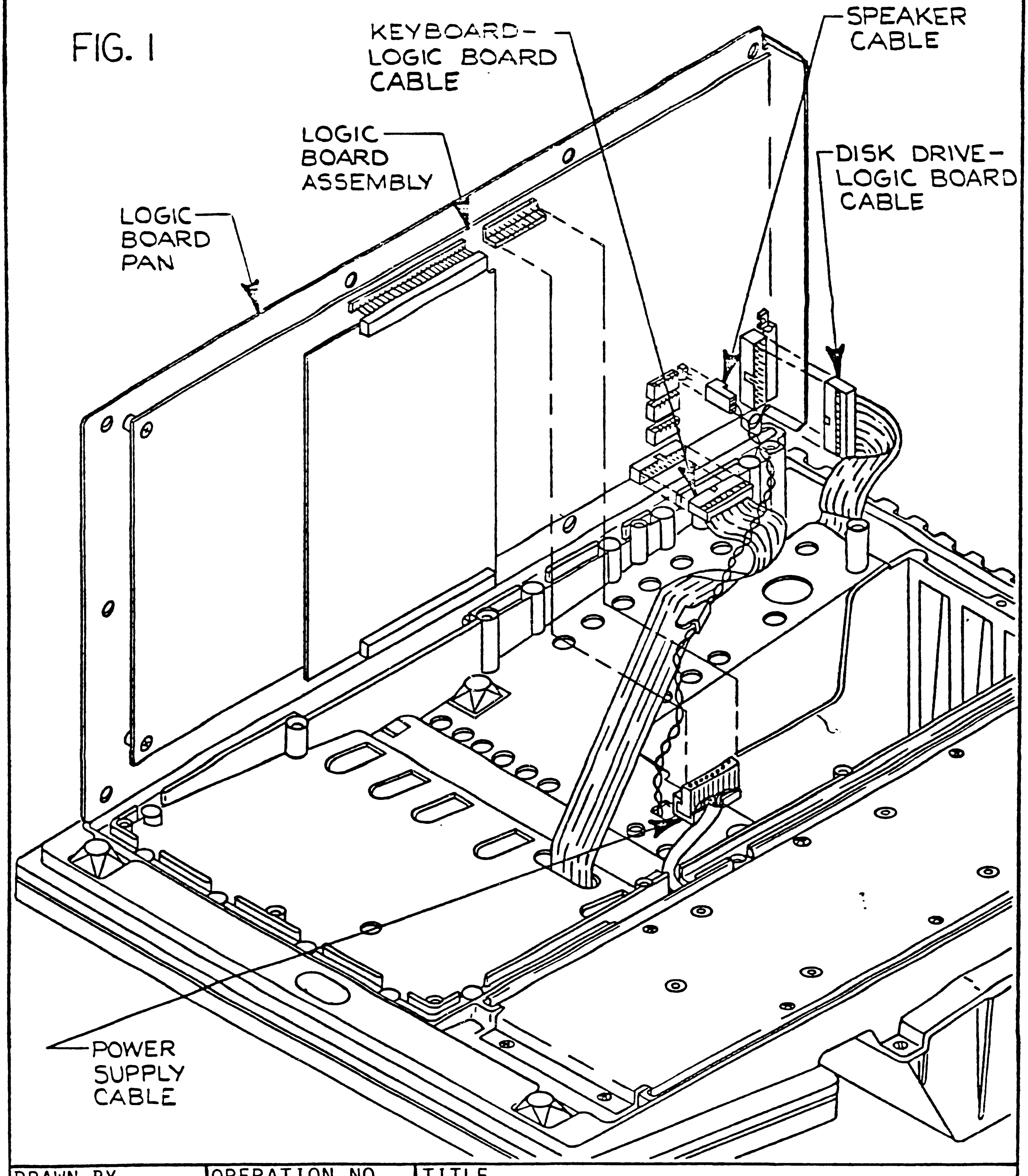
PAGE 11 OF 14

FIG. 5



DRAWN BY	OPERATION NO. 040	TITLE INSTALL POWER SUPPLY

FIG. 1



DRAWN BY	OPERATION NO.	TITLE
M. Castillo	050	INSTALL LOGIC BOARD ASSY.

apple computer inc.

APPLE /// SYSTEM OVERVIEW

FEATURING:

[] EXTENDED DISPLAY
[] EXPANDED RAM
[] NEW PROCESSOR DESIGN
[] BUILT IN I/O
[] APPLE II EMULATOR

STARRING: THE APPLE /// PROCESSOR

* 6502 INSTRUCTION SUBSET
* RELOCATABLE BASE REGISTER PAGE
* RELOCATABLE STACK
* 256K BYTE ADDRESS RANGE

VIDEO

* NTSC COLOR COMPOSITE VIDEO
* NTSC B/W COMPOSITE VIDEO
* SYNC
* 4 PRIMARY INDEPENDENT VIDEO LINES
* MIX TO FROM RGB APPLE COLORS
  THREE LINES CAN DRIVE TTL RGB MONITOR
  FOUR INDEPENDENT VIDEO OUTPUTS CAN BE GENERATED

DISPLAY MODES

* GRAY SCALE ON B/W OUTPUT
* RAM CHARACTER GENERATOR (128 CHAR.)
* 40 X 24 CHARACTER B/W TEXT (2K BYTES RAM)
* 80 X 24 CHARACTER B/W TEXT
* 40 X 24 CHARACTER COLOR TEXT
  (16 BACKGROUND, 16 TEXT COLORS)
* 280 K 192 B/W HIRES (8K RAM)
* 560 X 192 B/W HIRES
* 140 X 192 16-COLOR HIRES
* 280 X 192 16-COLOR HIRES WITH 40 X 192
  BACKGROUND/FOREGROUND RESOLUTION

I/O

* FOUR APPLE II BUS PERIPHERAL SLOTS
* ONE BUILT IN DISK DRIVE
* CONTROLLER FOR THREE ADDITIONAL DRIVES
* RS 232 PORT (COMPLETE)
* SILENTYPE PORT
* TWO PADDLE PORTS (A/D INPUTS)
* EXTERNAL SOUND JACK (SIX BIT AUDIO,
  HARDWARE BEEPER
* EXPANDED VIDEO LINES

- CLOCK/CALENDER

I/O BLOCK TRANSFER

- PERMITS UP TO 1 PAGE (256 BYTE) FAST I/O TRANSFER WITHOUT DMA HARDWARE ON PERIPHERAL

- TRANSFERS AT UP TO THE RAM CYCLE RATE

APPLE II EMULATION RESTRICTIONS

- NO LANGUAGE OR ROM CARD
- PADDLES ARE DIFFERENT
- ENTER WITH SOFTWARE BUT ONLY RESET WILL EXIT

6.1 Development Monitor

The current version of the diagnostic/boot ROM includes a monitor that may be useful for debugging. THE MONITOR IS NOT A PART OF THE SUPPORTED Apple III SOFTWARE AND IT MAY BE CHANGED OR DELETED IN FUTURE VERSIONS OF THE BOOT ROM. MONITOR SUBROUTINES MUST NOT BE CALLED FROM DRIVERS OR INTERPRETERS.

6.2 Monitor Commands

The monitor commands are listed below. Commands are read directly from the keyboard; blanks are not used except as data separators in a {byte list}. Command lines may be up to 79 characters long and are always terminated by a RETURN. Multiple commands may be entered on the same line using a slant (/) as a command separator. Numeric data is always entered in hex. ASCII strings may be entered by enclosing them in single or double quotes. If single quotes (´) are used, bit 7 of each byte will be clear; if double quotes (") are used, bit 7 will be set.

{address} ::= numeric value 0..FFFF
{address range} ::= {address} | {address}.{address}
{byte} ::= numeric value 0..FF | Single byte string
{byte list} ::= one or more bytes separated by blanks
{block num} ::= numeric value 0..117

{address range}	Memory dump
{address} : {byte list}	Memory store
{byte} < {address range} S	Memory search
{address} < {address range} M	Memory move
{address} < {address range} V	Memory verify
{block num} < {address range} R	Read disk
{block num} < {address range} W	Write disk
{address} G	Subroutine call (JSR)
{address} J	Execute code (JMP)
U	Call user subroutine (JSR $3F8)
X	Repeat command line
RETURN	Continue memory dump

When dumping memory, the output can be suspended then stepped by pressing the space bar; pressing any other key will resume normal output. Pressing the TAB key will terminate processing of the command line.

6.3 Escape Commands

Escape commands may be used during command input to move the cursor or control the display. Escape mode is entered by typing an ESCAPE; the cursor is changed to a flashing plus sign (+) to identify escape mode. Any character that is not an escape command will terminate escape mode.

↑ or K^c	Move cursor up
↓ or J^c	Move cursor down
← or H^c	Move cursor left
→ or U^c	Move cursor right

L	Clear to end of line
P	Clear to end of page
S	Home cursor and clear screen
4	Set 40 column display
8	Set 80 column display

6.4 Zero Page Locations

58	Window left
59	Window right
5A	Window top
5B	Window bottom
5C	Horizontal cursor position
5D	Vertical cursor position
74,75	A1
76,77	A2
78,79	A3
7A,7B	A4

6.5 Entering Addresses

adr1	A1, A2, A := adr1		
adr1.adr2	A1, A3 := adr1	A2 := adr2	
adr3<adr1.adr2	A1, A3 := adr1	A2 := adr2	A4 := adr3

6.6 Pointer Usage

Memory dump: (A1)
Memory store: (A3)
Memory move: (A4) := (A1)
Memory verify: (A4) : (A1)
Memory search: A4 : (A1)

APPLE /// LOGIC SIGNAL SOURCE

The location of the signal source is described first by the page number of the schematic followed by its coordinates.

SIGNAL	LOCATION	MEANING
6551sel*	5-4a	ACIA SEL
a0-a7	4-4d	ADDRESS BUS (EXTERNAL)
a8-a11	4-4c	
a12-a15	4-4b	
abk1	3-2c	ADDRESS BANK 1
abk2	3-2c	ADDRESS BANK 2
abk3	3-2c	ADDRESS BANK 3
abk4	3-2c	ADDRESS BANK 4
ahires	6-4a	AHIRES
aIIlores	6-4a	APPLE II LORES
altstk*	5-1b	ALTERNATE STACK
apple i*	9-4b	APPLE SWITCH 1
apple ii*	9-4b	APPLE SWITCH 2
ar0	3-3b	RAM ADDRESS X
anyky	9-4c	ANYKEY (DEPRESSED)
ar0	3-3d	
ar1	3-3d	
ar2	3-3c	
ar3	3-3c	
ar4	3-3c	
ar5	3-3b	
ar6	3-3b	
audio	8-1b	
ax,ax*	10-3a	ADDRESSS MUX SELECT
axco	5-2a	
bcksw1,3	8-4b	BANKSWITCH
bl	10-1b	BLANKING
c08xn-c0Fxn	5-4a	ADDRESS DECODE
c0xxn-c7xxn	5-4b	ADDRESS DECODE
c1m,c1m*	5-4b	CLOCK 1 MEGHERTZ
c14m,*	10-4c	CLOCK 14 MEGHERTZ
c3,5m,c3,5m*	10-4c	
c7m,c7m*	10-4b	
caplk*	9-4b	CAPS LOCK SWITCH
cas0*	3-2c	COLUMN ADDRESS SELECT (RAM)
cas1*	3-2c	
cas2*	3-2c	
cas3*	3-2c	
cas4,7*	3-2c	
cas5,6*	3-2c	
ch80*	6-4a	CHARACTER (80 COLUMN)
clkbat	5-2d	CLOCK BATTERY
clken80	6-2d	CLOCK ENABLE 80 (COLUMN)

clkirq*	5-1c	CLOCK INTERRUPT
clrkl*	6-4a	
clrstrb*	6-3a	CLEAR STROBE (KEYBOARD)
colrgate	10-1b	COLOR GATE
comp	10-1b	COMPENSATE
control*	9-4b	CONTROL KEY
cs6522	10-4a	
cts	8-1c	CLEAR TO SEND (EIA)
c00x-c07x	5-3a	ADDRESS DECODE
cxxx	5-4b	
c-fxxx	5-4c	
d0-d7	4-2c	
da0,da7	10-3b	
datain	8-1c	EIA
db0-db7	10-4b	
dc0,dc7	6-3d	VIDEO BUS (CHAR GEN OUT)
dcd	8-1c	DATA CARRIER DETECT
devsel1,6*	5-4a	DEVICE SELECT
dhires	5-4a	DHIRES
dma1*	4-4d	DIRECT MEMORY ACCESS IN
dmaok	4-4a	DMA OK
dph0,dph3	7-4b	DISK (MOTOR) PHASE X
dsply	10-1b	DISPLAY
dsr	8-1c	DATA SET READY (EIA)
dtrdy,*	9-4c	DATA READY (KEYBOARD)
dtr	8-1c	DATA TERMINAL READY
dv0,dv7	6-4d	VIDEO BUS (RAM LATCH OUT)
dxo,dx7	6-3a	VIDEO BUS (COLOR LATCH OUT)
en257	5-3d	ENABLE RAM BUS TO DATA BUS
en8304	5-3d	ENABLE MPU XCVR
enbl1,e*	7-2c	ENABLE DISK 1 EXTERNAL
enbl1,i*	7-2c	ENABLE DISK 1 INTERNAL
enbl2,e*	7-2b	ENABLE DISK 2 EXTERNAL
enbl3,i	7-2b	ENABLE DISK 3 EXTERNAL
encwrt	7-2c	ENABLE CHARACTER RAM WRITE
enhreg*	3-3c	ENABLE GRAPHICS REGISTER (LATCH)
ensel	7-2c	ENABLE EXT PRINTER SELECT
ensio	7-2c	ENABLE SERIAL I/O
PDL0	5-2a	PADDLE ADDRESS 0
ext*	7-4b	EXTERNAL (DRIVE)
extspk	8-1b	EXTERNAL SPEAKER
ffcx*	5-3c	
ffdx*	5-3c	
ffex*	5-3c	
fieldout	10-1b	
fspace*	5-3b	
gph1	5-3c	
gph2	5-3c	
h0,h3	10-2d	VIDEO STATE
h4,h5	10-2d	VIDEO STATE
hires	5-2a	
hpe*	10-2d	
id0-id7	4-3c	INTERNAL DATA BUS
ind*	3-3a	

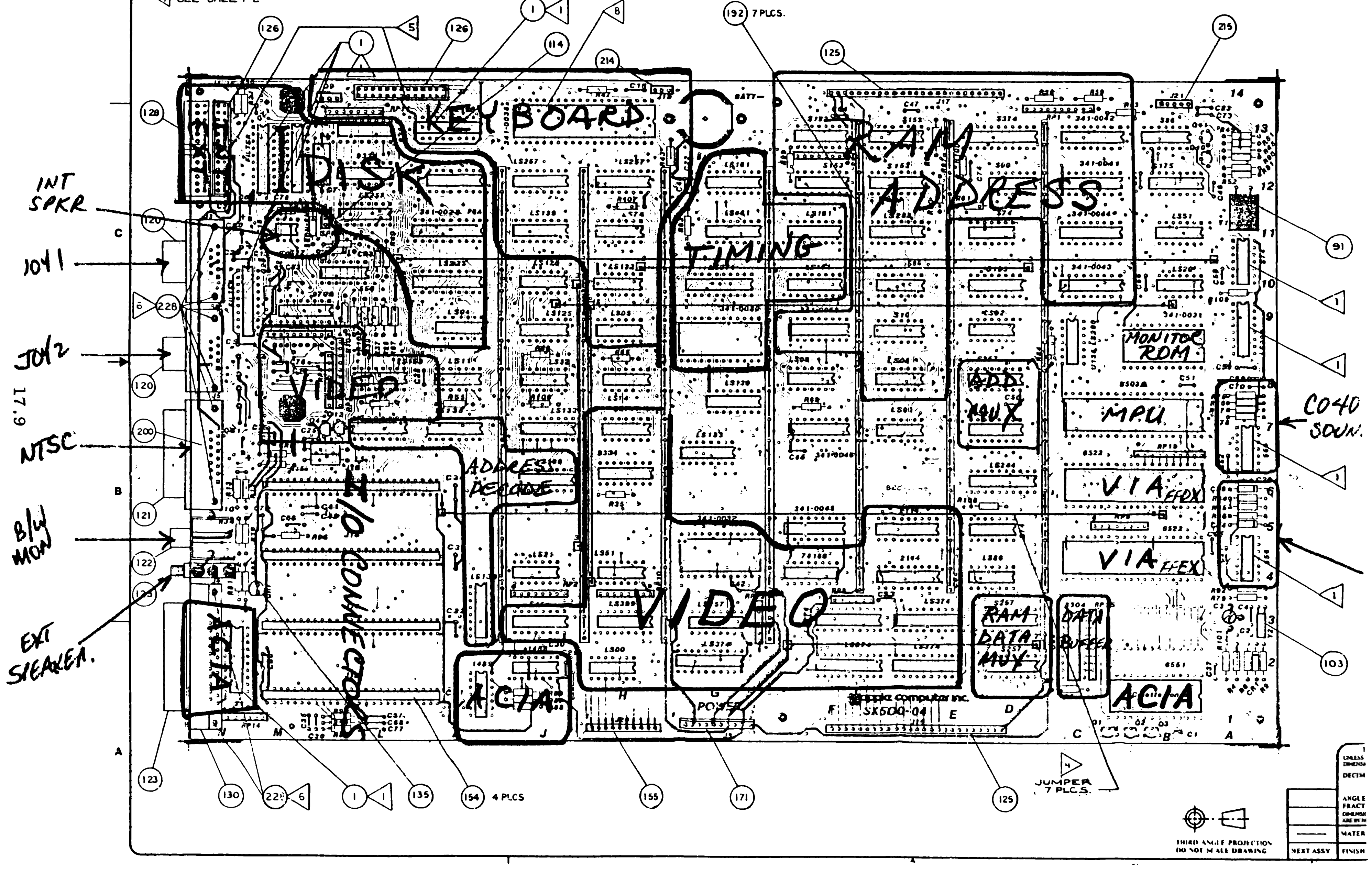
inh*	5-4c	INHIBIT (ROM)
int*	7-2d	INTERNAL (DRIVE)
blankin	8-3c	
ioen	5-1b	I/O (DEVICES) ENABLE
ionmi*	9-2b	I/O NON MASKABLE INTERRUPT
iosel1,4*	5-4b	I/O SELECT
iostopd*	10-4b	I/O STOPPED
iostrb*	5-4b	I/O STROBE
io sync	4-3b	I/O SYNC
irq1,4*	5-3c	
i r/w*	4-2c	INTERNAL READ/WRITE
i r/w*	4-3c	
kbint*	9-2c	KEYBOARD INTERRUPT
kbo*	5-3a	KEYBOARD STROBE(ENABLE KEY TO DATA)
kreset*	9-4b	RESET KEY
kvcc	9-4b	KEYBOARD VCC
ldps*	10-4c	LOAD PARARELL SHIFT REGISTER
mix	5-2a	
mux1	3-3c	
nmi*	9-1b	
ntsca,b	6-2b	
oe374	6-4a	ENABLE COLOR LATCH OUTPUTS
pa8	4-4b	PROCESSOR ADDRESS 8
pa15	4-4b	PROCESSOR ADDRESS 15
page 2	5-2a	
pcas0*	3-2d	PROM CAS X
pcas1*	3-2d	
pcas2*	3-2d	
pcas3*	3-2c	
pdint*	5-1c	POWER DOWN INTERRUPT (CLOCK)
pdl2	5-2a	PADDLE ADDRESS 2
pdlen	5-2a	PADDLE ENABLE (ADC RAMPSTART)
pdlot*	8-3a	PADDLE OUT (RAMPSTART)
pg2*	6-4a	
ph0	10-3a	PROCESSOR 0
ponrst	9-3a	POWER ON RESET
pras0,3*	3-2b	PROM RAS X
pras1,2*	3-2b	
pras4,5*	3-2b	
pras6,7*	3-2b	
preim	10-4b	PRE 1 MEGAHERTZ
pwrdwn*	5-2d	POWER DOWN
q0,q3	10-3c	Q STATE (ZMEG)
ram r/w	3-1b	
ras, ras*	10-4b	RAM ROW ADDRESS SELECT
ras0,3*	3-1b	
ras1,2*	3-1b	
ras4,5*	3-1b	
ras6,7*	3-1b	
rbl	10-1c	ROM BLANK
rclkpwr	5-2d	CLOCK POWER
rcolrgt	10-1c	ROM COLORGATE
rddata	7-2d	READ DATA (DISK)
rdy	3-3a	READY

rdy*	3-3a	
reset*	9-2b	
resetlk*	5-1b	RESET LOCK
rfield	10-1b	
rfsh	10-1b	REFRESH
rgb1,rgb8	6-3b	RED,GREEN,BLUE
romsel*	5-3b	ROM SELECT
romsel1	5-1b	
romsel2	5-1b	
rrfsh	10-1b	ROM REFRESH
rtcwrt	10-1c	ROM TIME CHARACTER RAM WRITE
rts	8-1c	REQUEST TO SEND
rsync	10-1c	ROM SYNC
rwpr	5-1b	
rwrprot	10-1b	
r/w	4-3c	READ WRITE
s399	3-3a	
s50/60	10-1b	SELECT 50 HZ/60 HR
sco	5-1b	SERIAL CLOCK
scr	7-2c	SCROLL
scrn	5-1b	SCREEN
sel2m*	5-1b	SELECT 2 MEG
sel374	6-4a	SELECT ORDER OF 374'S to dvx bux
ser	5-1b	SERIAL DATE
shift*	9-3c	SHIFT KEY
spkr*	5-3a	SPEAKER (STROBE)
sum4	3-3d	
sum3	3-3d	
sum2	3-3d	
sum1	3-3d	
synch	10-1b	
tcwrt	10-1b	TIME CHARACTER RAM WRITE
text	5-2a	
tromsel	4-3a	
tromsel*	5-3d	
tsadb*	4-4d	
txd	8-1c	
uselb	3-2c	MICROPROCESSOR SELECT B RAM BUS
v0,v1	10-2c	
v2,v5	10-2b	
va	10-2c	
vb,vc	10-2c	
vbl	10-1c	
we2114	6-4d	WRITE ENABLE CHARACTER RAM
wrdata	7-2d	WRITE DATE (DISK)
wramen	10-4a	WRITE RAM ENABLE
wrprot	7-2d	WRITE PROTECT
wrreq	7-2d	WRITE REQUEST
x0,x7	9-4c	KEY SCAN
y0,y9	9-4c	KEY SCAN
z0,z7	5-1b	ZERO PAGE ADDRESS BITS
zpage*	4-4b	ZERO PAGE

NOTE: UNLESS OTHERWISE SPECIFIED

1. COMPONENTS WITHOUT I.C. SOCKETS.
2) ALL OTHER COMPONENTS TO HAVE APPROPRIATE I.C. SOCKETS.
3. ~~INSERT COMPONENTS AS SHOWN, WITH NEGATIVE SIDE OF BATTERIES UP, TIGHTEN CAP (ITEM 173) SECURELY.~~
4. JUMPER WIRES ARE TO BE UNDER BUSS BARS (ITEM 192).
5. NOTE POLARIZATION
6. CONNECTORS TO BE RIVETED TO BOARD BEFORE SOLDERING (ITEM 228)
7. SEE SHEET 2

8. THE IC'S, AND THE COMPLETED ASSEMBLY MUST BE REASONABLY PROTECTED FROM DAMAGE DUE TO STATIC ELECTRICITY. P/N 341-0035 IS PARTICULARLY SENSITIVE TO STATIC. EXTREME CARE MUST BE TAKEN WITH THIS IC AND ASSEMBLIES CONTAINING THIS IC.



HOW TO READ PROM (ROM) LOGIC EXPRESSIONS

X′ -- The single quote at the end of an expression means that the state of the signal is true when low, or it may represent the inversion of the state of the signal.

* -- Defines a logic AND operation. The expressions on either side of the asterisk is ANDed.

+ -- Defines a logic OR operation. The expression on either side of the asterisk is OR′d.

() -- Defines the boundaries of a logic expression. A new expression is defined by what ever is inside of the brackets.

RULES FOR INTERPRETATION

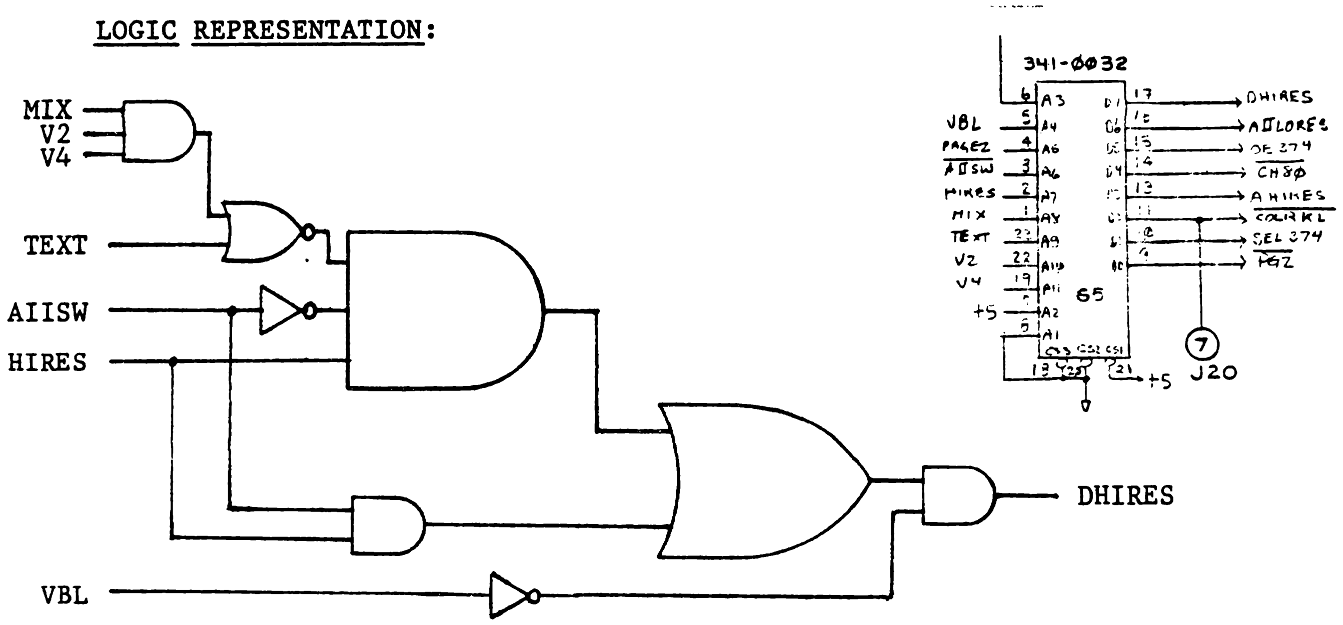
1. Always interpret (transform) the expression within the brackets first.
2. Interpret AND (*) logic operations before OR (+) operations.

EXAMPLE:

Given: INPUTS: AIISW′ HIRES TEXT
MIX V2 V4
VBL

OUTPUT: DHIRES = (AIISW*HIRES*(TEXT+MIX*V2*V4)′+AIISW′*HIRES)*VBL′

LOGIC REPRESENTATION:



PROM 341-0043

A=A11
B=A12
C=A13
D=A14
E=IOSYNC
F=SEL2M'
G=ABK4
H=PA8
I=A15
J=ZPAGE'
D0=S399
D1=PRDY'
D2=IND'

S399=ZPAGE*PA8'*A15'*A14'*A13'*A12*A11

PRDY'=IOSYNC*SEL2M*ABK4

IND'=(ABK4*(ZPAGE*PA8')')'

PROM 341-0042

```
A=A13
B=A11
C=A15
D=IND'
E=DHIRES
F=ABK1
G=ABK2
H=ABK3
I=A14
J=AY'
D0=PCAS4,7'
D1=PCAS5,6'
D2=PCAS1'
D3=PCAS2'

PCAS4,7'=(AY*IND'*ABK3'*A15'*(ABK1*ABK2'+ABK1'*ABK2)*(A14'*A13+A14*A13')+AY*
IND*ABK3'*(ABK2'*ABK1'*A15+ABK2'*ABK1+ABK2*ABK1'*A15')*A14'+AY*IND'*ABK1*
ABK2*ABK3'*(A15'*A14'*A13+A15*A14'*A13')+AY*IND*ABK3'*ABK2*(A15'*ABK1+A15*
ABK1')*(A14'*A13'+A14*A13))'

PCAS5,6'=(AY*IND'*ABK3'*(ABK1*ABK2'+ABK1'*ABK2)*(A15'*A14*A13+A15*A14'*A13')+
AY*IND*ABK3'*(ABK2'*ABK1'*A15+ABK2'*ABK1+ABK2*ABK1'*A15')*A14+AY*IND'*ABK1*
ABK2*ABK3'*(A15'*A14)+AY*IND*ABK3'*ABK2*(A15'*ABK1+A15*ABK1')*(A14'*A13+A14*
A13'))'

PCAS1' =(DHIRES *AY'+AY*(ABK1'*ABK2'*ABK3'*IND'+ABK1*ABK2*ABK3)*(A15'*A14'*
A13+A15*A14'*A13')+AY*IND*ABK1'*ABK2'*ABK3'*A15'*(A14'*A13'+A14*A13))'

PCAS2' =(DHIRES *AY'+AY*(ABK1'*ABK2'*ABK3'*IND'+ABK1*ABK2*ABK3)*(A15'*A14)+
AY*IND*ABK1'*ABK2'*ABK3'*A15'*(A14'*A13+A14*A13'))'
```

```
ROM 341-0032

A=A
B=B
C=S4
D=VBL
E=PAGE2
F=AIISW'
G=HIRES
H=MIX
I=TEXT
J=V2
K=V4
D0=PG2
D1=SEL374
D2=COLRKL'
D3=AHIRES
D4=CH80'
D5=OE374
D6=AIILORES
D7=DHIRES

PG2=AIISW'*(HIRES*MIX'*TEXT ')'*HIRES*PAGE2*S4*VBL'

SEL374=(VBL'*(AIISW*(PAGE2'*(TEXT +MIX*V2*V4)'+PAGE2*(TEXT +MIX*V2*V4))+
AIISW'*(HIRES*(PAGE2*S4)'+HIRES'*(PAGE2*S4))))'

COLRKL'=(AIISW*TEXT +AIISW'*(HIRES'*(MIX+TEXT ')+HIRES*TEXT '))'

AHIRES=AIISW'*(HIRES*MIX*TEXT )

CH80'=(AIISW'*MIX)'

OE374=(AIISW*HIRES'*(TEXT +MIX*V2*V4)'+AIISW'*MIX'*TEXT )'

AIILORES=AIISW*HIRES'*(TEXT +MIX*V2*V4)'+AIISW'*HIRES*MIX*TEXT

DHIRES=(AIISW*HIRES*(TEXT +MIX*V2*V4)'+AIISW'*HIRES)*VBL'
```

PROM 341-0046 U180

```
A=C1M
B=C07X'
C=RAMEN
D=DSPLY
E=IOSTOPD'
F=C-FXXX
G=FSPACE'
H=R/WN
I=RWRPROT
J=SEL2M'
D0=PCS6522
D1=PHASEN
D2=WRAMEN

PCS6522=(IOSTOPD'*C1M+FSPACE'*C1M')'

PHASEN=((SEL2M'*C07X')'*IOSTOPD'*FSPACE+FSPACE*C1M'+C1M'*SEL2M'+C1M'*DSPLY*
RAMEN)'

WRAMEN=RAMEN*(RWRPROT*C-FXXX)'*R/WN'*(DSPLY*C1M')'
```

PROM 341-0056

A=A11
B=A13
C=A14
D=A15
E=R/WN
F=DHIRES
G=AY'
H=ABK2
I=PRAS1,2
J=PRAS0,3
D0=PCAS0'
D1=PUSELB
D2=PCAS0,3
D3=PCAS3'

```
PCAS0'=(PRAS0,3 *(DHIRES'*AY'+AY*(A15'*A14'*A13'*A11'*R/WN'+A15'*A14'*A13'*
R/WN+A15*A14'*A13+A15*A14*A13'*A11)))'

PUSELB =PRAS0,3 *(A15'*A14'*A13'*A11+A15*A14*A13'*A11'+A15*A14*A13)+PRAS0,3 *
PRAS1,2 *(A15'*A14'*A13+A15*A14'*A13')+PRAS0,3 *PRAS1,2 '*(A15'*A14'*A13+A15'*
A14*A13')+PRAS0,3 '*PRAS1,2 *(A14'*A13'+A14*A13)+PRAS0,3 '*PRAS1,2 '*A14'

PCAS0,3 =(PRAS0,3 *(DHIRES'*AY'+AY*(A15'*A14'*A13'*A11+A15*A14*A13'*A11'+A15*
A14*A13))+PRAS0,3 *(DHIRES'*AY'+AY*(A15'*A14'*A13'*A11'*R/WN'+A15'*A14'*A13'*
R/WN+A15*A14'*A13+A15*A14*A13'*A11)))'

PCAS3'=(PRAS0,3 *(DHIRES'*AY'+AY*(A15'*A14'*A13'*A11+A15*A14*A13'*A11'+A15*
A14*A13)))'
```

PROM 341-0044 RAS

```
A=ABK1
B=ABK2
C=ABK3
D=PA15
E=AY'
F=PA8
G=ZPAGE'
H=DHIRES
I=RFSH
J=ABK4
D0=PRAS0,3
D1=PRAS1,2
D2=PRAS4,5
D3=PRAS6,7


PRAS0,3 =AY'*(DHIRES'+RFSH)+((ABK4*(ZPAGE*PA8')')'+ABK1*ABK2*ABK3)*AY

PRAS1,2 =AY'*(DHIRES+RFSH)+AY*(ABK1'*ABK2'*ABK3'*(ABK4*(ZPAGE*PA8')'*PA15)'+
ABK1*ABK2*ABK3)+AY*ABK3'*(ABK1'*ABK2*ABK4*(ZPAGE*PA8')'*PA15+ABK1*ABK2*(ABK4*(
ZPAGE*PA8')'*PA15)')

PRAS4,5 =RFSH*AY'+AY*ABK2'*ABK3'*(ABK1'*ABK4*(ZPAGE*PA8')'*PA15+ABK1*(ABK4*(
ZPAGE*PA8')'*PA15)')

PRAS6,7 =RFSH*AY'+AY*ABK3'*(ABK1*ABK2'*ABK4*(ZPAGE*PA8')'*PA15+ABK1'*ABK2*(
ABK4*(ZPAGE*PA8')'*PA15)')
```

PROM 341-0045 U176

```
A=C5XXN
B=R/WN
C=C6XXN
D=INH'
E=ROMSEL'
F=DMAI'
G=FSPACE'
H=PH2M
I=C7XXN
J=CXXX
D0=EN257
D1=EN8304
D3=RAMEN

EN257=(PH2M*R/WN*ROMSEL'*INH'*FSPACE'*(C5XXN *C6XXN*C7XXN*CXXX)')'

EN8304=(PH2M*FSPACE'*ROMSEL'*DMAI')'

RAMEN=ROMSEL'*INH'*FSPACE'*(C5XXN *C6XXN*C7XXN*CXXX)'
```

PROM 341-0055 U175.1

```
A=VA
B=VB
C=VC
D=VA1
E=VB1
F=VC1
G=DHIRES
H=SCR
I=WE2114'
J=VBL
D0=MUX1
D1=MUX2
D2=MUX3
D3=ENHREG'

MUX1=((DHIRES'+SCR*(VA*VA1'+VA'*VA1)+SCR'*VA)*VBL'+VBL)'+VBL*WE2114'*SCR*VC1

MUX2=(DHIRES*(SCR*(VA*VA1*(VB*VB1'+VB'*VB1)'+(VA*VA1)'*(VB*VB1'+VB'*VB1))+VB*
SCR'))'

MUX3=DHIRES*(SCR*((VA*VA1*(VB+VB1)+VB*VB1)*(VC*VC1'+VC'*VC1)'+(VA*VA1*(VB+
VB1)+VB*VB1)'*(VC*VC1'+VC'*VC1))+VC*SCR')

ENHREG'=DHIRES'*WE2114'
```

ASCII Conversion Tables

DEC	ASCII	OCTAL	HEX	BINARY 76543210	DEC	ASCII	OCTAL	HEX	BINARY 76543210
0	NUL	000	00	00000000	64	@	100	40	01000000
1	SOH	001	01	00000001	65	A	101	41	01000001
2	STX	002	02	00000010	66	B	102	42	01000010
3	ETX	003	03	00000011	67	C	103	43	01000011
4	EOT	004	04	00000100	68	D	104	44	01000100
5	ENQ	005	05	00000101	69	E	105	45	01000101
6	ACK	006	06	00000110	70	F	106	46	01000110
7	BEL	007	07	00000111	71	G	107	47	01000111
8	BS	010	08	00001000	72	H	110	48	01001000
9	HT	011	09	00001001	73	I	111	49	01001001
10	LF	012	0A	00001010	74	J	112	4A	01001010
11	VT	013	0B	00001011	75	K	113	4B	01001011
12	FF	014	0C	00001100	76	L	114	4C	01001100
13	CR	015	0D	00001101	77	M	115	4D	01001101
14	SO	016	0E	00001110	78	N	116	4E	01001110
15	SI	017	0F	00001111	79	O	117	4F	01001111
16	DLE	020	10	00010000	80	P	120	50	01010000
17	DC1	021	11	00010001	81	Q	121	51	01010001
18	DC2	022	12	00010010	82	R	122	52	01010010
19	DC3	023	13	00010011	83	S	123	53	01010011
20	DC4	024	14	00010100	84	T	124	54	01010100
21	NAK	025	15	00010101	85	U	125	55	01010101
22	SYN	026	16	00010110	86	V	126	56	01010110
23	ETB	027	17	00010111	87	W	127	57	01010111
24	CAN	030	18	00011000	88	X	130	58	01011000
25	EM	031	19	00011001	89	Y	131	59	01011001
26	SUB	032	1A	00011010	90	Z	132	5A	01011010
27	ESC	033	1B	00011011	91	[	133	5B	01011011
28	FS	034	1C	00011100	92		134	5C	01011100
29	GS	035	1D	00011101	93	]	135	5D	01011101
30	RS	036	1E	00011110	94		136	5E	01011110
31	US	037	1F	00011111	95	_	137	5F	01011111

DEC	ASCII	OCTAL	HEX	BINARY	DEC	ASCII	OCTAL	HEX	BINARY
32	SP	040	20	00100000	96	,	140	60	01100000
33	!	041	21	00100001	97	a	141	61	01100001
34	"	042	22	00100010	98	b	142	62	01100010
35	#	043	23	00100011	99	c	143	63	01100011
36	$	044	24	00100100	100	d	144	64	01100100
37	%	045	25	00100101	101	e	145	65	01100101
38	&	046	26	00100110	102	f	146	66	01100110
39	'	047	27	00100111	103	g	147	67	01100111
40	(	050	28	00101000	104	h	150	68	01101000
41	)	051	29	00101001	105	i	151	69	01101001
42	*	052	2A	00101010	106	j	152	6A	01101010
43	+	053	2B	00101011	107	k	153	6B	01101011
44	,	054	2C	00101100	108	l	154	6C	01101100
45	-	055	2D	00101101	109	m	155	6D	01101101
46	.	056	2E	00101110	110	n	156	6E	01101110
47	/	057	2F	00101111	111	o	157	6F	01101111
48	0	060	30	00110000	112	p	160	70	01110000
49	1	061	31	00110001	113	q	161	71	01110001
50	2	062	32	00110010	114	r	162	72	01110010
51	3	063	33	00110011	115	s	163	73	01110011
52	4	064	34	00110100	116	t	164	74	01110100
53	5	065	35	00110101	117	u	165	75	01110101
54	6	066	36	00110110	118	v	166	76	01110110
55	7	067	37	00110111	119	w	167	77	01110111
56	8	070	38	00111000	120	x	170	78	01111000
57	9	071	39	00111001	121	y	171	79	01111001
58	:	072	3A	00111010	122	z	172	7A	01111010
59	;	073	3B	00111011	123		173	7B	01111011
60	<	074	3C	00111100	124		174	7C	01111100
61	=	075	3D	00111101	125		175	7D	01111101
62	>	076	3E	00111110	126		176	7E	01111110
63	?	077	3F	00111111	127	DEL	177	7F	01111111

SERVICE AND SUPPORT NOTICE

APPLE /// INTERLACE KIT: INSTALLATION INSTRUCTIONS

A. INSTALLING THE APPLE /// INTERLACE KIT

NECESSARY TOOLS:

#1 and #2 Phillips Screwdriver
Needle Nose Pliers
Apple /// Interlace Kit

1. Remove the Apple /// Main Logic Board (the bottom tray need not to be removed from the Main logic Board) and top cover. For instructions on removing the Main Logic Board refer to page 1.15 of the Apple /// Technical Procedures.
   16.19 ff   of Service Ref Manual

2. Place the Main Logic Board on a flat surface in front of you so that the 3 Pin Molex Connector at J-19 is located to your right. Refer to the illustation of the A/// Main Logic Board (Figure 1). Due to the fact that a small percentage of Main Logic Boards have had the 3 Pin Molex Connector at J-19 clipped, it is necessary to inspect the connector. If the 3 Pin Connector has not been clipped then proceed with the installation instructions. If the Main Logic Board has had the 3 Pin Connector clipped you will need to obtain a Main Logic Board with the connector in place.
   341-0030-00   342-0145-A

3. Locate the IC socket at G-9 and remove the old IC. Insert the New IC into ther empty socket with the notch on top of the chip facing toward the front as shown in Figure 1. (see pages 5.9, 14.2, 14.3, 5.10, 11.10, 1.8 11.2 of SERVICE REFENCE MANUAL

4. Locate the Disk Drive Ribbon Cable hole in the casting (see Figure 2). Insert and route the Interlace Switch and attaching wires through the hole as shown.

5. Turn the Apple /// right side-up and locate the square hole in the upper right hand corner of the casting (refer to Figure 2). This is the hole you will install the Interlace Switch in. Because of the lack of room, it will be necessary to hold the hex nut with needle nose pliers. Insert the switch into the square hole and turn the switch clockwise until it fits snug against the casting.

6. Reinstall the Main Logic Board. Be sure the two pin Molex connector is connected to the lower pins of the 3 pin Molex connector at J-19 such that the lowest pin (refer to Figure 1) marked pin #3 has two wires going to it. Note the orientation of the ten pin Molex connector so that the 4th pin marked pin #7 at J-20 is connected.

7. Make all the necessary connections to the Main Logic Board and reinstall. Replace the Apple /// cover and make the necessary connections to hook-up the Apple /// to the external drive and monitor. Boot any word processor, switch on Interlace to verify that it is functioning properly.

8. If you have followed these procedures correctly, the space normally found in the characters will be filled in when the Interlace is activated.

B. INSTALLING THE MOLEX CONNECTOR

CAUTION: Any damage to the Main Logic Board resulting from the improper soldering of the three-pin Molex connector will be the responsibility of the Dealer. Apple will not accept such a board as an exchange module.

Remove the solder and/or wires from the holes marked J-19 on the Main Logic Board. The directions below for desoldering explain how this is done. Place the Molex connector in the holes. If the connector is a two pin Molex connector, place it in the two holes closest to the keyboard end (front) of the Main Logic Board. Finally, solder the connector to the board. The directions below for soldering explain how this is done. Be careful not to hold the connector by the metal leads as these leads heat up very quickly and can burn your fingers.

Soldering:

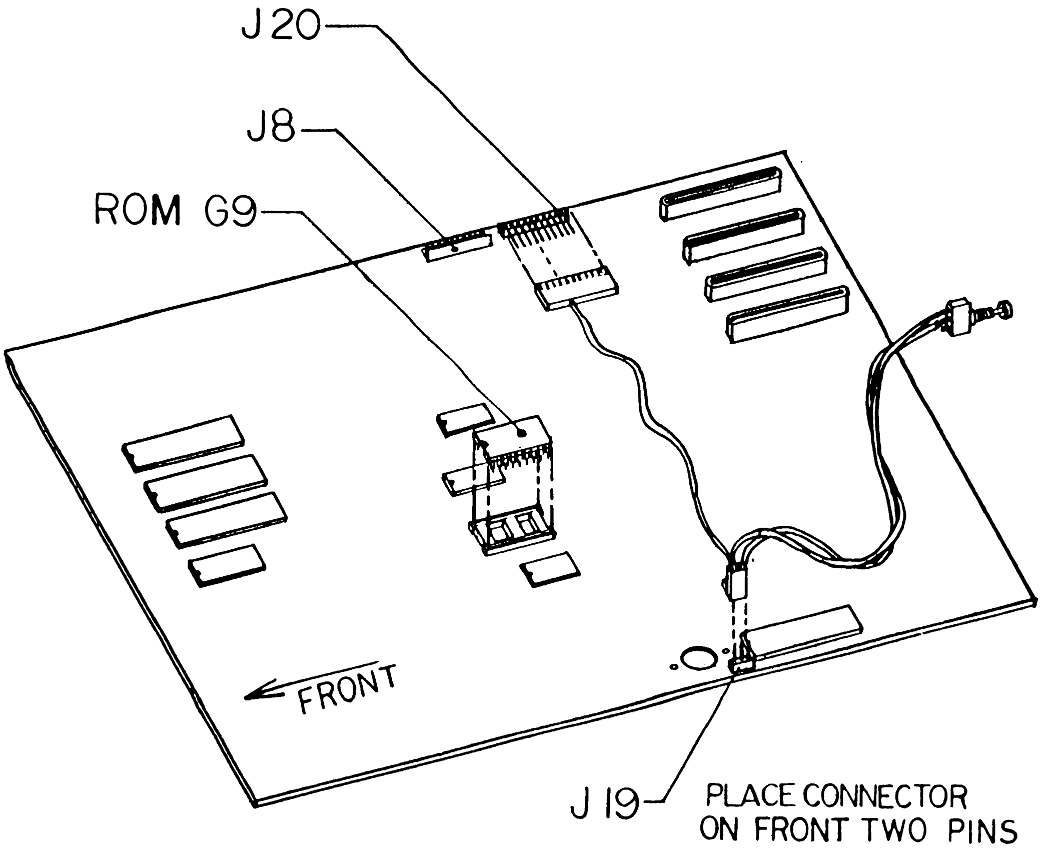
The first step is to properly clean and tin the soldering iron. It is important when soldering to avoid a cold solder joint. Proper soldering technique to avoid this calls for heat to be applied to the solder joint by a solder pencil or gun before placing the solder on the joint. When the joint is heated, bring the solder to the joint and allow the solder to flow over the parts being soldered, in this case the connector and printed circuit board pads. When the solder starts flowing, stop feeding more solder but keep the solder pencil or gun heating the joint. This will boil the solder flux away from the parts and allow the solder itself to adhere properly to the parts. Be careful not to apply too much heat as this can damage semiconductor components and cause printed circuit board pads to lift away from the board. Finally, remove the pencil or gun and keep the soldered joint stationary while it is cooling. After the joint has cooled, the parts can be moved. It doesn't take much solder to make a connection and too much solder tends to short the connection to nearby components, so use solder sparingly.

Removing Solder or Wires:

The best way to remove solder is with solder wick. Another method to remove solder is with a solder vacuum. To use the wick, the end of the wick is placed over the solder joint and then heat is applied to the joint until the solder melts. The solder will flow up the solder wick. The wick is then removed and the used end piece is cut off of the wick. This process is repeated until there is no solder left on the joint. To use the vacuum, the solder joint is heated with the solder pencil or gun until the solder is flowing. The vacuum is then placed over the joint and the solder is sucked into the vacuum. This process is also repeated until no solder remains.

After removing the solder, the parts can be freed by heating them once more and separating them with a pair of pliers. If this takes any noticeable pressure at all; if it does too much solder remains on the joint. Care must be taken with printed circuit board pads so as not to pull the pads off of the board. Likewise, component leads must not be pulled off of the components and the heat weakens the bond between the leads and the components. **BE CAREFUL!**

If the old solder cannot readily be heated to flowing, usually the addition of some fresh solder will cause both the new and old solder to flow. As with soldering parts together, a clean solder pencil with fresh solder applied to it gives the best results for melting solder or heating up components.



APPLE /// LOGIC BOARD

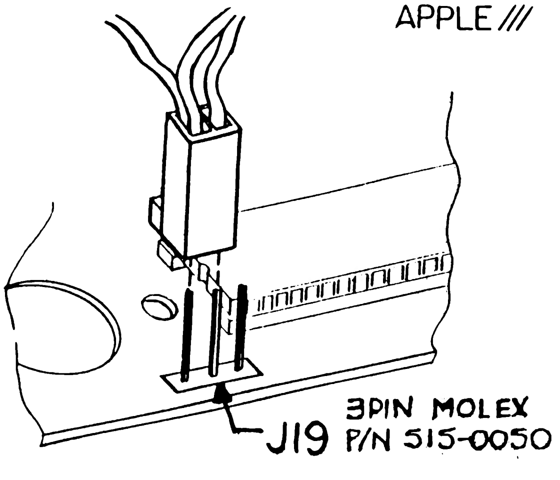


FIGURE 1

apple computer inc.	SIZE A	DRAWING NUMBER
	SCALE:	SHEET 3 OF 4

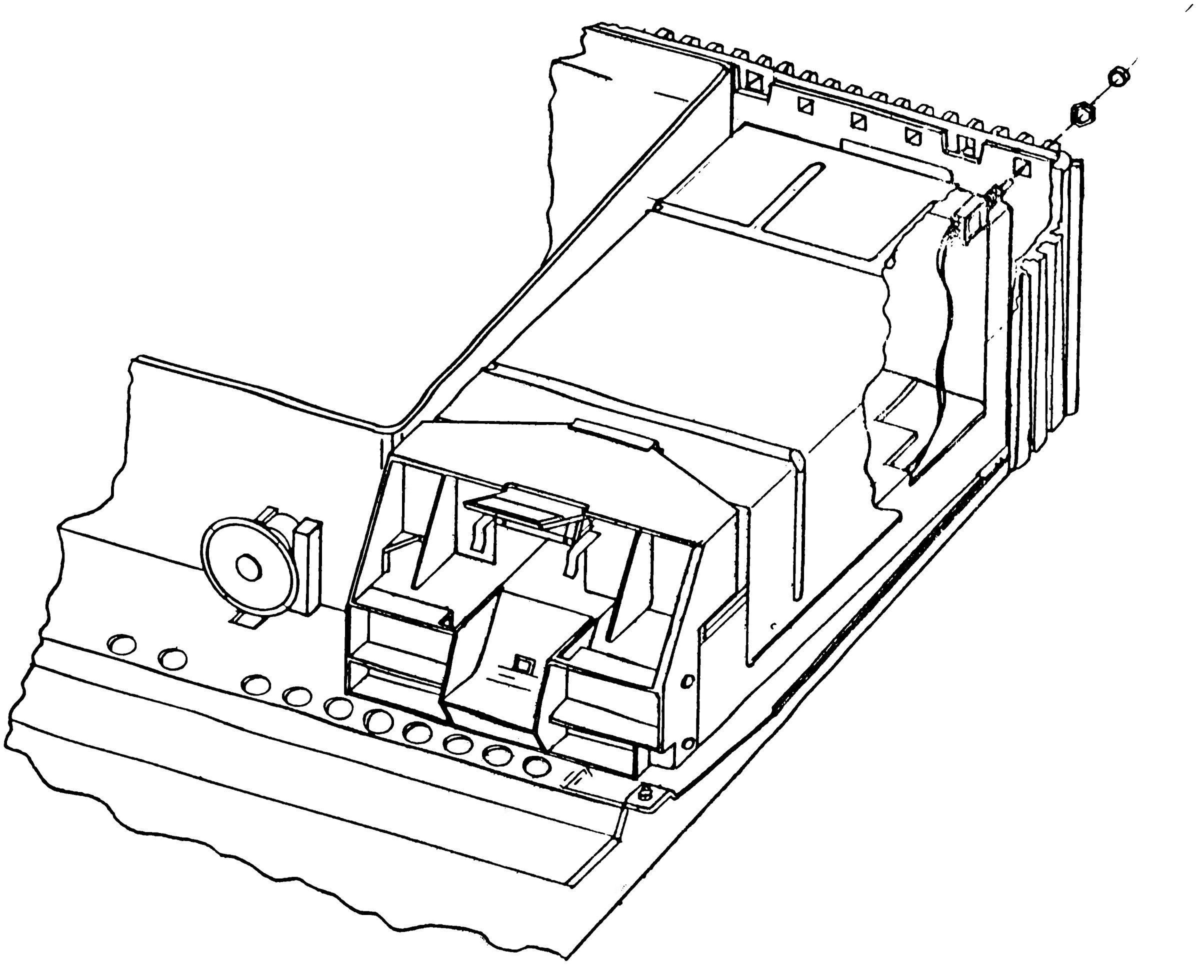


FIGURE 2

apple computer inc.	SIZE A	DRAWING NUMBER
	SCALE:	SHEET 4 OF 4